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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0+ |
| Core Size | 32-Bit Single-Core |
| Speed | 48MHz |
| Connectivity | I²C, SPI, UART/USART, USB |
| Peripherals | DMA, I²S, LVD, POR, PWM, WDT |
| Number of I/O | 23 |
| Program Memory Size | 256KB (256K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 32K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.71V ~ 3.6V |
| Data Converters | A/D 16x16b; D/A 1x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 32-UFQFN Exposed Pad |
| Supplier Device Package | 32-QFN (5x5) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mkl27z256vfm4r |

**Operating Characteristics**

- Voltage range: 1.71 to 3.6 V
- Flash write voltage range: 1.71 to 3.6 V
- Temperature range: –40 to 105 °C

**Packages**

- 64 LQFP 10mm x 10mm, 0.5mm pitch, 1.6mm thickness
- 64 MAPBGA 5mm x 5mm, 0.5mm pitch, 1.23mm thickness
- 48 QFN 7mm x 7mm, 0.5mm pitch, 0.65mm thickness
- 32 QFN 5mm x 5mm, 0.5mm pitch, 0.65mm thickness

**Security and Integrity**

- 80-bit unique identification number per chip
- Advanced flash security

**I/O**

- Up to 50 general-purpose input/output pins (GPIO) and 6 high-drive pad

**Low Power**

- Down to 54uA/MHz in very low power run mode
- Down to 1.96uA in VLLS3 mode (RAM + RTC retained)
- Six flexible static modes

## Ordering Information

| Product | | Memory | | Package | | IO and ADC channel | | |
|---|---|---|---|---|---|---|---|---|
| Part number | Marking (Line1/ Line2) | Flash (KB) | SRAM (KB) | Pin count | Package | GPIOs | GPIOs (INT/HD)[1] | ADC channels (SE/DP) |
| MKL27Z128VFM4 | M27P7V | 128 | 32 | 32 | QFN | 23 | 19/6 | 7/0 |
| MKL27Z256VFM4 | M27P8V | 256 | 32 | 32 | QFN | 23 | 19/6 | 7/0 |
| MKL27Z128VFT4 | M27P7V | 128 | 32 | 48 | QFN | 36 | 24/6 | 14/1 |
| MKL27Z256VFT4 | M27P8V | 256 | 32 | 48 | QFN | 36 | 24/6 | 14/1 |
| MKL27Z128VLH4 | MKL27Z128V//LH4 | 128 | 32 | 64 | LQFP | 50 | 31/6 | 16/2 |
| MKL27Z256VLH4 | MKL27Z256V//LH4 | 256 | 32 | 64 | LQFP | 50 | 31/6 | 16/2 |
| MKL27Z128VMP4 | M27P7V | 128 | 32 | 64 | MAPBGA | 50 | 31/6 | 16/2 |
| MKL27Z256VMP4 | M27P8V | 256 | 32 | 64 | MAPBGA | 50 | 31/6 | 16/2 |

1. INT: interrupt pin numbers; HD: high drive pin numbers

## Related Resources

| Type | Description | Resource |
|---|---|---|
| Selector Guide | The Freescale Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector. | Solution Advisor |
| Product Brief | The Product Brief contains concise overview/summary information to enable quick evaluation of a device for design suitability. | KL2XPB[1] |
| Reference Manual | The Reference Manual contains a comprehensive description of the structure and function (operation) of a device. | KL27P64M48SF6RM[1] |
| Data Sheet | The Data Sheet includes electrical characteristics and signal connections. | This document. |
| Chip Errata | The chip mask set Errata provides additional or corrective information for a particular device mask set. | KINETIS_L_1N71K[1] |
| Package drawing | Package dimensions are provided in package drawings. | 64-LQFP: 98ASS23234W[1] 64 MAPBGA: 98ASA00420D[1]32 QFN: 98ASA00615D[1] 48 QFN: 98ASA00616D[1] |

1. To find the associated resource, go to http://www.freescale.com and perform a search using this term.

## 1.4 Voltage and current operating ratings

**Table 4. Voltage and current operating ratings**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{DD}$ | Digital supply voltage | –0.3 | 3.8 | V |
| $I_{DD}$ | Digital supply current | — | 120 | mA |
| $V_{IO}$ | IO pin input voltage | –0.3 | $V_{DD}$ + 0.3 | V |
| $I_D$ | Instantaneous maximum current single pin limit (applies to all port pins) | –25 | 25 | mA |
| $V_{DDA}$ | Analog supply voltage | $V_{DD}$ – 0.3 | $V_{DD}$ + 0.3 | V |
| $V_{USB\_DP}$ | USB_DP input voltage | –0.3 | 3.63 | V |
| $V_{USB\_DM}$ | USB_DM input voltage | –0.3 | 3.63 | V |
| $V_{REGIN}$ | USB regulator input | –0.3 | 6.0 | V |

# 2 General

## 2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

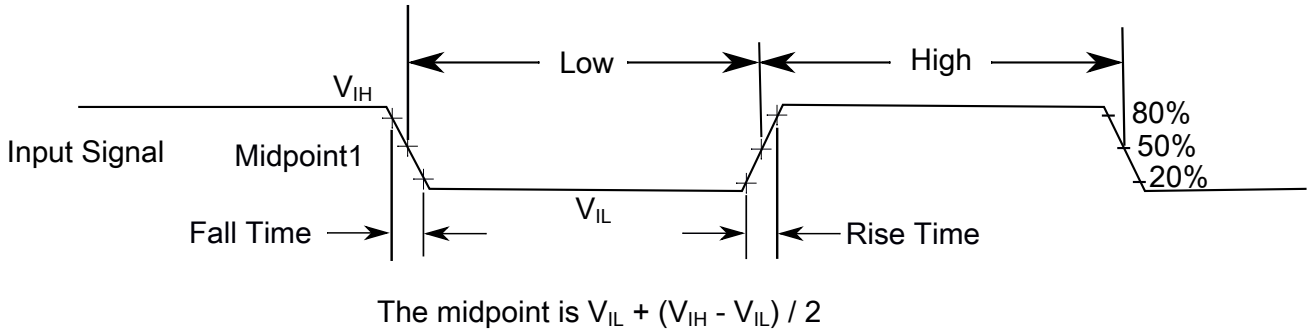



**Figure 1. Input signal measurement reference**

All digital I/O switching characteristics, unless otherwise specified, assume that the output pins have the following characteristics.

- $C_L$=30 pF loads
- Slew rate disabled
- Normal drive strength

**Table 8. Power mode transition operating behaviors (continued)**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| | • LLS → RUN | — | 7.5 | 8 | µs | |
| | • VLPS → RUN | — | 7.5 | 8 | µs | |
| | • STOP → RUN | — | 7.5 | 8 | µs | |

1. Normal boot (FTFA_FOPT[LPBOOT]=11)

## 2.2.5 Power consumption operating behaviors

The maximum values stated in the following table represent characterized results equivalent to the mean plus three times the standard deviation (mean + 3 sigma).

**NOTE**

The while (1) test is executed with flash cache enabled.

**Table 9. Power consumption operating behaviors**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $I_{DDA}$ | Analog supply current | — | — | See note | mA | 1 |
| $I_{DD\_RUNCO}$ | Running CoreMark in flash in compute operation mode—48M HIRC mode, 48 MHz core / 24 MHz flash, $V_{DD}$ = 3.0 V | | | | | 2 |
| | • at 25 °C | — | 5.76 | 6.40 | mA | |
| | • at 105 °C | — | 6.04 | 6.68 | | |
| $I_{DD\_RUNCO}$ | Running While(1) loop in flash in compute operation mode—48M HIRC mode, 48 MHz core / 24 MHz flash, $V_{DD}$ = 3.0 V | | | | | |
| | • at 25 °C | — | 3.21 | 3.85 | mA | |
| | • at 105 °C | — | 3.49 | 4.13 | | |
| $I_{DD\_RUN}$ | Run mode current—48M HIRC mode, running CoreMark in Flash all peripheral clock disable 48 MHz core/24 MHz flash, $V_{DD}$ = 3.0 V | | | | | 2 |
| | • at 25 °C | — | 6.45 | 7.09 | mA | |
| | • at 105 °C | — | 6.75 | 7.39 | | |
| $I_{DD\_RUN}$ | Run mode current—48M HIRC mode, running CoreMark in flash all peripheral clock disable, 24 MHz core/12 MHz flash, $V_{DD}$ = 3.0 V | | | | | 2 |
| | | — | 3.95 | 4.59 | | |
| | | — | 4.23 | 4.87 | mA | |

*Table continues on the next page...*

## Table 9. Power consumption operating behaviors (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| | disable, 125 kHz core / 31.25 kHz flash, $V_{DD}$ = 3.0 V<br>• at 25 °C | — | 50 | 131 | µA | |
| $I_{DD\_VLPR}$ | Very-low-power run mode current—2 MHz LIRC mode, While(1) loop in SRAM all peripheral clock enable, 2 MHz core / 0.5 MHz flash, $V_{DD}$ = 3.0 V<br>• at 25 °C | — | 208 | 289 | µA | |
| $I_{DD\_WAIT}$ | Wait mode current—core disabled, 48 MHz system/24 MHz bus, flash disabled (flash doze enabled), all peripheral clocks disabled, MCG_Lite under HIRC mode, $V_{DD}$ = 3.0 V | — | 1.81 | 1.89 | mA | |
| $I_{DD\_WAIT}$ | Wait mode current—core disabled, 24 MHz system/12 MHz bus, flash disabled (flash doze enabled), all peripheral clocks disabled, MCG_Lite under HIRC mode, $V_{DD}$ = 3.0 V | — | 1.22 | 1.39 | mA | |
| $I_{DD\_VLPW}$ | Very-low-power wait mode current, core disabled, 4 MHz system/ 1 MHz bus and flash, all peripheral clocks disabled, $V_{DD}$ = 3.0 V | — | 172 | 182 | µA | |
| $I_{DD\_VLPW}$ | Very-low-power wait mode current, core disabled, 2 MHz system/ 0.5 MHz bus and flash, all peripheral clocks disabled, $V_{DD}$ = 3.0 V | — | 69 | 76 | µA | |
| $I_{DD\_VLPW}$ | Very-low-power wait mode current, core disabled, 125 kHz system/ 31.25 kHz bus and flash, all peripheral clocks disabled, $V_{DD}$ = 3.0 V | — | 36 | 40 | µA | |
| $I_{DD\_PSTOP2}$ | Partial Stop 2, core and system clock disabled, 12 MHz bus and flash, $V_{DD}$ = 3.0 V | — | 1.81 | 2.06 | mA | |
| $I_{DD\_PSTOP2}$ | Partial Stop 2, core and system clock disabled, flash doze enabled, 12 MHz bus, $V_{DD}$ = 3.0 V | — | 1.00 | 1.25 | mA | |
| $I_{DD\_STOP}$ | Stop mode current at 3.0 V<br>• at 25 °C and below<br>• at 50 °C<br>• at 85 °C<br>• at 105 °C | —<br>—<br>—<br>— | 161.93<br>181.45<br>236.29<br>390.33 | 171.82<br>191.96<br>271.17<br>465.58 | µA | |
| $I_{DD\_VLPS}$ | Very-low-power stop mode current at 3.0 V<br>• at 25 °C and below<br>• at 50 °C<br>• at 85 °C<br>• at 105 °C | —<br>—<br>—<br>— | 3.31<br>10.43<br>34.14<br>104.38 | 5.14<br>17.68<br>61.06<br>164.44 | µA | |
| $I_{DD\_VLPS}$ | Very-low-power stop mode current at 1.8 V<br>• at 25 °C and below | — | 3.21 | 5.22 | | |

*Table continues on the next page...*

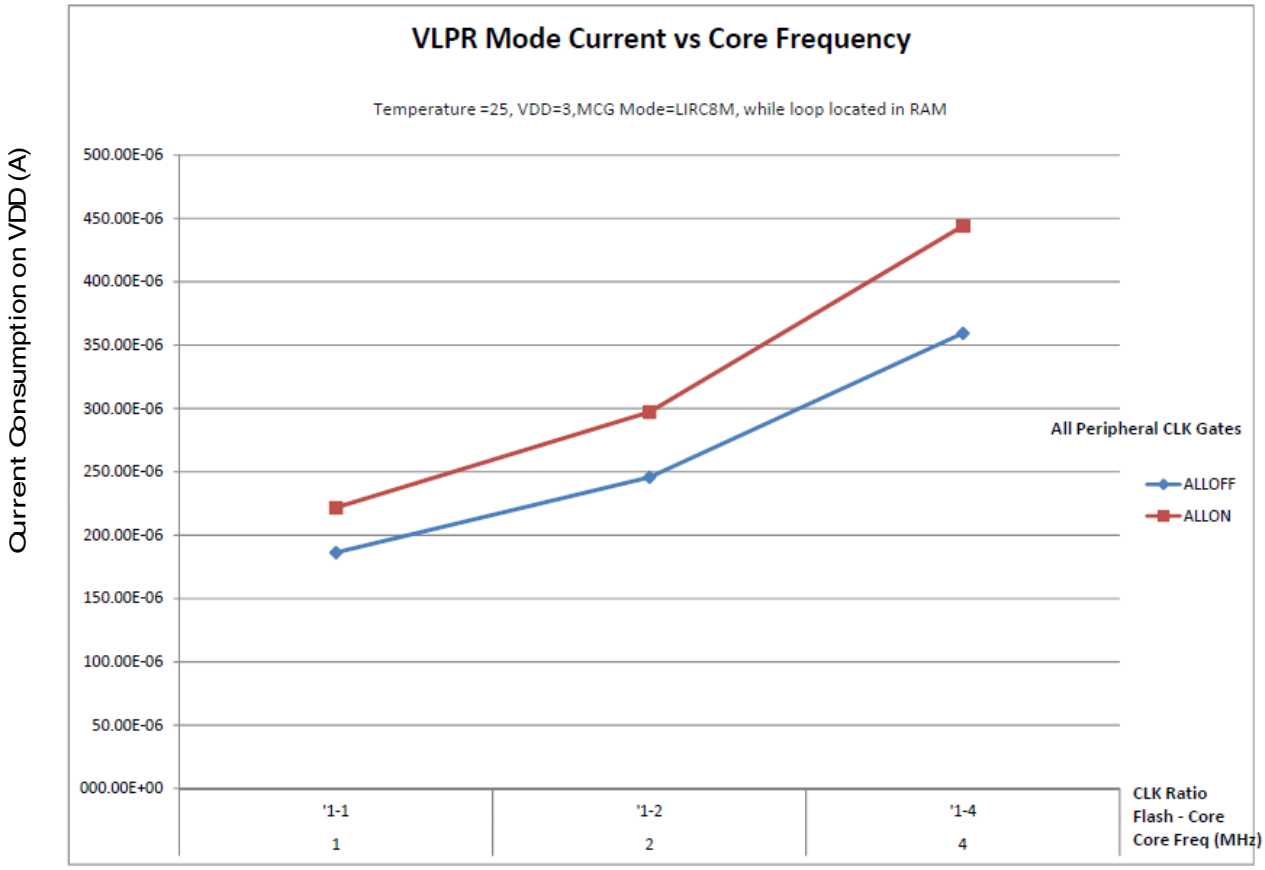



**Figure 3. VLPR mode current vs. core frequency**

## 2.2.6 EMC radiated emissions operating behaviors

**Table 11. EMC radiated emissions operating behaviors for 64-pin LQFP package**

| Symbol | Description | Frequency band (MHz) | Typ. | Unit | Notes |
|---|---|---|---|---|---|
| $V_{RE1}$ | Radiated emissions voltage, band 1 | 0.15–50 | 11 | dBµV | 1, 2 |
| $V_{RE2}$ | Radiated emissions voltage, band 2 | 50–150 | 12 | dBµV | |
| $V_{RE3}$ | Radiated emissions voltage, band 3 | 150–500 | 10 | dBµV | |
| $V_{RE4}$ | Radiated emissions voltage, band 4 | 500–1000 | 6 | dBµV | |
| $V_{RE\_IEC}$ | IEC level | 0.15–1000 | N | — | 2, 3 |

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions* and IEC Standard 61967-2, *Integrated Circuits - Measurement*

**Table 13. Device clock specifications (continued)**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $f_{LPTMR}$ | LPTMR clock[3] | — | 24 | MHz |
| $f_{LPTMR\_ERCLK}$ | LPTMR external reference clock | — | 16 | MHz |
| $f_{osc\_hi\_2}$ | Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x) | — | 16 | MHz |
| $f_{TPM}$ | TPM asynchronous clock | — | 8 | MHz |
| $f_{LPUART0/1}$ | LPUART0/1 asynchronous clock | — | 8 | MHz |

1. The maximum value of system clock, core clock, bus clock, and flash clock under normal run mode can be 3% higher than the specified maximum frequency when IRC 48MHz is used as the clock source.
2. The frequency limitations in VLPR and VLPS modes here override any frequency specification listed in the timing specification for any other module. These same frequency limits apply to VLPS, whether VLPS was entered from RUN or from VLPR.
3. The LPTMR can be clocked at this speed in VLPR or VLPS only when the source is an external pin.

## 2.3.2 General switching specifications

These general-purpose specifications apply to all signals configured for GPIO and UART signals.

**Table 14. General switching specifications**

| Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|
| GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path | 1.5 | — | Bus clock cycles | 1 |
| External RESET and NMI pin interrupt pulse width — Asynchronous path | 100 | — | ns | 2 |
| GPIO pin interrupt pulse width — Asynchronous path | 16 | — | ns | 2 |
| Port rise and fall time | — | 36 | ns | 3 |

1. The synchronous and asynchronous timing must be met.
2. This is the shortest pulse that is guaranteed to be recognized.
3. 75 pF load

# 2.4 Thermal specifications

4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.
5. Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

# 3 Peripheral operating requirements and behaviors

## 3.1 Core modules

### 3.1.1 SWD electricals

**Table 17. SWD full voltage range electricals**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| | Operating voltage | 1.71 | 3.6 | V |
| J1 | SWD_CLK frequency of operation<br>• Serial wire debug | 0 | 25 | MHz |
| J2 | SWD_CLK cycle period | 1/J1 | — | ns |
| J3 | SWD_CLK clock pulse width<br>• Serial wire debug | 20 | — | ns |
| J4 | SWD_CLK rise and fall times | — | 3 | ns |
| J9 | SWD_DIO input data setup time to SWD_CLK rise | 10 | — | ns |
| J10 | SWD_DIO input data hold time after SWD_CLK rise | 0 | — | ns |
| J11 | SWD_CLK high to SWD_DIO data valid | — | 32 | ns |
| J12 | SWD_CLK high to SWD_DIO high-Z | 5 | — | ns |

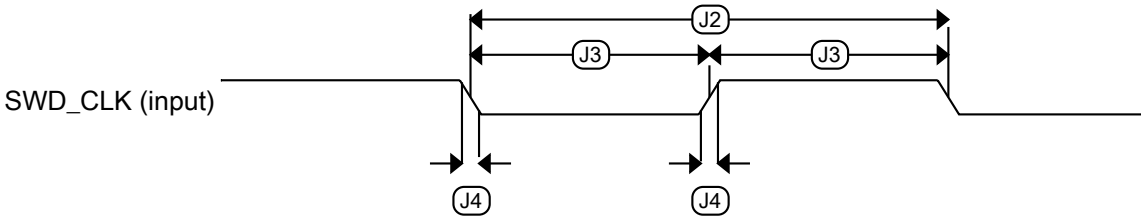



**Figure 4. Serial wire clock input timing**

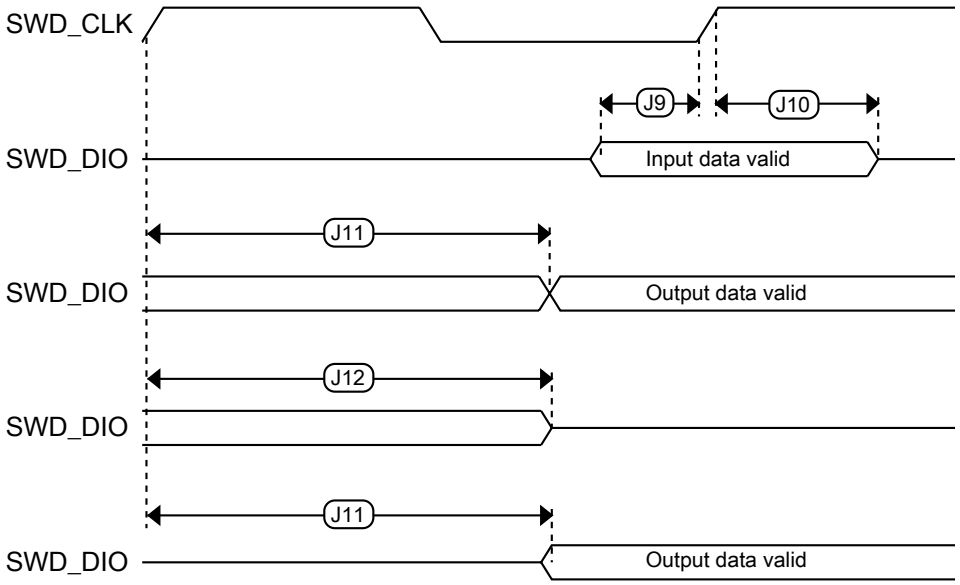



**Figure 5. Serial wire data timing**

## 3.2 System modules

There are no specifications necessary for the device's system modules.

## 3.3 Clock modules

### 3.3.1 MCG-Lite specifications

**Table 18. IRC48M specification**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $I_{DD}$ | Supply current | — | 400 | 500 | µA | — |
| $f_{IRC}$ | Output frequency | — | 48 | — | MHz | — |
| $\Delta f_{irc48m\_ol\_lv}$ | Open loop total deviation of IRC48M frequency at low voltage (VDD=1.71V-1.89V) over temperature | — | ± 0.5 | ± 1.5 | $\%f_{irc48m}$ | 1 |
| $\Delta f_{irc48m\_ol\_hv}$ | Open loop total deviation of IRC48M frequency at high voltage (VDD=1.89V-3.6V) over temperature | — | ± 0.5 | ± 1.0 | $\%f_{irc48m}$ | 1 |

*Table continues on the next page...*

## Table 18. IRC48M specification (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $T_j$ | Period jitter (RMS) | — | 35 | 150 | ps | — |
| $T_{su}$ | Startup time | — | 2 | 3 | µs | — |

1. The maximum value represents characterized results equivalent to mean plus or minus three times the standard deviation (mean +/-3sigma).

## Table 19. IRC8M/2M specification

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $I_{DD\_2M}$ | Supply current in 2 MHz mode | — | 14 | 17 | µA | — |
| $I_{DD\_8M}$ | Supply current in 8 MHz mode | — | 30 | 35 | µA | — |
| $f_{IRC\_2M}$ | Output frequency | — | 2 | — | MHz | — |
| $f_{IRC\_8M}$ | Output frequency | — | 8 | — | MHz | — |
| $f_{IRC\_T\_2M}$ | Output frequency range (trimmed) | — | — | ±3 | $\%f_{IRC}$ | — |
| $f_{IRC\_T\_8M}$ | Output frequency range (trimmed) | — | — | ±3 | $\%f_{IRC}$ | — |
| $T_{su\_2M}$ | Startup time | — | — | 12.5 | µs | — |
| $T_{su\_8M}$ | Startup time | — | — | 12.5 | µs | — |

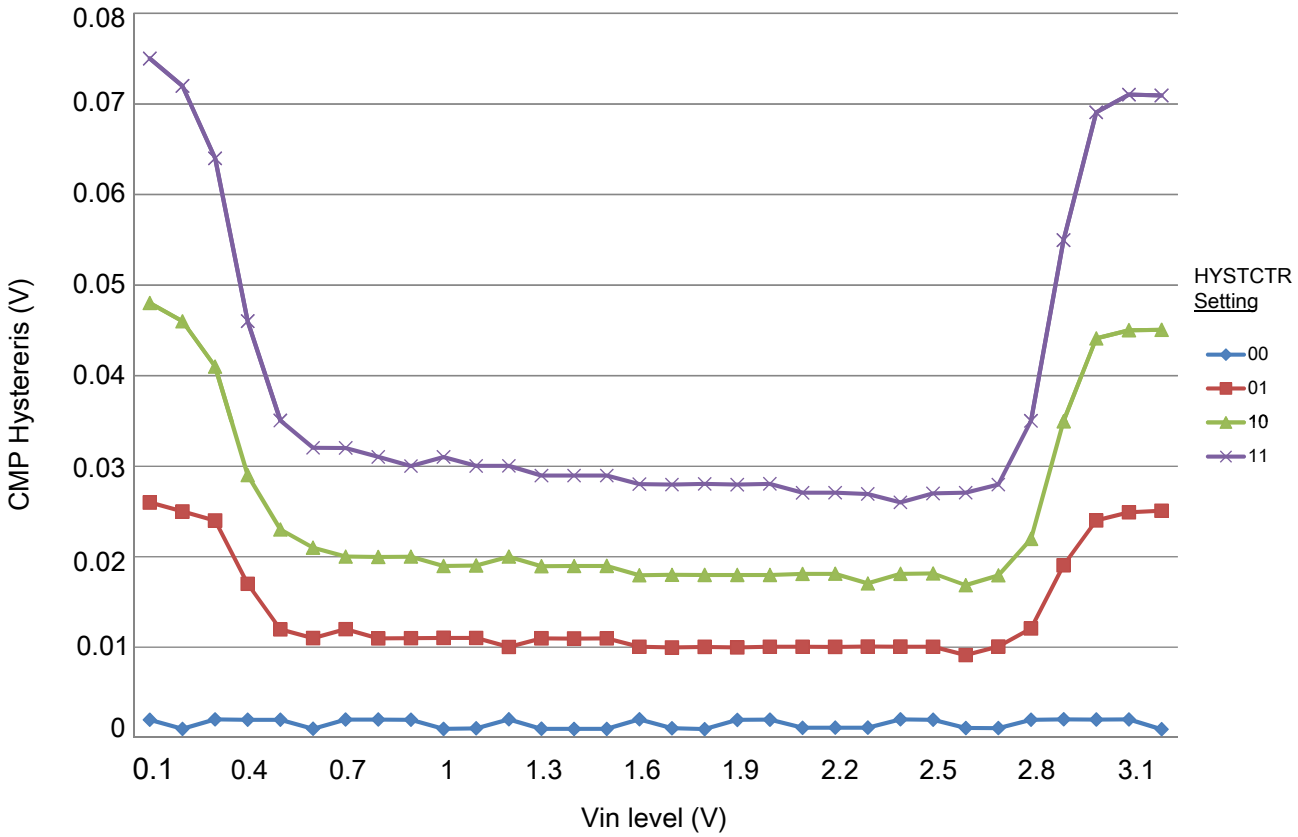



**Figure 10. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 0)**

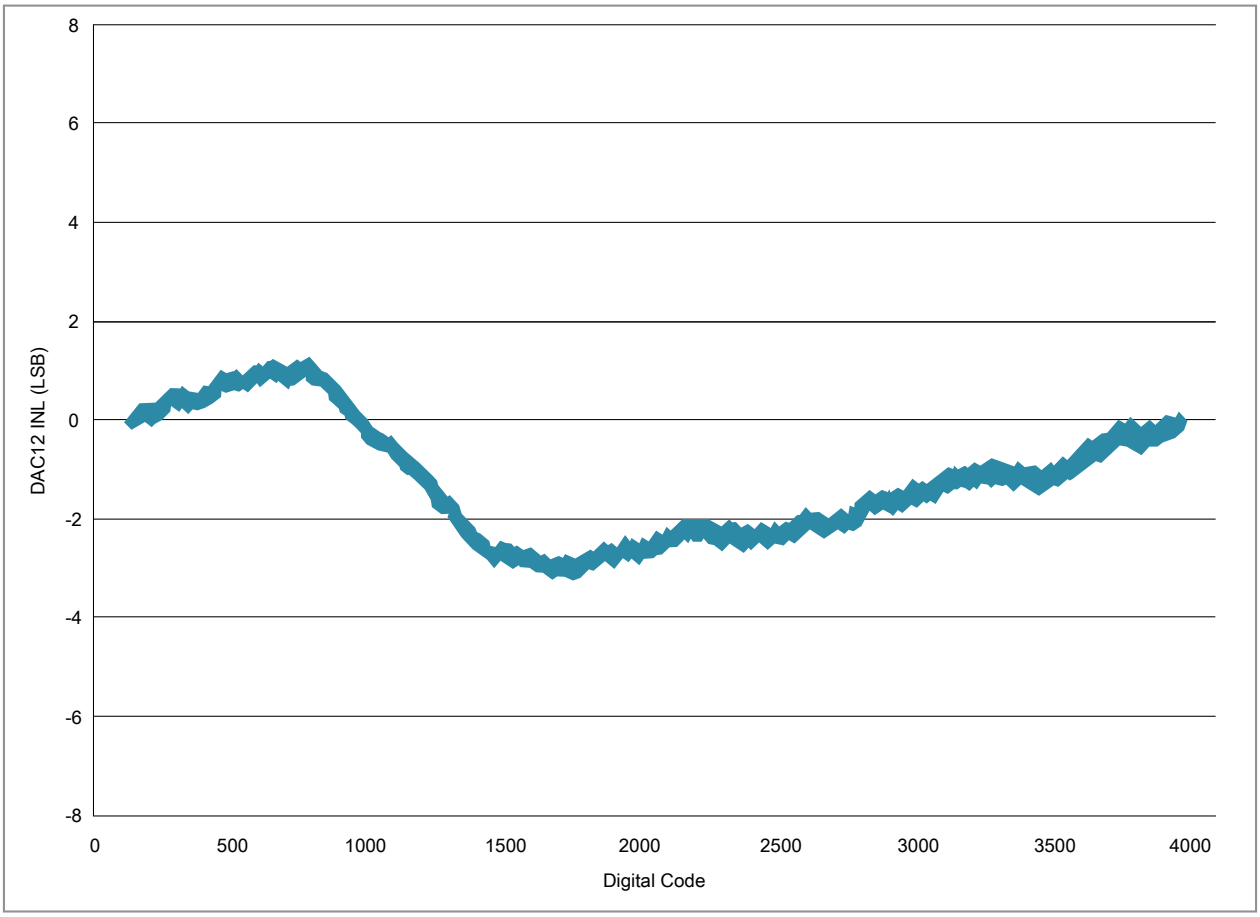



**Figure 12. Typical INL error vs. digital code**

**NOTE**

The IRC48M do not meet the USB jitter specifications for certification for Host mode operation.

This device cannot support Host mode operation.

## 3.8.2 USB VREG electrical specifications

**Table 35. USB VREG electrical specifications**

| Symbol | Description | Min. | Typ.[1] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| VREGIN | Input supply voltage | 2.7 | — | 5.5 | V | |
| $I_{DDon}$ | Quiescent current — Run mode, load current equal zero, input supply (VREGIN) > 3.6 V | — | 125 | 186 | µA | |
| $I_{DDstby}$ | Quiescent current — Standby mode, load current equal zero | — | 1.1 | 10 | µA | |
| $I_{DDoff}$ | Quiescent current — Shutdown mode<br>• VREGIN = 5.0 V and temperature=25 °C<br>• Across operating voltage and temperature | —<br>— | 650<br>— | —<br>4 | nA<br>µA | |
| $I_{LOADrun}$ | Maximum load current — Run mode | — | — | 120 | mA | |
| $I_{LOADstby}$ | Maximum load current — Standby mode | — | — | 1 | mA | |
| $V_{Reg33out}$ | Regulator output voltage — Input supply (VREGIN) > 3.6 V<br>• Run mode<br>• Standby mode | <br>3<br>2.1 | <br>3.3<br>2.8 | <br>3.6<br>3.6 | <br>V<br>V | |
| $V_{Reg33out}$ | Regulator output voltage — Input supply (VREGIN) < 3.6 V, pass-through mode | 2.1 | — | 3.6 | V | 2 |
| $C_{OUT}$ | External output capacitor | 1.76 | 2.2 | 8.16 | µF | |
| ESR | External output capacitor equivalent series resistance | 1 | — | 100 | mΩ | |
| $I_{LIM}$ | Short circuit current | — | 290 | — | mA | |

1. Typical values assume VREGIN = 5.0 V, Temp = 25 °C unless otherwise stated.
2. Operating in pass-through mode: regulator output voltage equal to the input voltage minus a drop proportional to $I_{Load}$.

### 3.8.3 SPI switching specifications

The Serial Peripheral Interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes. See the SPI chapter of the chip's Reference Manual for information about the modified transfer formats used for communicating with slower peripheral devices.

All timing is shown with respect to 20% $V_{DD}$ and 80% $V_{DD}$ thresholds, unless noted, as well as input signal transitions of 3 ns and a 30 pF maximum load on all SPI pins.

**Table 36. SPI master mode timing on slew rate disabled pads**

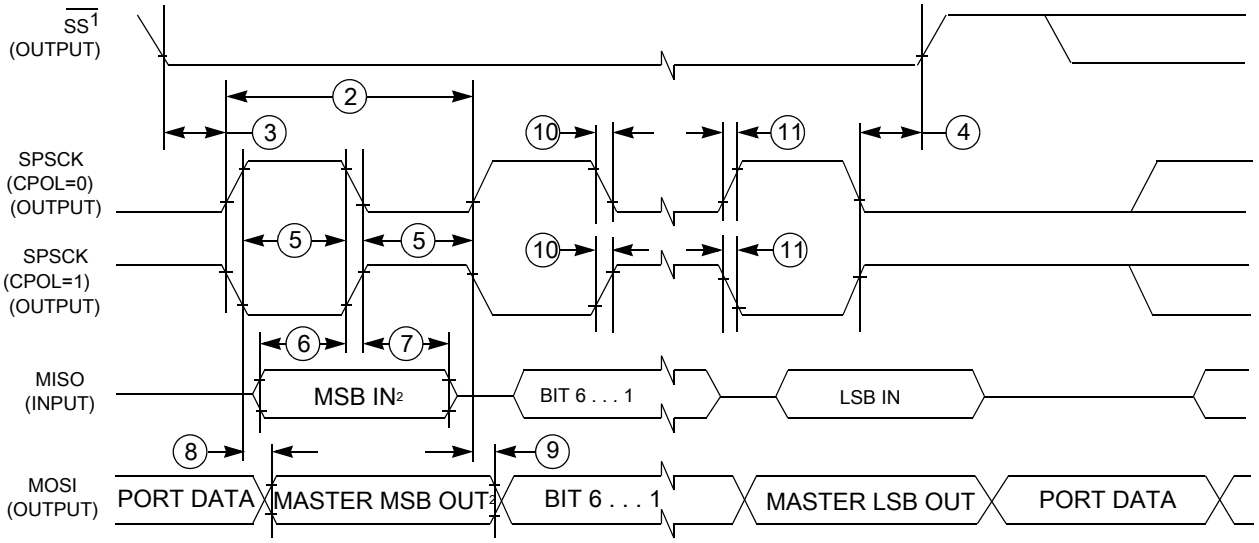
| Num. | Symbol | Description | Min. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| 1 | $f_{op}$ | Frequency of operation | $f_{periph}/2048$ | $f_{periph}/2$ | Hz | 1 |
| 2 | $t_{SPSCK}$ | SPSCK period | 2 x $t_{periph}$ | 2048 x $t_{periph}$ | ns | 2 |
| 3 | $t_{Lead}$ | Enable lead time | 1/2 | — | $t_{SPSCK}$ | — |
| 4 | $t_{Lag}$ | Enable lag time | 1/2 | — | $t_{SPSCK}$ | — |
| 5 | $t_{WSPSCK}$ | Clock (SPSCK) high or low time | $t_{periph}$ - 30 | 1024 x $t_{periph}$ | ns | — |
| 6 | $t_{SU}$ | Data setup time (inputs) | 18 | — | ns | — |
| 7 | $t_{HI}$ | Data hold time (inputs) | 0 | — | ns | — |
| 8 | $t_{v}$ | Data valid (after SPSCK edge) | — | 15 | ns | — |
| 9 | $t_{HO}$ | Data hold time (outputs) | 0 | — | ns | — |
| 10 | $t_{RI}$ | Rise time input | — | $t_{periph}$ - 25 | ns | — |
| | $t_{FI}$ | Fall time input | | | | |
| 11 | $t_{RO}$ | Rise time output | — | 25 | ns | — |
| | $t_{FO}$ | Fall time output | | | | |

1. For SPI0 $f_{periph}$ is the bus clock ($f_{BUS}$). For SPI1 $f_{periph}$ is the system clock ($f_{SYS}$).
2. $t_{periph} = 1/f_{periph}$

**Table 37. SPI master mode timing on slew rate enabled pads**

| Num. | Symbol | Description | Min. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| 1 | $f_{op}$ | Frequency of operation | $f_{periph}/2048$ | $f_{periph}/2$ | Hz | 1 |
| 2 | $t_{SPSCK}$ | SPSCK period | 2 x $t_{periph}$ | 2048 x $t_{periph}$ | ns | 2 |
| 3 | $t_{Lead}$ | Enable lead time | 1/2 | — | $t_{SPSCK}$ | — |
| 4 | $t_{Lag}$ | Enable lag time | 1/2 | — | $t_{SPSCK}$ | — |
| 5 | $t_{WSPSCK}$ | Clock (SPSCK) high or low time | $t_{periph}$ - 30 | 1024 x $t_{periph}$ | ns | — |
| 6 | $t_{SU}$ | Data setup time (inputs) | 96 | — | ns | — |
| 7 | $t_{HI}$ | Data hold time (inputs) | 0 | — | ns | — |

*Table continues on the next page...*




1.If configured as output

2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

**Figure 15. SPI master mode timing (CPHA = 1)**

## Table 38. SPI slave mode timing on slew rate disabled pads

| Num. | Symbol | Description | Min. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| 1 | $f_{op}$ | Frequency of operation | 0 | $f_{periph}/4$ | Hz | 1 |
| 2 | $t_{SPSCK}$ | SPSCK period | 4 x $t_{periph}$ | — | ns | 2 |
| 3 | $t_{Lead}$ | Enable lead time | 1 | — | $t_{periph}$ | — |
| 4 | $t_{Lag}$ | Enable lag time | 1 | — | $t_{periph}$ | — |
| 5 | $t_{WSPSCK}$ | Clock (SPSCK) high or low time | $t_{periph}$ - 30 | — | ns | — |
| 6 | $t_{SU}$ | Data setup time (inputs) | 2.5 | — | ns | — |
| 7 | $t_{HI}$ | Data hold time (inputs) | 3.5 | — | ns | — |
| 8 | $t_a$ | Slave access time | — | $t_{periph}$ | ns | 3 |
| 9 | $t_{dis}$ | Slave MISO disable time | — | $t_{periph}$ | ns | 4 |
| 10 | $t_v$ | Data valid (after SPSCK edge) | — | 31 | ns | — |
| 11 | $t_{HO}$ | Data hold time (outputs) | 0 | — | ns | — |
| 12 | $t_{RI}$ | Rise time input | — | $t_{periph}$ - 25 | ns | — |
| | $t_{FI}$ | Fall time input | | | | |
| 13 | $t_{RO}$ | Rise time output | — | 25 | ns | — |
| | $t_{FO}$ | Fall time output | | | | |

1. For SPI0 $f_{periph}$ is the bus clock ($f_{BUS}$). For SPI1 $f_{periph}$ is the system clock ($f_{SYS}$).
2. $t_{periph} = 1/f_{periph}$
3. Time to data active from high-impedance state
4. Hold time to high-impedance state

**Table 42. I2S/SAI master mode timing (continued)**

| Num. | Characteristic | Min. | Max. | Unit |
|---|---|---|---|---|
| S6 | I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid | 0 | — | ns |
| S7 | I2S_TX_BCLK to I2S_TXD valid | — | 19 | ns |
| S8 | I2S_TX_BCLK to I2S_TXD invalid | 0 | — | ns |
| S9 | I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK | 26 | — | ns |
| S10 | I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK | 0 | — | ns |

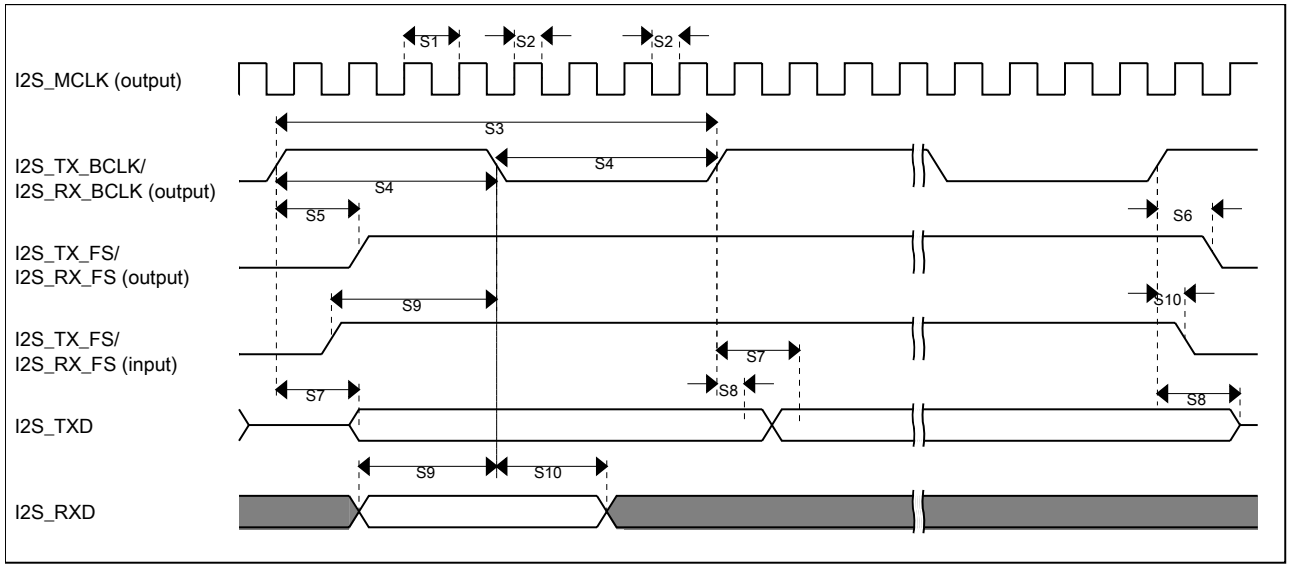



**Figure 19. I2S/SAI timing — master modes**

**Table 43. I2S/SAI slave mode timing**

| Num. | Characteristic | Min. | Max. | Unit |
|---|---|---|---|---|
| | Operating voltage | 1.71 | 3.6 | V |
| S11 | I2S_TX_BCLK/I2S_RX_BCLK cycle time (input) | 80 | — | ns |
| S12 | I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input) | 45% | 55% | MCLK period |
| S13 | I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK | 10 | — | ns |
| S14 | I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK | 2 | — | ns |
| S15 | I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid | — | 33 | ns |
| S16 | I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid | 0 | — | ns |
| S17 | I2S_RXD setup before I2S_RX_BCLK | 10 | — | ns |

*Table continues on the next page...*

| 32 QFN | 48 QFN | 64 MAP BGA | 64 LQFP | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 17 | 24 | H8 | 32 | PTA18 | EXTAL0 | EXTAL0 | PTA18 | | LPUART1_ RX | TPM_ CLKIN0 | | | |
| 18 | 25 | G8 | 33 | PTA19 | XTAL0 | XTAL0 | PTA19 | | LPUART1_ TX | TPM_ CLKIN1 | | LPTMR0_ ALT1 | |
| 19 | 26 | F8 | 34 | PTA20 | RESET_b | | PTA20 | | | | | | RESET_b |
| 20 | 27 | F7 | 35 | PTB0/ LLWU_P5 | ADC0_SE8 | ADC0_SE8 | PTB0/ LLWU_P5 | I2C0_SCL | TPM1_CH0 | | | | |
| 21 | 28 | F6 | 36 | PTB1 | ADC0_SE9 | ADC0_SE9 | PTB1 | I2C0_SDA | TPM1_CH1 | | | | |
| 22 | 34 | C6 | 44 | PTC1/ LLWU_P6/ RTC_CLKIN | ADC0_SE15 | ADC0_SE15 | PTC1/ LLWU_P6/ RTC_CLKIN | I2C1_SCL | | TPM0_CH0 | | I2S0_TXD0 | |
| 23 | 35 | B7 | 45 | PTC2 | ADC0_SE11 | ADC0_SE11 | PTC2 | I2C1_SDA | | TPM0_CH1 | | I2S0_TX_FS | |
| 24 | 36 | C8 | 46 | PTC3/ LLWU_P7 | DISABLED | | PTC3/ LLWU_P7 | SPI1_SCK | LPUART1_ RX | TPM0_CH2 | CLKOUT | I2S0_TX_ BCLK | |
| 25 | 37 | B8 | 49 | PTC4/ LLWU_P8 | DISABLED | | PTC4/ LLWU_P8 | SPI0_SS | LPUART1_ TX | TPM0_CH3 | I2S0_MCLK | | |
| 26 | 38 | A8 | 50 | PTC5/ LLWU_P9 | DISABLED | | PTC5/ LLWU_P9 | SPI0_SCK | LPTMR0_ ALT2 | I2S0_RXD0 | | CMP0_OUT | |
| 27 | 39 | A7 | 51 | PTC6/ LLWU_P10 | CMP0_IN0 | CMP0_IN0 | PTC6/ LLWU_P10 | SPI0_MOSI | EXTRG_IN | I2S0_RX_ BCLK | SPI0_MISO | I2S0_MCLK | |
| 28 | 40 | B6 | 52 | PTC7 | CMP0_IN1 | CMP0_IN1 | PTC7 | SPI0_MISO | audioUSB_ SOF_OUT | I2S0_RX_FS | SPI0_MOSI | | |
| 29 | 45 | A3 | 61 | PTD4/ LLWU_P14 | DISABLED | | PTD4/ LLWU_P14 | SPI1_SS | UART2_RX | TPM0_CH4 | | FXIO0_D4 | |
| 30 | 46 | C1 | 62 | PTD5 | ADC0_SE6b | ADC0_SE6b | PTD5 | SPI1_SCK | UART2_TX | TPM0_CH5 | | FXIO0_D5 | |
| 31 | 47 | B2 | 63 | PTD6/ LLWU_P15 | ADC0_SE7b | ADC0_SE7b | PTD6/ LLWU_P15 | SPI1_MOSI | LPUART0_ RX | | SPI1_MISO | FXIO0_D6 | |
| 32 | 48 | A2 | 64 | PTD7 | DISABLED | | PTD7 | SPI1_MISO | LPUART0_ TX | | SPI1_MOSI | FXIO0_D7 | |

## 5.2 KL27 Family Pinouts

Figure below shows the 32 QFN pinouts:

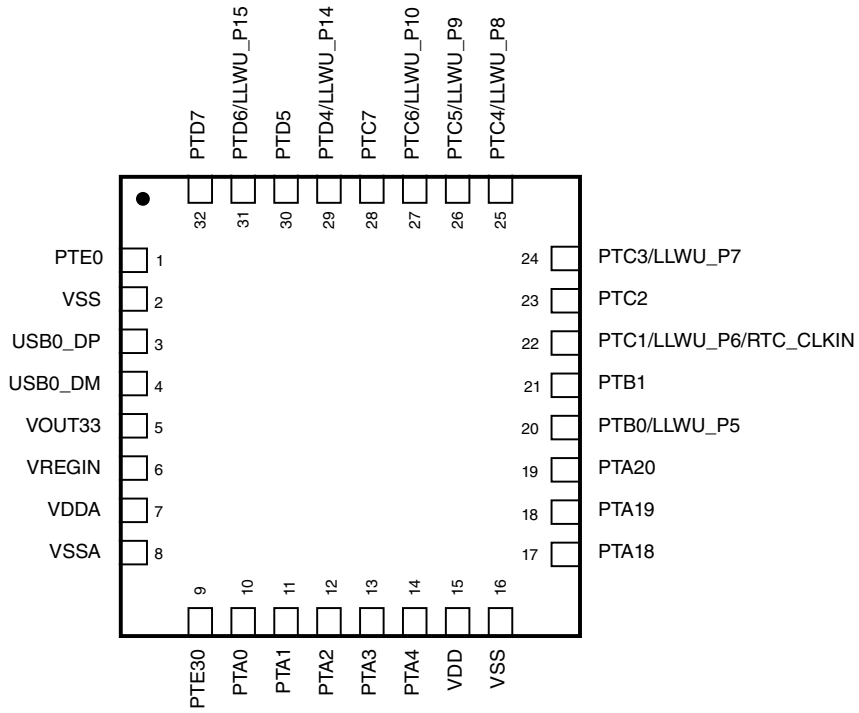



**Figure 23. 32 QFN Pinout diagram**

Figure below shows the 48 QFN pinouts:

## 7.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

## 7.2 Format

Part numbers for this device have the following format:

Q KL## A FFF R T PP CC N

## 7.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

**Table 46. Part number fields descriptions**

| Field | Description | Values |
|---|---|---|
| Q | Qualification status | • M = Fully qualified, general market flow<br>• P = Prequalification |
| KL## | Kinetis family | • KL27 |
| A | Key attribute | • Z = Cortex-M0+ |
| FFF | Program flash memory size | |
| R | Silicon revision | • (Blank) = Main<br>• A = Revision after main |
| T | Temperature range (°C) | • V = –40 to 105 |
| PP | Package identifier | • FM = 32 QFN (5 mm x 5 mm)<br>• FT = 48 QFN (7 mm x 7 mm)<br>• LH = 64 LQFP (10 mm x 10 mm)<br>• MP = 64 MAPBGA (5 mm x 5 mm) |
| CC | Maximum CPU frequency (MHz) | • 4 = 48 MHz |
| N | Packaging type | • R = Tape and reel |

## 7.4 Example

This is an example part number:

MKL27Z256VFT4

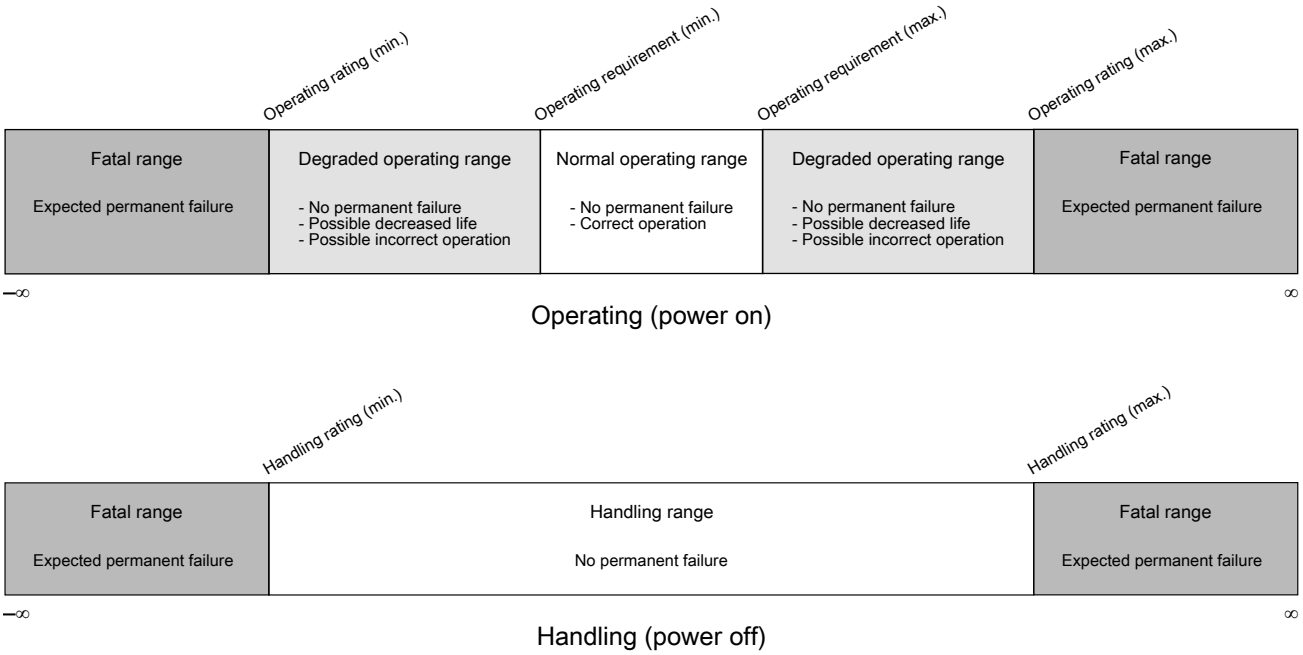
# 8 Terminology and guidelines

## 8.1 Definitions

Key terms are defined in the following table:

| Term | Definition |
|---|---|
| Rating | A minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:<br>• *Operating ratings* apply during operation of the chip.<br>• *Handling ratings* apply when the chip is not powered.<br>**NOTE:** The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings. |
| Operating requirement | A specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip |
| Operating behavior | A specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions |
| Typical value | A specified value for a technical characteristic that:<br>• Lies within the range of values specified by the operating behavior<br>• Is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions<br>**NOTE:** Typical values are provided as design guidelines and are neither tested nor guaranteed. |

## 8.4 Relationship between ratings and operating requirements




## 8.5 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

# 9 Revision History

The following table provides a revision history for this document.

**Table 47. Revision History**

| Rev. No. | Date | Substantial Changes |
|---|---|---|
| 3 | 09 August 2014 | Initial Public release<br>• Updated Table 9 - Power consumption operating behaviors.<br>• Added a note related to 32 QFN pin package in Pinouts topic. |
| 4 | 03 March 2015 | • Updated the features and completed the ordering information.<br>• Removed thickness dimension from package diagrams. |

*Table continues on the next page...*