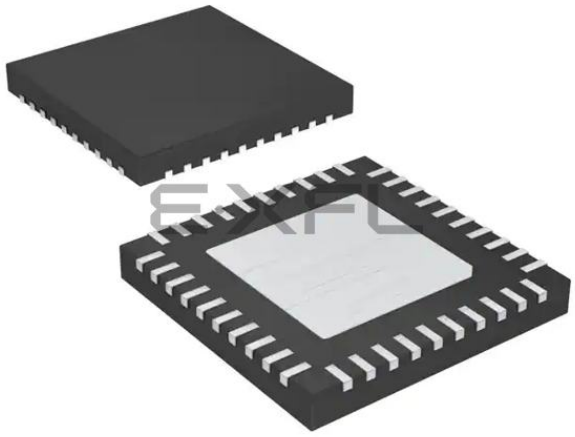
Renesas Electronics America Inc - R5F213M6QNNP#U0 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	R8C
Core Size	16-Bit
Speed	16MHz
Connectivity	I²C, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	18
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	2.5K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-WFQFN Exposed Pad
Supplier Device Package	40-HWQFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f213m6qnnp-u0

Table 1.2 Specifications for R8C/3MQ Group (2)

Item	Function	Specification
Serial Interface (UART0)		Shared with clock synchronous serial I/O mode and clock asynchronous serial I/O
Synchronous Serial Communication Unit (SSU)		1 (shared with I²C bus)
I²C bus		1 (shared with SSU)
RF	RF frequency	2405 MHz to 2480 MHz
	Reception sensitivity	-95 dBm
	Transmission output level	0 dBm
Baseband		• 127-byte transmit RAM, 127-byte receive RAM × 2 • Automatic ACK response function • 26-bit timer: Compare function in 3 channels
Encryption	AES	AES Encryption/Decryption (Key length 128bits)
Flash Memory		• Programming and erasure voltage: VCC = 1.8 to 3.6 V (in CPU rewrite mode) • Programming and erasure endurance: 10,000 times (data flash) 1,000 times (program ROM) • Program security: ROM code protect, ID code check • Debug functions: On-chip debug, on-board flash rewrite function • Background operation (BGO) function
Operating Frequency/ Supply Voltage (in single mode)		f(BCLK) = 16 MHz, VCC = 2.7 to 3.6 V) f(BCLK) = 8 MHz (VCC = 2.15 to 3.6V) f(BCLK) = 4 MHz, VCC = 1.8 to 3.6 V) Note: f(XIN) = fixed at 16 MHz

Table 1.3 Specifications for R8C/3MQ Group (3)

Item	Function	Specification
Current Consumption (1)		RF = Tx: 18 mA RF = Rx (reception in progress): 25 mA RF = Rx (reception standby): 24 mA RF = Rx (reception standby)/wait mode: 23 mA RF = idle: 4 mA RF = off: 2.5 mA *The above applies when: f(XIN) = 16 MHz, f(BCLK)= 4 MHz, and VCC = VCCRF = 1.8 to 3.6 V
		RF = Tx: 19 mA RF = Rx (reception in progress): 26 mA RF = Rx (reception standby): 25 mA RF = Rx (reception standby)/wait mode: 23 mA RF = idle: 5 mA RF = off: 3.5 mA *The above applies when: f(XIN) = 16 MHz, f(BLCK) = 8 MHz, and VCC = VCCRF = 2.15 to 3.6 V
		RF = Tx: 21.5 mA RF = Rx (reception in progress): 28.5 mA RF = Rx (reception standby): 27.5 mA RF = Rx (reception standby)/wait mode: 23 mA RF = idle: 7.5 mA RF = off: 6 mA *The above applies when: f(XIN) = 16 MHz, f(BLCK) = 16 MHz, and VCC = VCCRF = 2.7 to 3.6 V
		Low-speed on-chip oscillator mode (f(BCLK) = 15.6 kHz): 80 μA Low-speed clock mode (f(BCLK) = 32 kHz, flash memory low-power-consumption mode): 95 μA Low-speed clock mode (f(BCLK) = 32 kHz, flash memory off/program operation on RAM: 45 μA Wait mode (system clock = XCIN (32 kHz)), peripheral function clock on: 6 μA Wait mode (system clock = XCIN (32 kHz)), peripheral function clock off: 4.5 μA Wait mode (system clock = fOCO-S (125 kHz)), peripheral function clock on: 13 μA Wait mode (system clock = fOCO-S (125 kHz)), peripheral function clock off: 7.5 μA Stop mode (all clocks off): 2 μA *When VCC = VCCRF = 1.8 to 3.6 V and RF = off
Operating Ambient Temperature		–20°C to 85°C (N version)
Package		40-pin HWQFN Package code: PWQN0040KB-A (previous code: 40PJS-A)

Note:
1. Refer to **5. Electrical Characteristics** for details on the measurement conditions.

1.2 Product List

Table 1.4 lists Product List for R8C/3MQ Group. Figure 1.1 shows a Part Number, Memory Size, and Package of R8C/3MQ Group.

Table 1.4 Product List for R8C/3MQ Group **Current of Jun 2012**

Part No.	ROM Capacity		RAM Capacity	Package Type	Remarks
	Program ROM	Data flash			
R5F213M6QNNP	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PWQN0040KB-A	N version
R5F213M7QNNP	48 Kbytes	1 Kbyte × 4	4 Kbytes		
R5F213M8QNNP	64 Kbytes	1 Kbyte × 4	6 Kbytes		
R5F213MAQNNP	96 Kbytes	1 Kbyte × 4	7 Kbytes		
R5F213MCQNNP	112 Kbytes	1 Kbyte × 4	7.5 Kbytes		

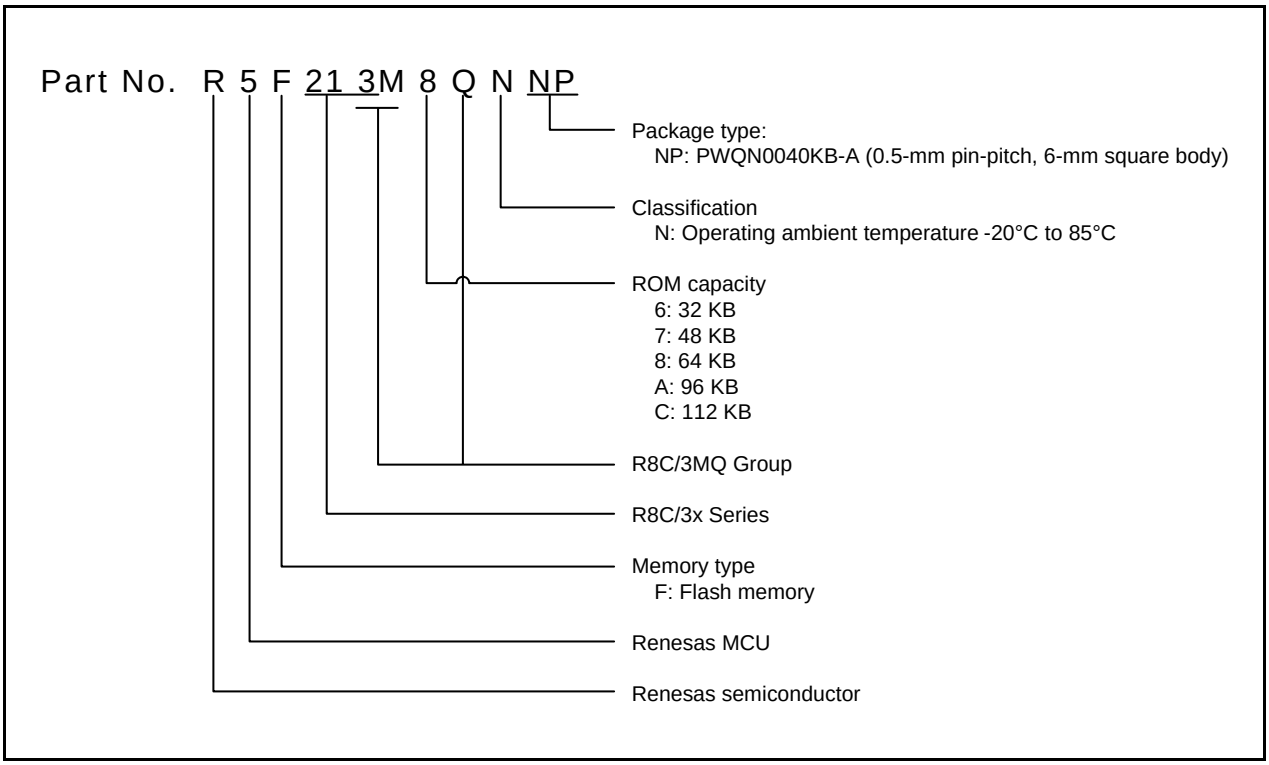
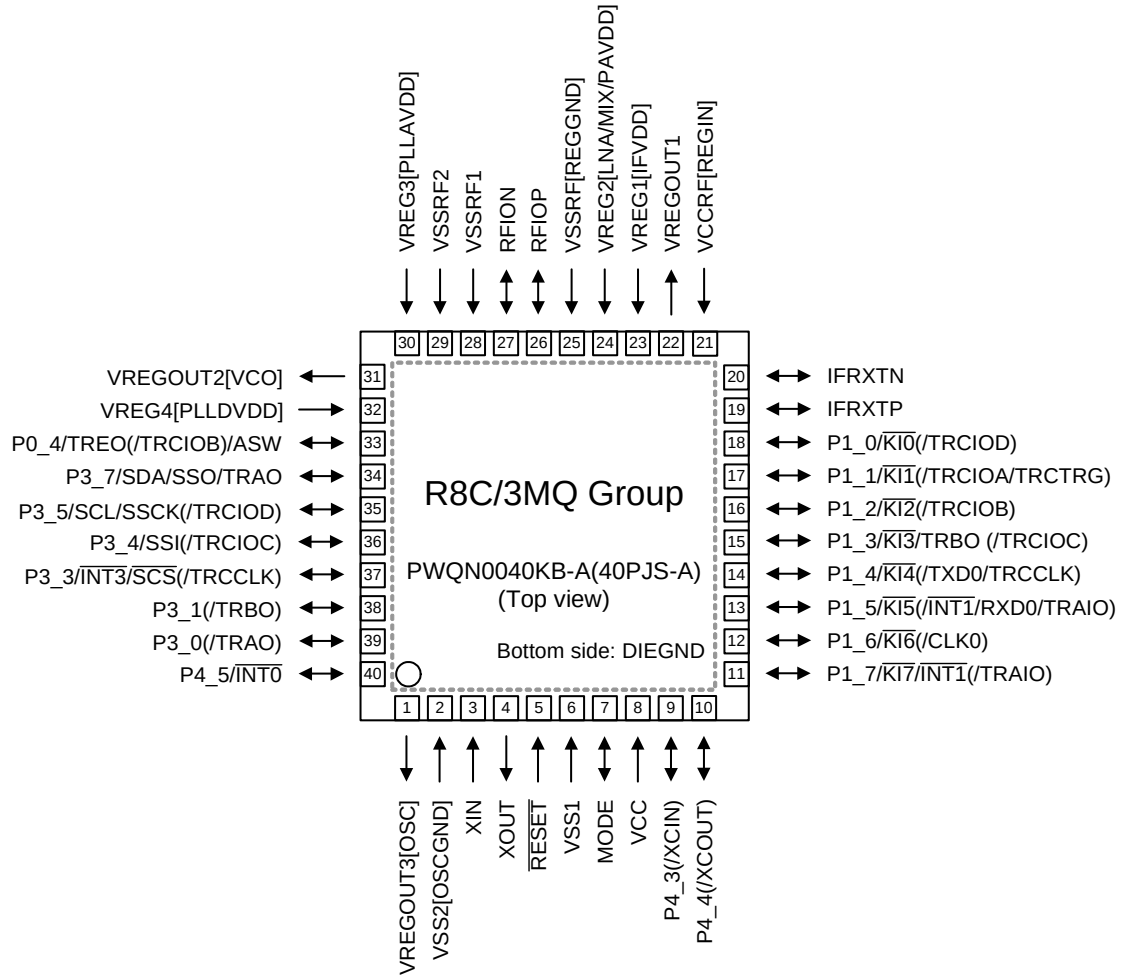


Figure 1.1 Part Number, Memory Size, and Package of R8C/3MQ Group

1.4 Pin Assignment

Figure 1.3 shows Pin Assignment (Top View). Table 1.5 outlines Pin Name Information by Pin Number.



Notes:
1. The function in parentheses can be assigned to the pin by a program.
2. [ ] indicates the internal function name related to the pin.
3. Confirm the pin 1 position on the package by referring to the package dimensions.
4. Connect the metal pad (DIEGND) of the package's bottom side to the board's GND side.

Figure 1.3 Pin Assignment (Top View)

Table 1.5 Pin Name Information by Pin Number

Pin Number	Control Pin	Port	I/O Pin Functions for Peripheral Modules					
			Interrupt	Timer	Serial Interface	SSU	I^2C bus	RF Pin Other
1	VREGOUT3							
2	VSS2							
3	XIN							
4	XOUT							
5	$\overline{\text{RESET}}$							
6	VSS1							
7	MODE							
8	VCC							
9	(XCIN)	P4_3						
10	(XCOUT)	P4_4						
11		P1_7	$\overline{\text{KI7}}$/$\overline{\text{INT1}}$	(TRAIO)				
12		P1_6	$\overline{\text{KI6}}$		(CLK0)			
13		P1_5	$\overline{\text{KI5}}$(/$\overline{\text{INT1}}$)	(TRAIO)	(RXD0)			
14		P1_4	$\overline{\text{KI4}}$	(TRCCLK)	(TXD0)			
15		P1_3	$\overline{\text{KI3}}$	TRBO(/TRCIOC)				
16		P1_2	$\overline{\text{KI2}}$	(TRCIOB)				
17		P1_1	$\overline{\text{KI1}}$	(TRCIOA/TRCTRG)				
18		P1_0	$\overline{\text{KI0}}$	(TRCIOD)				
19								IFRXTP
20								IFRXTN
21	VCCRF							
22	VREGOUT1							
23	VREG1							
24	VREG2							
25	VSSRF							
26								RFIOP
27								RFION
28	VSSRF1							
29	VSSRF2							
30	VREG3							
31	VREGOUT2							
32	VREG4							
33		P0_4		TREO(/TRCIOB)				ASW
34		P3_7		TRAO		SSO	SDA	
35		P3_5		(TRCIOD)		SSCK	SCL	
36		P3_4		(TRCIOC)		SSI		
37		P3_3	$\overline{\text{INT3}}$	(TRCCLK)		$\overline{\text{SCS}}$		
38		P3_1		(TRBO)				
39		P3_0		(TRAO)				
40		P4_5	$\overline{\text{INT0}}$					
Bottom side	DIEGND							

Note:
1. The function in parentheses can be assigned to the pin by a program.

1.5 Pin Functions

Tables 1.6 and 1.7 list Pin Functions.

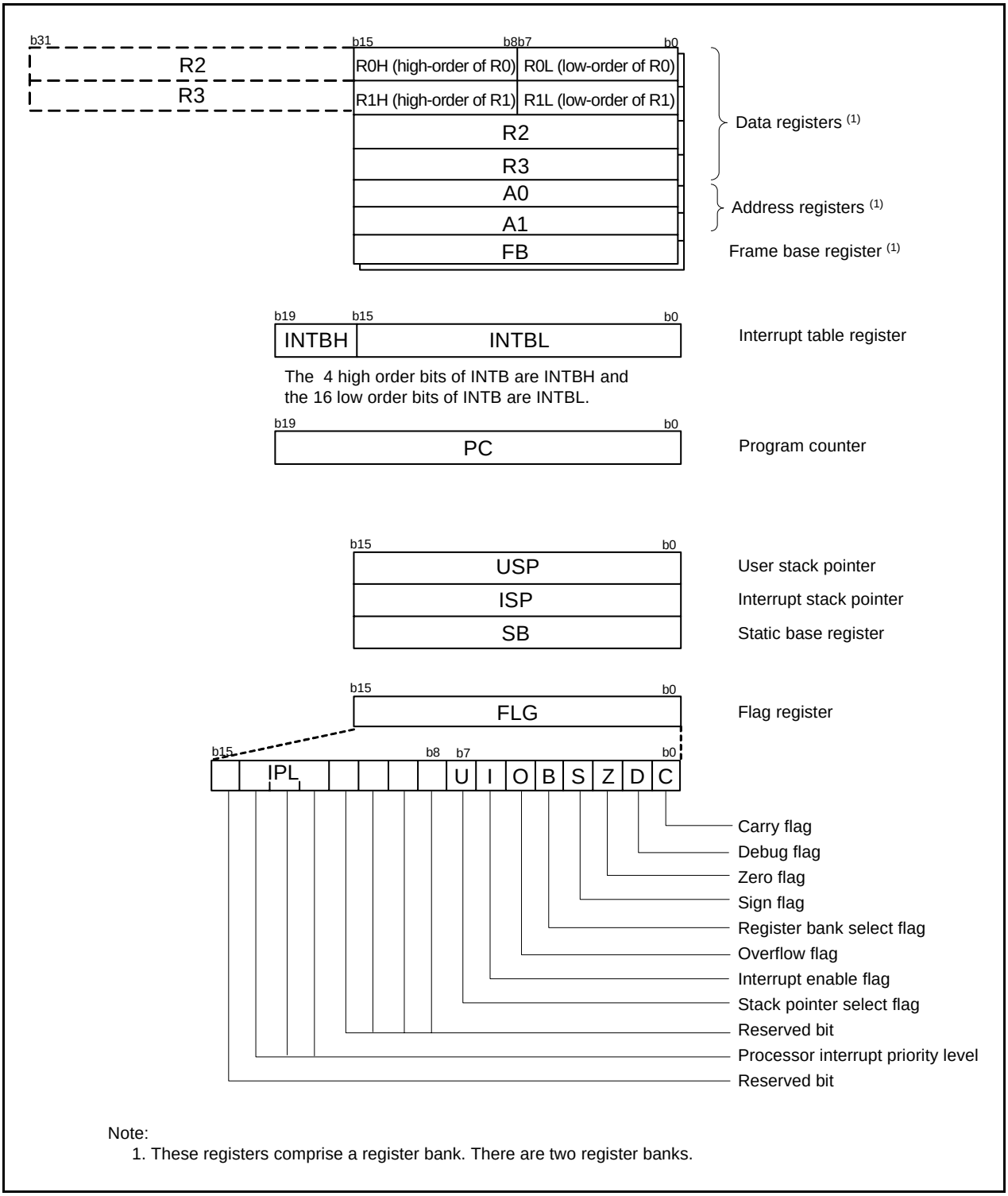
Table 1.6 Pin Functions (1)

Item	Pin Name	I/O Type	Description
Power supply input	VCC, VSS1	—	Apply 1.8 to 3.6 V to the VCC pin. Apply 0 V to the VSS1 pin.
Reset input	$\overline{\text{RESET}}$	I	Input “L” on this pin resets the MCU.
MODE	MODE	I	Connect this pin to VCC via a resistor.
XIN clock input	XIN	I	These pins are provided for XIN clock oscillation circuit I/O. Connect a crystal oscillator between the XIN and XOUT pins.
XIN clock output	XOUT	I/O	
XCIN clock input	XCIN	I	These pins are provided for XCIN clock oscillation circuit I/O. Connect a crystal oscillator between the XCIN and XCOUT pins.
XCIN clock output	XCOUT	O	
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$, $\overline{\text{INT1}}$, $\overline{\text{INT3}}$	I	$\overline{\text{INT}}$ interrupt input pins. $\overline{\text{INT0}}$ is used as an input pin for timer RB and timer RC.
Key input interrupt input	$\overline{\text{KI0}}$ to $\overline{\text{KI7}}$	I	Key input interrupt input pins.
Timer RA	TRAIO	I/O	Timer RA I/O pin.
	TRAO	O	Timer RA output pin.
Timer RB	TRBO	O	Timer RB output pin.
Timer RC	TRCCLK	I	External clock input pin.
	TRCTRG	I	External trigger input pin.
	TRCIOA, TRCIOB, TRCIOC, TRCIOD	I/O	Timer RC I/O pins.
Timer RE	TREO	O	Divided clock output pin.
Serial interface	CLK0	I/O	Transfer clock I/O pin.
	RXD0	I	Serial data input pin.
	TXD0	O	Serial data output pin.
SSU	SSI	I/O	Data I/O pin.
	$\overline{\text{SCS}}$	I/O	Chip-select signal I/O pin.
	SSCK	I/O	Clock I/O pin.
	SSO	I/O	Data I/O pin.
I^2C bus	SCL	I/O	Clock I/O pin
	SDA	I/O	Data I/O pin
I/O ports	P0_4, P1_0 to P1_7, P3_0, P3_1, P3_3 to P3_5, P3_7, P4_3 to P4_5	I/O	CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program.

I: Input O: Output I/O: Input and output

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register bank.



Note:
1. These registers comprise a register bank. There are two register banks.

Figure 2.1 CPU Registers

2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.
Interrupts are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.
The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has higher priority than IPL, the interrupt is enabled.

2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.11 list the special function registers. Table 4.12 lists the ID Code Areas and Option Function Select Area.

Table 4.1 SFR Information (1) (0000h to 002Fh) (1)

Address	Register	Symbol	After Reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	00101000b
0007h	System Clock Control Register 1	CM1	00101000b
0008h	Module Standby Control Register	MSTCR	00h
0009h	System Clock Control Register 3	CM3	00h
000Ah	Protect Register	PRCR	00h
000Bh	Reset Source Determination Register	RSTFR	0XXXXXXXb (2)
000Ch	Oscillation Stop Detection Register	OCD	00000100b
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDTC	00111111b
0010h			
0011h			
0012h			
0013h			
0014h			
0015h			
0016h			
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	00h 10000000b (3)
001Dh			
001Eh			
001Fh			
0020h			
0021h			
0022h			
0023h			
0024h			
0025h			
0026h			
0027h			
0028h	Clock Prescaler Reset Flag	CPSRF	00h
0029h			
002Ah			
002Bh			
002Ch			
002Dh			
002Eh			
002Fh			

X: Undefined

Notes:

1. The blank areas are reserved and cannot be accessed by users.
2. The CWR bit in the RSTFR register is set to 0 after power-on and voltage monitor 0 reset. Hardware reset, software reset, or watchdog timer reset does not affect this bit.
3. The CSPROINI bit in the OFS register is set to 0.

Table 4.5 SFR Information (5) (0120h to 019Fh) (1)

Address	Register	Symbol	After Reset
0120h	Timer RC Mode Register	TRCMR	01001000b
0121h	Timer RC Control Register 1	TRCCR1	00h
0122h	Timer RC Interrupt Enable Register	TRCIER	01110000b
0123h	Timer RC Status Register	TRCSR	01110000b
0124h	Timer RC I/O Control Register 0	TRCIOR0	10001000b
0125h	Timer RC I/O Control Register 1	TRCIOR1	10001000b
0126h	Timer RC Counter	TRC	00h
0127h			00h
0128h	Timer RC General Register A	TRCGRA	FFh
0129h			FFh
012Ah	Timer RC General Register B	TRCGRB	FFh
012Bh			FFh
012Ch	Timer RC General Register C	TRCGRC	FFh
012Dh			FFh
012Eh	Timer RC General Register D	TRCGRD	FFh
012Fh			FFh
0130h	Timer RC Control Register 2	TRCCR2	00011000b
0131h	Timer RC Digital Filter Function Select Register	TRCDF	00h
0132h	Timer RC Output Master Enable Register	TRCOER	01111111b
0133h			
0134h			
0135h			
0136h			
0137h			
0138h			
0139h			
013Ah			
013Bh			
013Ch			
013Dh			
013Eh			
013Fh			
:			
0180h	Timer RA Pin Select Register	TRASR	00h
0181h	Timer RB/RC Pin Select Register	TRBRCSR	00h
0182h	Timer RC Pin Select Register 0	TRCPSR0	00h
0183h	Timer RC Pin Select Register 1	TRCPSR1	00h
0184h			
0185h			
0186h			
0187h			
0188h	UART0 Pin Select Register	U0SR	00h
0189h			
018Ah			
018Bh			
018Ch	SSU/IIC Pin Select Register	SSUIICSR	00h
018Dh			
018Eh	INT Interrupt Input Pin Select Register	INTSR	00h
018Fh	I/O Function Pin Select Register	PINSR	00h
0190h			
0191h			
0192h			
0193h	SS Bit Counter Register	SSBR	11111000b
0194h	SS Transmit Data Register L / IIC bus Transmit Data Register (2)	SSTDR / ICDRT	FFh
0195h	SS Transmit Data Register H (2)	SSTDRH	FFh
0196h	SS Receive Data Register L / IIC bus Receive Data Register (2)	SSRDR / ICDRR	FFh
0197h	SS Receive Data Register H (2)	SSRDRH	FFh
0198h	SS Control Register H / IIC bus Control Register 1 (2)	SSCRH / ICCR1	00h
0199h	SS Control Register L / IIC bus Control Register 2 (2)	SSCRL / ICCR2	01111101b
019Ah	SS Mode Register / IIC bus Mode Register (2)	SSMR / ICMR	00011000b
019Bh	SS Enable Register / IIC bus Interrupt Enable Register (2)	SSER / ICIER	00h
019Ch	SS Status Register / IIC bus Status Register (2)	SSSR / ICSR	00h / 0000X000b
019Dh	SS Mode Register 2 / Slave Address Register (2)	SSMR2 / SAR	00h
019Eh			
019Fh			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.
2. Selectable by the IICSEL bit in the SSUIICSR register.

Table 4.11 SFR Information (11) (2D30h to 2FFFh) (1)

Address	Register	Symbol	After Reset
2D30h	Time Stamp Register 0	BBTSTAMP0	00h
2D31h			00h
2D32h	Time Stamp Register 1	BBTSTAMP1	00h
2D33h			00h
2D34h	Timer Control Register	BBTIMECON	00h
2D35h	Backoff Period Register	BBBOFFPROD	00h
2D36h			
2D37h			
2D38h			
2D39h			
2D3Ah	PLL Division Register 0	BBPLLDIVL	65h
2D3Bh	PLL Division Register 1	BBPLLDIVH	09h
2D3Ch	Transmit Output Power Register	BBTXOUTPWR	00h
2D3Dh	RSSI Offset Register	BBRSSIOFS	F6h
2D3Eh			
2D3Fh			
2D40h			
:			
2D45h			
2D46h	Automatic ACK Response Timing Adjustment Register	BBACKRTNTIMG	22h
2D47h			
:			
2D63h			
2D64h			
2D65h			
2D66h			
2D67h			
2D68h	Verification Mode Set Register	BBEVAREG	00h
2D69h			
2D6Ah			
2D6Bh			
2D6Ch			
2D6Dh			
2D6Eh			
2D6Fh			
2D70h			
2D71h			
2D72h			
2D73h			
2D74h			
2D75h			
2D76h	IDLE Wait Set Register	BBIDELWAIT	01h
2D77h			
2D78h			
2D79h			
2D7Ah	ANTSW Output Timing Set Register	BBANTSWTIMG	72h
2D7Bh			
2D7Ch	RF Initial Set Register	BBRFINI	XXh
2D7Dh			XXh
2D7Eh			
2D7Fh			
2D80h			
2D81h			
2D82h	ANTSW Control Register	BBANTSWCON	00h
2D83h			
:			
2DFFh			
2E00h	Transmit RAM	TRANSMIT_RAM_START	
:	Transmit RAM		
2E7Eh	Transmit RAM	TRANSMIT_RAM_END	
2E7Fh			
2D80h	Receive RAM	RECIEVE_RAM_START	
:	Receive RAM		
2EFEh	Receive RAM	RECIEVE_RAM_END	
2EFFh			
2F00h			
:			
2FFFh			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.12 ID Code Areas and Option Function Select Area

Address	Area Name	Symbol	After Reset
:			
FFDBh	Option Function Select Register 2	OFS2	(Note 1)
:			
FFDFh	ID1		(Note 2)
:			
FFE3h	ID2		(Note 2)
:			
FFEBh	ID3		(Note 2)
:			
FFEFh	ID4		(Note 2)
:			
FFF3h	ID5		(Note 2)
:			
FFF7h	ID6		(Note 2)
:			
FFFBh	ID7		(Note 2)
:			
FFFFh	Option Function Select Register	OFS	(Note 1)

Notes:
1. The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the option function select area. If the block including the option function select area is erased, the option function select area is set to FFh.
   At shipment, the option function select area is set to FFh. It is set to the written value after written by the user.
2. The ID code areas are allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the ID code areas. If the block including the ID code areas is erased, the ID code areas are set to FFh.
   At shipment, the ID code areas are set to FFh. They are set to the written value after written by the user.

Table 5.4 Flash Memory (Data flash Block A to Block D) Electrical Characteristics

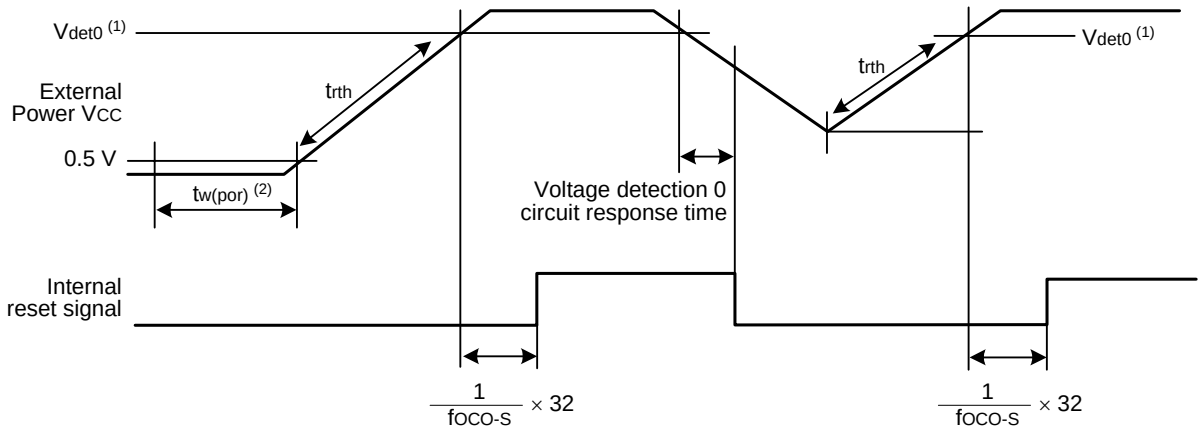
Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
—	Program/erase endurance (2)		10,000 (3)	—	—	times
—	Byte program time (program/erase endurance ≤ 1,000 times)		—	160	1500	µs
—	Byte program time (program/erase endurance > 1,000 times)		—	300	1500	µs
—	Block erase time (program/erase endurance ≤ 1,000 times)		—	0.2	1	s
—	Block erase time (program/erase endurance > 1,000 times)		—	0.3	1	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		—	—	5 + CPU clock × 3 cycles	ms
—	Interval from erase start/restart until following suspend request		0	—	—	µs
—	Time from suspend until erase restart		—	—	30 + CPU clock × 1 cycle	µs
$t_{d(CMDRST-READY)}$	Time from when command is forcibly stopped until reading is enabled		—	—	30 + CPU clock × 1 cycle	µs
—	Program, erase voltage	CPU rewrite mode	1.8	—	3.6	V
		Standard serial I/O mode	2.7	—	3.6	
		Parallel I/O mode	2.7	—	3.6	
—	Read voltage		1.8	—	3.6	V
—	Program, erase temperature	CPU rewrite mode	−20	—	85	°C
		Standard serial I/O mode	0	—	60	
		Parallel I/O mode	0	—	60	
—	Data hold time (7)	Ambient temperature = 55°C	20	—	—	year

Notes:
1. V_{CC} = 1.8 to 3.6 V and T_{opr} = −20°C to 85°C, unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one. However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed.)
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the erasure endurance between blocks A to D can further reduce the actual erasure endurance. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.7 Power-on Reset Circuit (2)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t_{rth}	External power V_{CC} rise gradient	(1)	0	—	50,000	mV/msec

Notes:
1. The measurement condition is T_{opr} = –20°C to 85°C, unless otherwise specified.
2. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.



Notes:
1. V_{det0} indicates the voltage detection level of the voltage detection 0 circuit. Refer to **6. Voltage Detection Circuit** of User's Manual: Hardware for details.
2. $t_{w(por)}$ indicates the duration the external power V_{CC} must be held below the valid voltage (0.5 V) to enable a power-on reset. When turning on the power after it falls with voltage monitor 0 reset disabled, maintain $t_{w(por)}$ for 1 ms or more.

Figure 5.3 Power-on Reset Circuit Electrical Characteristics

Table 5.8 System Clock Low-Speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-S	Low-speed on-chip oscillator frequency		100	125	150	kHz
—	Oscillation stability time		—	30	100	µs

Note:
1. V_{CC} = 1.8 V to 3.6 V and T_{opr} = –20°C to 85°C, unless otherwise specified.

Table 5.9 Watchdog Timer Low-Speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-WDT	Low-speed on-chip oscillator frequency		60	125	250	kHz
—	Oscillation stability time		—	30	100	µs

Note:
1. V_{CC} = 1.8 V to 3.6 V and T_{opr} = –20°C to 85°C, unless otherwise specified.

Table 5.10 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for internal power supply stabilization during power-on (2)		—	—	2,000	µs

Notes:
1. The measurement condition is V_{CC} = 1.8 to 3.6 V and T_{opr} = 25°C.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.

Table 5.11 Timing Requirements of Synchronous Serial Communication Unit (SSU) (1)

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
t_{SUCYC}	SSCK clock cycle time			4	—	—	t_{CYC} (2)
t_{HI}	SSCK clock “H” width			0.4	—	0.6	t_{SUCYC}
t_{LO}	SSCK clock “L” width			0.4	—	0.6	t_{SUCYC}
t_{RISE}	SSCK clock rising time	Master		—	—	1	t_{CYC} (2)
		Slave		—	—	1	µs
t_{FALL}	SSCK clock falling time	Master		—	—	1	t_{CYC} (2)
		Slave		—	—	1	µs
t_{SU}	SSO, SSI data input setup time			100	—	—	ns
t_H	SSO, SSI data input hold time			1	—	—	t_{CYC} (2)
t_{LEAD}	$\overline{SCS}$ setup time	Slave		1t_{CYC} + 50	—	—	ns
t_{LAG}	$\overline{SCS}$ hold time	Slave		1t_{CYC} + 50	—	—	ns
t_{OD}	SSO, SSI data output delay time			—	—	1.5	t_{CYC} (2)
t_{SA}	SSI slave access time		2.7 V ≤ V_{CC} ≤ 3.6 V	—	—	1.5t_{CYC} + 100	ns
			1.8 V ≤ V_{CC} < 2.7 V	—	—	1.5t_{CYC} + 200	ns
t_{OR}	SSI slave out open time		2.7 V ≤ V_{CC} ≤ 3.6 V	—	—	1.5t_{CYC} + 100	ns
			1.8 V ≤ V_{CC} < 2.7 V	—	—	1.5t_{CYC} + 200	ns

Notes:
1. V_{CC} = 1.8 V to 3.6 V and T_{opr} = –20°C to 85°C, unless otherwise specified.
2. 1t_{CYC} = 1/f1(s)

Table 5.14 Electrical Characteristics (2) [2.7 V ≤ Vcc ≤ 3.6 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” voltage	P0_4, P1, P3_0, P3_1, P3_3 to P3_5, P3_7, P4_3 to P4_5	Drive capacity High	I_{OH} = –5 mA	V_{CC} – 0.5	—	V_{CC}	V
			Drive capacity Low	I_{OH} = –1 mA	V_{CC} – 0.5	—	V_{CC}	V
V_{OL}	Output “L” voltage	P0_4, P1, P3_0, P3_1, P3_3 to P3_5, P3_7, P4_3 to P4_5	Drive capacity High	I_{OL} = 5 mA	—	—	0.5	V
			Drive capacity Low	I_{OL} = 1 mA	—	—	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, $\overline{KI4}$, $\overline{KI6}$, $\overline{KI7}$, TRAIO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRCTRG, TRCCLK, RXD0, CLK0, SSI, SCL, SDA, SSO	VCC = 3.0 V		0.1	0.4	—	V
		$\overline{RESET}$	VCC = 3.0 V		0.1	0.5	—	V
I_{IH}	Input “H” current		V_I = 3 V, V_{CC} = 3.0 V		—	—	4.0	µA
I_{IL}	Input “L” current		V_I = 0 V, V_{CC} = 3.0 V		—	—	–4.0	µA
R_{PULLUP}	Pull-up resistance		V_I = 0 V, V_{CC} = 3.0 V		42	84	168	kΩ
R_{fXIN}	Feedback resistance	XIN			—	0.3	—	MΩ
R_{fXCIN}	Feedback resistance	XCIN			—	8	—	MΩ
V_{RAM}	RAM hold voltage		During stop mode		1.8	—	3.6	V

Note:
1. 2.7 V ≤ V_{CC} ≤ 3.6 V, T_{opr} = –20°C to 85°C, and f(XIN) =16 MHz, unless otherwise specified.

Timing requirements (VCC = 3 V, Topr = −20°C to 85°C, unless otherwise specified)

Table 5.15 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	300	—	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	120	—	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	120	—	ns

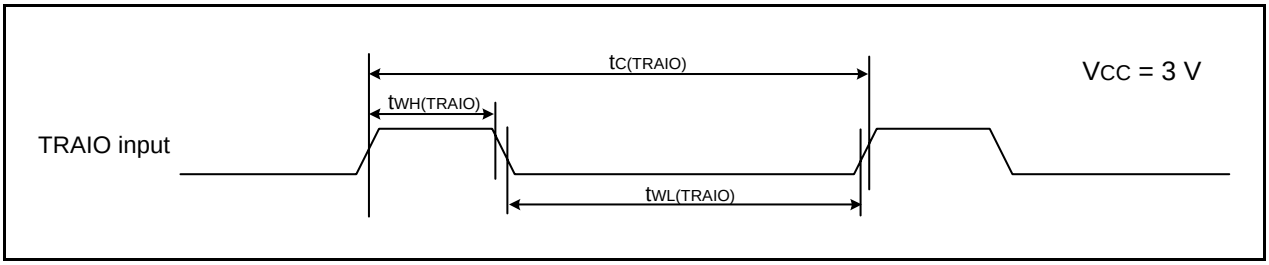


Figure 5.8 TRAIO Input Timing Diagram when VCC = 3 V

Table 5.16 Serial Interface

Symbol	Parameter		Standard		Unit
			Min.	Max.	
$t_{c(CK)}$	CLK0 input cycle time	When an external clock is selected	300	—	ns
$t_{W(CKH)}$	CLK0 input “H” width		150	—	ns
$t_{W(CKL)}$	CLK0 Input “L” width		150	—	ns
$t_{d(C-Q)}$	TXD0 output delay time		—	120	ns
$t_{h(C-Q)}$	TXD0 hold time		0	—	ns
$t_{su(D-C)}$	RXD0 input setup time		30	—	ns
$t_{h(C-D)}$	RXD0 input hold time		90	—	ns
$t_{h(C-Q)}$	TXD0 output delay time	When an internal clock is selected	—	30	ns
$t_{su(D-C)}$	RXD0 input setup time		120	—	ns
$t_{h(C-D)}$	RXD0 input hold time		90	—	ns

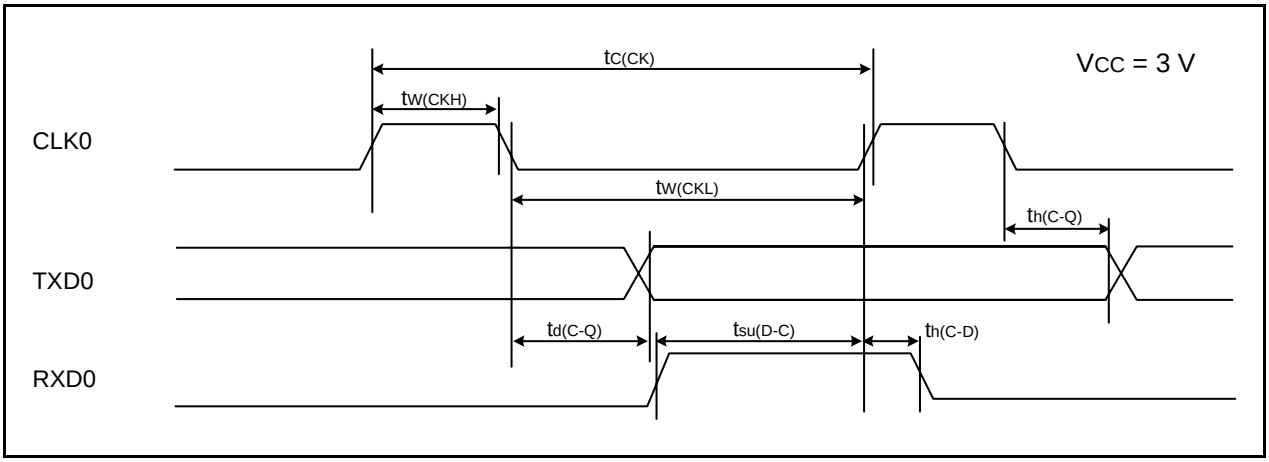


Figure 5.9 Serial Interface Timing Diagram when VCC = 3 V

Table 5.21 External Interrupt $\overline{INTi}$ (i = 0, 1, 3) Input, Key Input Interrupt $\overline{KIi}$ (i = 0 to 7)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input “H” width, $\overline{KIi}$ input “H” width	1000 (1)	—	ns
$t_{W(INL)}$	$\overline{INTi}$ input “L” width, $\overline{KIi}$ input “L” width	1000 (2)	—	ns

Notes:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

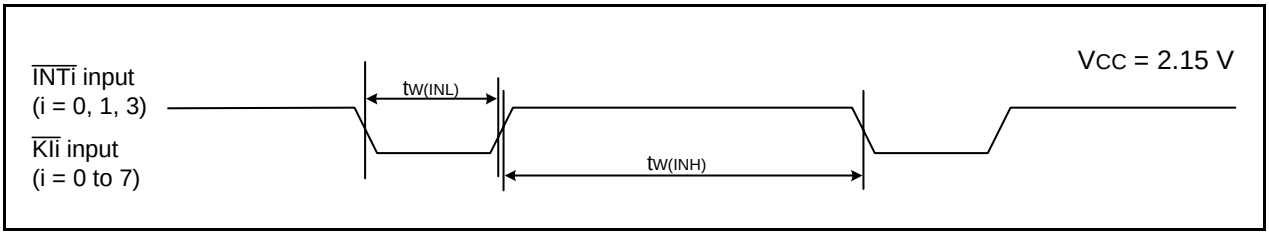
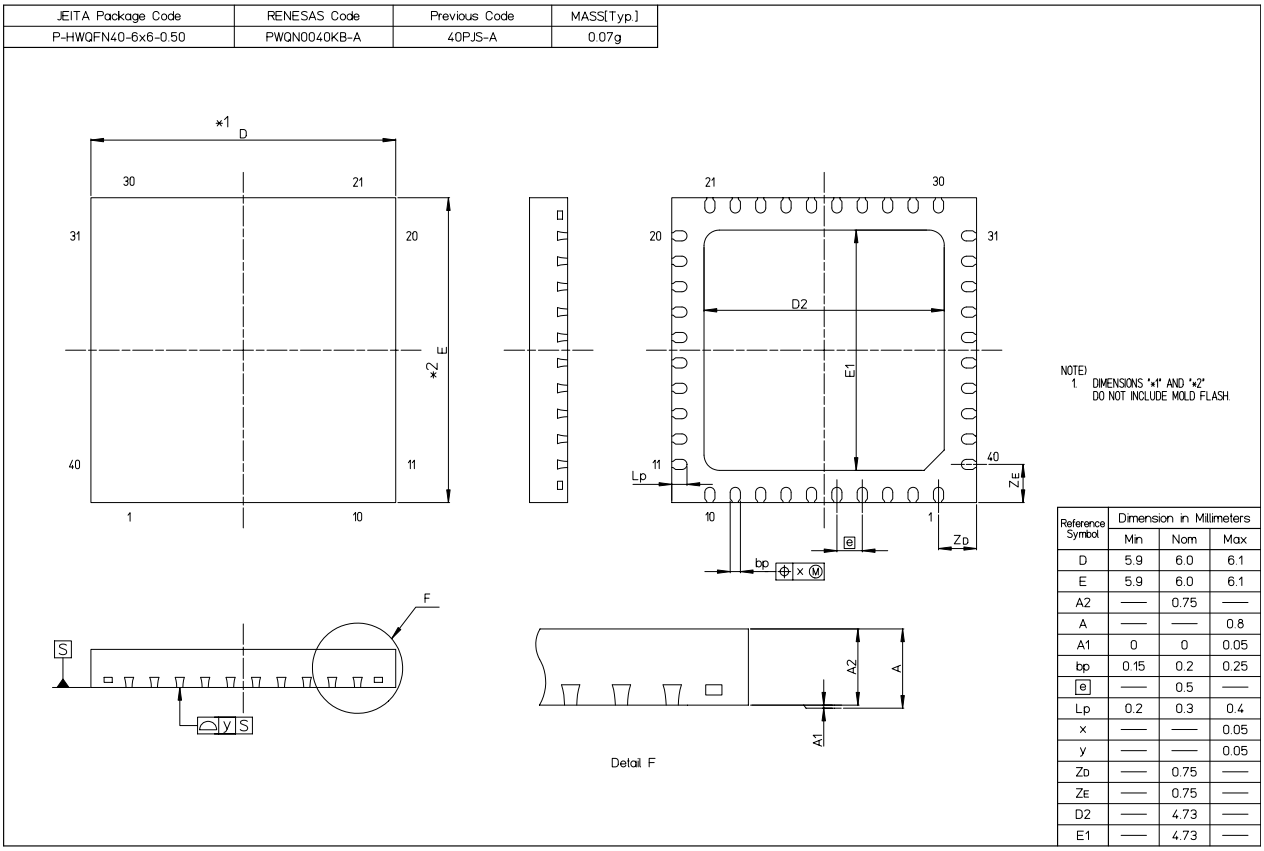


Figure 5.13 Input Timing Diagram for External Interrupt $\overline{INTi}$ and Key Input Interrupt $\overline{KIi}$ when V_{CC} = 2.15 V

Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Electronics website.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-HWQFN40-6x6-0.50	PWQN0040KB-A	40PJS-A	0.07g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	5.9	6.0	6.1
E	5.9	6.0	6.1
A2	—	0.75	—
A	—	—	0.8
A1	0	0	0.05
bp	0.15	0.2	0.25
e	—	0.5	—
Lp	0.2	0.3	0.4
x	—	—	0.05
y	—	—	0.05
Zp	—	0.75	—
ZE	—	0.75	—
D2	—	4.73	—
E1	—	4.73	—

REVISION HISTORY	R8C/3MQ Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.10	Nov 19, 2010	—	First Edition issued
1.00	Aug 11, 2011	All pages	“Preliminary”, “Under development” deleted
		4	Table 1.2 revised, Note 1 added
		5	Table 1.3 “(D): Under development”, (P): Under planning” deleted
		6	Figure 1.2 revised
		7	Figure 1.3 revised
		9, 10	Table 1.5, Table 1.6 revised
		12	2.4 revised
		14	3.1 revised
		16, 17	Table 4.2, Table 4.3 revised
		19	Table 4.5 Note 2 added
		20	Table 4.6 revised
		24, 25	Table 4.10, Table 4.11 revised
		32	Table 5.6 revised
		39	Table 5.13 revised
		46	Table 5.22, Table 5.23 revised, Table 5.22 Note 1 added
2.00	Jun 29, 2012	2	Table 1.1 “Voltage detection” revised, Table 1.2 “2.2 V” → “2.15 V”
		3, 4	Tables 1.2 and 1.3 “2.2 V” → “2.15 V”
		5	Table 1.4 and Figure 1.1 revised
		6	Figure 1.2 revised
		14	Figure 3.1 revised
		28	Table 5.2 “2.2 V” → “2.15 V”
		32	Table 5.5 revised, Note 4 added
		39	Table 5.13 “2.2 V” → “2.15 V”
		43	Table 5.18 “2.2 V” → “2.15 V”
		44, 45	Timing requirements, Figures 5.11 to 5.13, titles “2.2 V” → “2.15 V”
		46	Table 5.23 revised