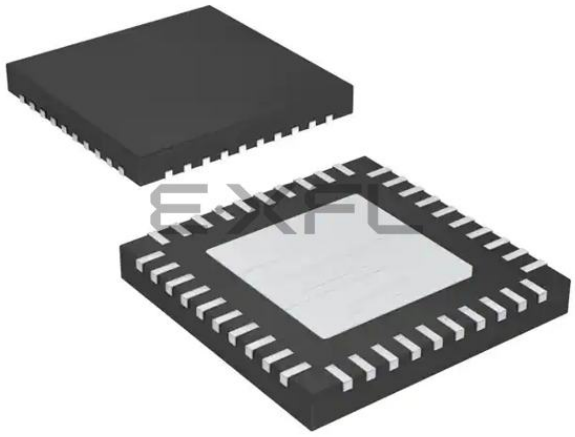
Renesas Electronics America Inc - R5F213M7QNNP#U0 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	R8C
Core Size	16-Bit
Speed	16MHz
Connectivity	I²C, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	18
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-WFQFN Exposed Pad
Supplier Device Package	40-HWQFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f213m7qnnp-u0

Table 1.2 Specifications for R8C/3MQ Group (2)

Item	Function	Specification
Serial Interface (UART0)		Shared with clock synchronous serial I/O mode and clock asynchronous serial I/O
Synchronous Serial Communication Unit (SSU)		1 (shared with I²C bus)
I²C bus		1 (shared with SSU)
RF	RF frequency	2405 MHz to 2480 MHz
	Reception sensitivity	-95 dBm
	Transmission output level	0 dBm
Baseband		• 127-byte transmit RAM, 127-byte receive RAM × 2 • Automatic ACK response function • 26-bit timer: Compare function in 3 channels
Encryption	AES	AES Encryption/Decryption (Key length 128bits)
Flash Memory		• Programming and erasure voltage: VCC = 1.8 to 3.6 V (in CPU rewrite mode) • Programming and erasure endurance: 10,000 times (data flash) 1,000 times (program ROM) • Program security: ROM code protect, ID code check • Debug functions: On-chip debug, on-board flash rewrite function • Background operation (BGO) function
Operating Frequency/ Supply Voltage (in single mode)		f(BCLK) = 16 MHz, VCC = 2.7 to 3.6 V) f(BCLK) = 8 MHz (VCC = 2.15 to 3.6V) f(BCLK) = 4 MHz, VCC = 1.8 to 3.6 V) Note: f(XIN) = fixed at 16 MHz

1.3 Block Diagram

Figure 1.2 shows a Block Diagram.

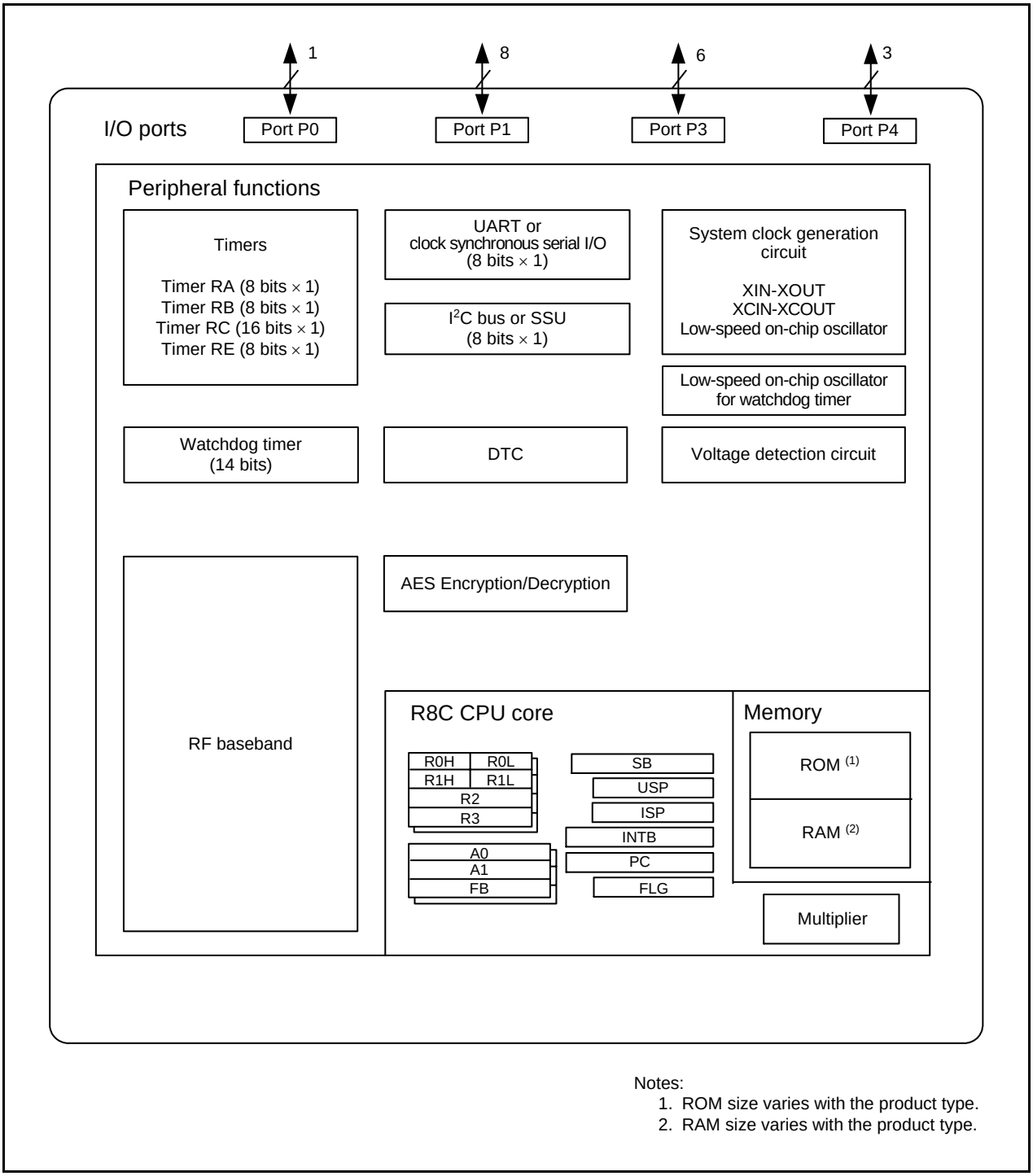


Figure 1.2 Block Diagram

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the starting address of a relocatable interrupt vector table.

2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.11 list the special function registers. Table 4.12 lists the ID Code Areas and Option Function Select Area.

Table 4.1 SFR Information (1) (0000h to 002Fh) (1)

Address	Register	Symbol	After Reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	00101000b
0007h	System Clock Control Register 1	CM1	00101000b
0008h	Module Standby Control Register	MSTCR	00h
0009h	System Clock Control Register 3	CM3	00h
000Ah	Protect Register	PRCR	00h
000Bh	Reset Source Determination Register	RSTFR	0XXXXXXXb (2)
000Ch	Oscillation Stop Detection Register	OCD	00000100b
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDTC	00111111b
0010h			
0011h			
0012h			
0013h			
0014h			
0015h			
0016h			
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	00h 10000000b (3)
001Dh			
001Eh			
001Fh			
0020h			
0021h			
0022h			
0023h			
0024h			
0025h			
0026h			
0027h			
0028h	Clock Prescaler Reset Flag	CPSRF	00h
0029h			
002Ah			
002Bh			
002Ch			
002Dh			
002Eh			
002Fh			

X: Undefined

Notes:

1. The blank areas are reserved and cannot be accessed by users.
2. The CWR bit in the RSTFR register is set to 0 after power-on and voltage monitor 0 reset. Hardware reset, software reset, or watchdog timer reset does not affect this bit.
3. The CSPROINI bit in the OFS register is set to 0.

Table 4.4 SFR Information (4) (00B0h to 011Fh) (1)

Address	Register	Symbol	After Reset
00B0h			
:			
00DFh			
00DFh			
00E0h	Port P0 Register	P0	XXh
00E1h	Port P1 Register	P1	XXh
00E2h	Port P0 Direction Register	PD0	00h
00E3h	Port P1 Direction Register	PD1	00h
00E4h			
00E5h	Port P3 Register	P3	XXh
00E6h			
00E7h	Port P3 Direction Register	PD3	00h
00E8h	Port P4 Register	P4	XXh
00E9h			
00EAh	Port P4 Direction Register	PD4	00h
00EBh			
00ECh			
00EDh			
00EEh			
00EFh			
00F0h			
00F1h			
00F2h			
00F3h			
00F4h			
00F5h			
00F6h			
00F7h			
00F8h			
00F9h			
00FAh			
00FBh			
00FCh			
00FDh			
00FEh			
00FFh			
0100h	Timer RA Control Register	TRACR	00h
0101h	Timer RA I/O Control Register	TRAIOC	00h
0102h	Timer RA Mode Register	TRAMR	00h
0103h	Timer RA Prescaler Register	TRAPRE	FFh
0104h	Timer RA Register	TRA	FFh
0105h			
0106h			
0107h			
0108h	Timer RB Control Register	TRBCR	00h
0109h	Timer RB One-Shot Control Register	TRBOCR	00h
010Ah	Timer RB I/O Control Register	TRBIOC	00h
010Bh	Timer RB Mode Register	TRBMR	00h
010Ch	Timer RB Prescaler Register	TRBPRE	FFh
010Dh	Timer RB Secondary Register	TRBSC	FFh
010Eh	Timer RB Primary Register	TRBPR	FFh
010Fh			
0110h			
0111h			
0112h			
0113h			
0114h			
0115h			
0116h			
0117h			
0118h	Timer RE Second Data Register / Counter Data Register	TRESEC	00h
0119h	Timer RE Minute Data Register / Compare Data Register	TREMIN	00h
011Ah	Timer RE Hour Data Register	TREHR	00h
011Bh	Timer RE Day of Week Data Register	TREWK	00h
011Ch	Timer RE Control Register 1	TRECR1	00h
011Dh	Timer RE Control Register 2	TRECR2	00h
011Eh	Timer RE Count Source Select Register	TRECSR	00001000b
011Fh			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

5. Electrical Characteristics

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter		Condition	Rated Value	Unit
VCC	Digital supply voltage			–0.3 to 3.8	V
VCCRF	Analog supply voltage			–0.3 to 3.8	V
V_I	Input voltage	$\overline{\text{RESET}}$, MODE, P0_4, P1, P3_0, P3_1, P3_3 to P3_5, P3_7, P4_3 to P4_5		–0.3 to V_{CC} + 0.3	V
V_O	Output voltage	P0_4, P1, P3_0, P3_1, P3_3 to P3_5, P3_7, P4_3 to P4_5		–0.3 to V_{CC} + 0.3	V
VRFIO	RF I/O pins	RFIOP, RFION		–0.3 to 2.1	V
VTESTIO	Test ports	IFRXTP, IFRXTN		–0.3 to 2.1	V
VANAIN	1.5 V analog supply (input)	VREG1, VREG2, VREG3, VREG4		–0.3 to 2.1	V
VANAOUT	1.5 V analog supply (output)	VREGOUT1, VREGOUT2, VREGOUT3		–0.3 to 2.1	V
VXINOUT	Main clock I/O	XIN, XOUT		–0.3 to 2.1	V
P_d	Power dissipation		–20°C ≤ T_{opr} ≤ 85°C	300	mW
T_{opr}	Operating ambient temperature	(1) During MCU operation under the conditions other than (2) and (3) below.		–20 to 85	°C
		(2) During programming and erasing of the flash memory using a serial programmer or parallel programmer.		0 to 60	
		(3) During on-chip debugging with the E8a emulator connected		10 to 35	
T_{stg}	Storage temperature			–65 to 150	°C

Table 5.2 Recommended Operating Conditions (1)

Symbol	Parameter				Conditions	Standard			Unit
						Min.	Typ.	Max.	
VCC	Digital supply voltage	(1) During MCU operation under the conditions other than (2) and (3) below.				1.8	3.3	3.6	V
		(2) During programming and erasing of the flash memory using a serial programmer or parallel programmer.				2.7	—	3.6	
		(3) During on-chip debugging with the E8a emulator connected				2.7	—	3.6	
VCCRF	Analog supply voltage					1.8	3.3	3.6	V
VSS/ VSS2/ VSSRF/ VSSRF1/ VSSRF2/ DIEGND	Supply voltage	VSS1, VSS2, VSSRF, VSSRF1, VSSRF2, DIEGND				—	0	—	V
V_{IH}	Input “H” voltage	Other than CMOS input				0.8 Vcc	—	Vcc	V
		CMOS input	Input level switching function (I/O port)	Input level selection: 0.35 Vcc	2.7 V ≤ Vcc ≤ 3.6 V	0.55 Vcc	—	Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0.65 Vcc	—	Vcc	V
				Input level selection: 0.5 Vcc	2.7 V ≤ Vcc ≤ 3.6 V	0.7 Vcc	—	Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0.8 Vcc	—	Vcc	V
				Input level selection: 0.7 Vcc	2.7 V ≤ Vcc ≤ 3.6 V	0.85 Vcc	—	Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0.85 Vcc	—	Vcc	V
V_{IL}	Input “L” voltage	Other than CMOS input				0	—	0.2 Vcc	V
		CMOS input	Input level switching function (I/O port)	Input level selection: 0.35 Vcc	2.7 V ≤ Vcc ≤ 3.6 V	0	—	0.2 Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0	—	0.2 Vcc	V
				Input level selection: 0.5 Vcc	2.7 V ≤ Vcc ≤ 3.6 V	0	—	0.3 Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0	—	0.2 Vcc	V
				Input level selection: 0.7 Vcc	2.7 V ≤ Vcc ≤ 3.6 V	0	—	0.45 Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0	—	0.35 Vcc	V
$I_{OH(sum)}$	Peak sum output “H” current	Sum of all pins $I_{OH(peak)}$				—	—	−160	mA
$I_{OH(sum)}$	Average sum output “H” current	Sum of all pins $I_{OH(avg)}$				—	—	−80	mA
$I_{OH(peak)}$	Peak output “H” current	Drive capacity Low				—	—	−10	mA
		Drive capacity High				—	—	−40	mA
$I_{OH(avg)}$	Average output “H” current	Drive capacity Low				—	—	−5	mA
		Drive capacity High				—	—	−20	mA
$I_{OL(sum)}$	Peak sum output “L” current	Sum of all pins $I_{OL(peak)}$				—	—	160	mA
$I_{OL(sum)}$	Average sum output “L” current	Sum of all pins $I_{OL(avg)}$				—	—	80	mA
$I_{OL(peak)}$	Peak output “L” current	Drive capacity Low				—	—	10	mA
		Drive capacity High				—	—	40	mA
$I_{OL(avg)}$	Average output “L” current	Drive capacity Low				—	—	5	mA
		Drive capacity High				—	—	20	mA
$f_{(XIN)}$	XIN clock input oscillation frequency				1.8 V ≤ Vcc ≤ 3.6 V	—	16	—	MHz
$f_{(XCIN)}$	XCIN clock input oscillation frequency				1.8 V ≤ Vcc ≤ 3.6 V	30	32.768	35	kHz
—	System clock frequency	f(XIN)=16 MHz			1.8 V ≤ Vcc ≤ 3.6 V	—	—	16	MHz
$f_{(BCLK)}$	CPU clock frequency	f(XIN)=16 MHz			2.7 V ≤ Vcc ≤ 3.6 V	—	—	16	MHz
					2.15 V ≤ Vcc < 2.7 V	—	—	8	
					1.8 V ≤ Vcc < 2.15 V	—	—	4	

Notes:
1. Vcc = 1.8 to 3.6 V and T_{opr} = −20°C to 85°C, unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.

Table 5.3 Flash Memory (Program ROM) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
—	Program/erase endurance (2)		1,000 (3)	—	—	times
—	Byte program time		—	80	500	µs
—	Block erase time		—	0.3	—	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		—	—	5 + CPU clock × 3 cycles	ms
—	Interval from erase start/restart until following suspend request		0	—	—	µs
—	Time from suspend until erase restart		—	—	30 + CPU clock × 1 cycle	µs
$t_{d(CMDRST-READY)}$	Time from when command is forcibly stopped until reading is enabled		—	—	30 + CPU clock × 1 cycle	µs
—	Program, erase voltage	CPU rewrite mode	1.8	—	3.6	V
		Standard serial I/O mode	2.7	—	3.6	
		Parallel I/O mode	2.7	—	3.6	
—	Read voltage		1.8	—	3.6	V
—	Program, erase temperature		0	—	60	°C
—	Data hold time (7)	Ambient temperature = 55°C	20	—	—	year

Notes:
1. V_{CC} = 2.7 to 3.6 V and T_{opr} = 0 to 60°C, unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one. However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed.)
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.4 Flash Memory (Data flash Block A to Block D) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
—	Program/erase endurance (2)		10,000 (3)	—	—	times
—	Byte program time (program/erase endurance ≤ 1,000 times)		—	160	1500	µs
—	Byte program time (program/erase endurance > 1,000 times)		—	300	1500	µs
—	Block erase time (program/erase endurance ≤ 1,000 times)		—	0.2	1	s
—	Block erase time (program/erase endurance > 1,000 times)		—	0.3	1	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		—	—	5 + CPU clock × 3 cycles	ms
—	Interval from erase start/restart until following suspend request		0	—	—	µs
—	Time from suspend until erase restart		—	—	30 + CPU clock × 1 cycle	µs
$t_{d(CMDRST-READY)}$	Time from when command is forcibly stopped until reading is enabled		—	—	30 + CPU clock × 1 cycle	µs
—	Program, erase voltage	CPU rewrite mode	1.8	—	3.6	V
		Standard serial I/O mode	2.7	—	3.6	
		Parallel I/O mode	2.7	—	3.6	
—	Read voltage		1.8	—	3.6	V
—	Program, erase temperature	CPU rewrite mode	−20	—	85	°C
		Standard serial I/O mode	0	—	60	
		Parallel I/O mode	0	—	60	
—	Data hold time (7)	Ambient temperature = 55°C	20	—	—	year

Notes:
1. V_{CC} = 1.8 to 3.6 V and T_{opr} = −20°C to 85°C, unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one. However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed.)
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the erasure endurance between blocks A to D can further reduce the actual erasure endurance. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

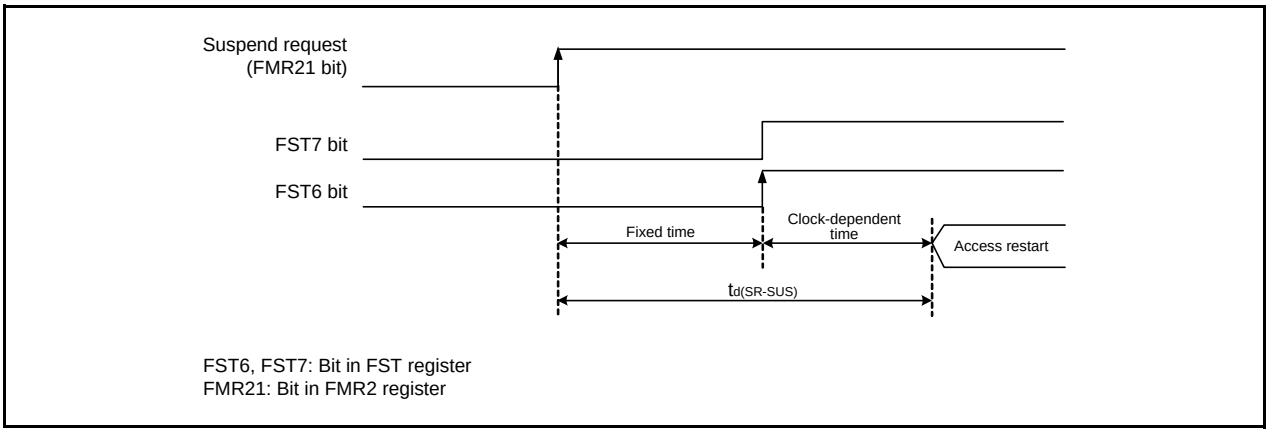


Figure 5.2 Time delay until Suspend

Table 5.5 Voltage Detection 0 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det0}	Voltage detection level Vdet0_0 (4)		1.80	1.90	2.05	V
	Voltage detection level Vdet0_1 (4)		2.15	2.35	2.50	V
	Voltage detection level Vdet0_2 (4)		2.70	2.85	3.05	V
—	Voltage detection 0 circuit response time (3)	At the falling of V_{CC} from 3.6 V to (Vdet0_0 – 0.1) V	—	6	150	µs
—	Voltage detection circuit self power consumption	VCA25 = 1, V_{CC} = 3.0 V	—	1.5	—	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts (2)		—	—	100	µs

Notes:
1. The measurement condition is V_{CC} = 1.8 V to 3.6 V and T_{opr} = –20°C to 85°C.
2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.
3. Time until the voltage monitor 0 reset is generated after the voltage passes V_{det0}.
4. Select the voltage detection level with bits VDSEL0 and VDSEL1 in the OFS register.

Table 5.6 Voltage Detection 1 Circuit Electrical Characteristics

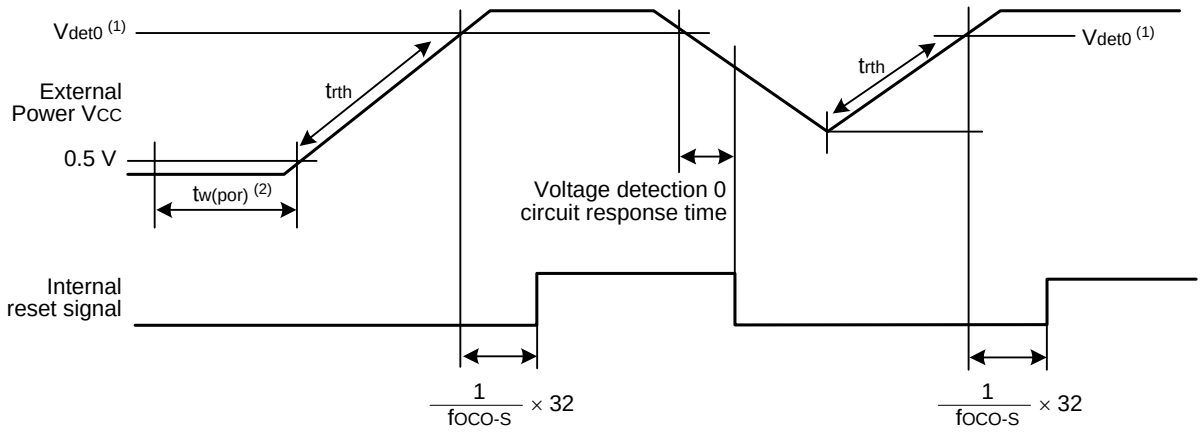
Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det1}	Voltage detection level Vdet1_2 (2)	At the falling of V_{CC}	2.30	2.50	2.70	V
	Voltage detection level Vdet1_5 (2)	At the falling of V_{CC}	2.75	2.95	3.15	V
—	Hysteresis width at the rising of V_{CC} in voltage detection 1 circuit		—	0.07	—	V
—	Voltage detection 1 circuit response time (3)	At the falling of V_{CC} from 3.6 V to (Vdet1_0 – 0.1) V	—	60	150	µs
—	Voltage detection circuit self power consumption	VCA26 = 1, V_{CC} = 3.0 V	—	1.7	—	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts (4)		—	—	100	µs

Notes:
1. The measurement condition is V_{CC} = 1.8 V to 3.6 V and T_{opr} = –20°C to 85°C.
2. Select the voltage detection level with bits VD1S0 to VD1S3 in the VD1LS register.
3. Time until the voltage monitor 1 interrupt request is generated after the voltage passes V_{det1}.
4. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

Table 5.7 Power-on Reset Circuit (2)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t_{rth}	External power V_{CC} rise gradient	(1)	0	—	50,000	mV/msec

Notes:
1. The measurement condition is T_{opr} = –20°C to 85°C, unless otherwise specified.
2. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.



Notes:
1. V_{det0} indicates the voltage detection level of the voltage detection 0 circuit. Refer to **6. Voltage Detection Circuit** of User's Manual: Hardware for details.
2. $t_{w(por)}$ indicates the duration the external power V_{CC} must be held below the valid voltage (0.5 V) to enable a power-on reset. When turning on the power after it falls with voltage monitor 0 reset disabled, maintain $t_{w(por)}$ for 1 ms or more.

Figure 5.3 Power-on Reset Circuit Electrical Characteristics

Table 5.8 System Clock Low-Speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-S	Low-speed on-chip oscillator frequency		100	125	150	kHz
—	Oscillation stability time		—	30	100	µs

Note:
1. V_{CC} = 1.8 V to 3.6 V and T_{opr} = –20°C to 85°C, unless otherwise specified.

Table 5.9 Watchdog Timer Low-Speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-WDT	Low-speed on-chip oscillator frequency		60	125	250	kHz
—	Oscillation stability time		—	30	100	µs

Note:
1. V_{CC} = 1.8 V to 3.6 V and T_{opr} = –20°C to 85°C, unless otherwise specified.

Table 5.10 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for internal power supply stabilization during power-on (2)		—	—	2,000	µs

Notes:
1. The measurement condition is V_{CC} = 1.8 to 3.6 V and T_{opr} = 25°C.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.

Table 5.11 Timing Requirements of Synchronous Serial Communication Unit (SSU) (1)

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
t_{SUCYC}	SSCK clock cycle time			4	—	—	t_{CYC} (2)
t_{HI}	SSCK clock “H” width			0.4	—	0.6	t_{SUCYC}
t_{LO}	SSCK clock “L” width			0.4	—	0.6	t_{SUCYC}
t_{RISE}	SSCK clock rising time	Master		—	—	1	t_{CYC} (2)
		Slave		—	—	1	µs
t_{FALL}	SSCK clock falling time	Master		—	—	1	t_{CYC} (2)
		Slave		—	—	1	µs
t_{SU}	SSO, SSI data input setup time			100	—	—	ns
t_H	SSO, SSI data input hold time			1	—	—	t_{CYC} (2)
t_{LEAD}	$\overline{SCS}$ setup time	Slave		1t_{CYC} + 50	—	—	ns
t_{LAG}	$\overline{SCS}$ hold time	Slave		1t_{CYC} + 50	—	—	ns
t_{OD}	SSO, SSI data output delay time			—	—	1.5	t_{CYC} (2)
t_{SA}	SSI slave access time		2.7 V ≤ V_{CC} ≤ 3.6 V	—	—	1.5t_{CYC} + 100	ns
			1.8 V ≤ V_{CC} < 2.7 V	—	—	1.5t_{CYC} + 200	ns
t_{OR}	SSI slave out open time		2.7 V ≤ V_{CC} ≤ 3.6 V	—	—	1.5t_{CYC} + 100	ns
			1.8 V ≤ V_{CC} < 2.7 V	—	—	1.5t_{CYC} + 200	ns

Notes:
1. V_{CC} = 1.8 V to 3.6 V and T_{opr} = –20°C to 85°C, unless otherwise specified.
2. 1t_{CYC} = 1/f1(s)

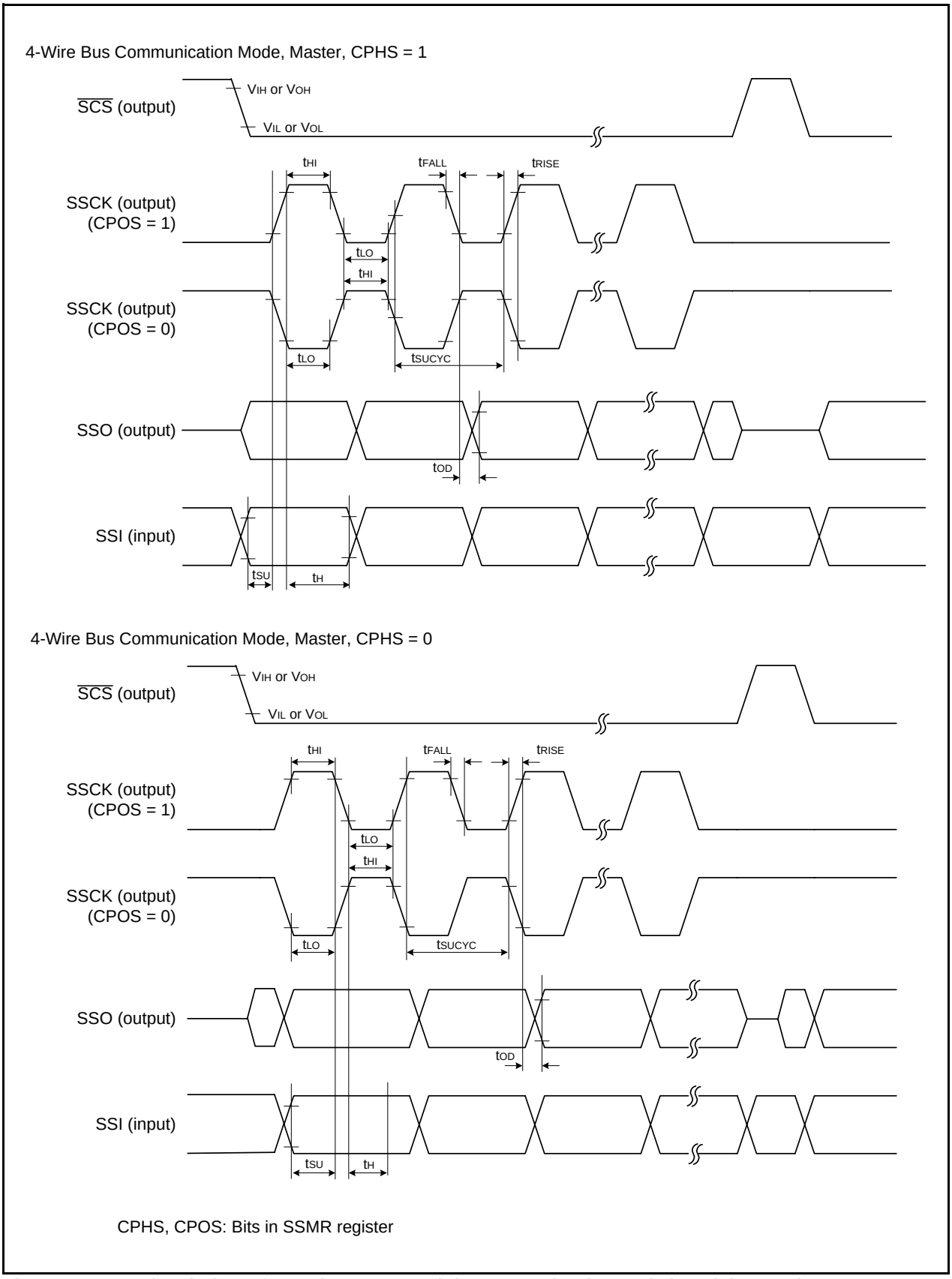


Figure 5.4 I/O Timing of Synchronous Serial Communication Unit (SSU) (Master)

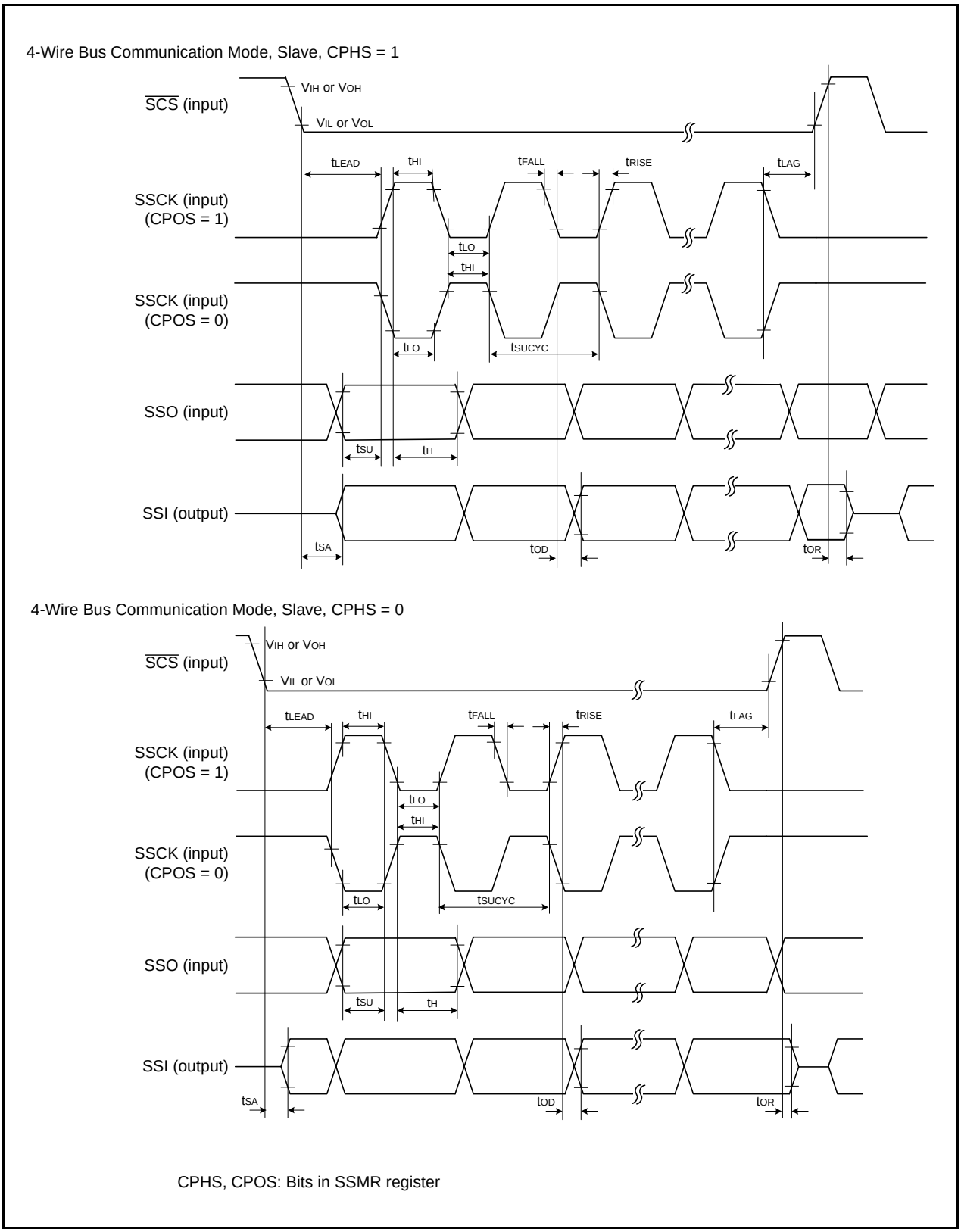
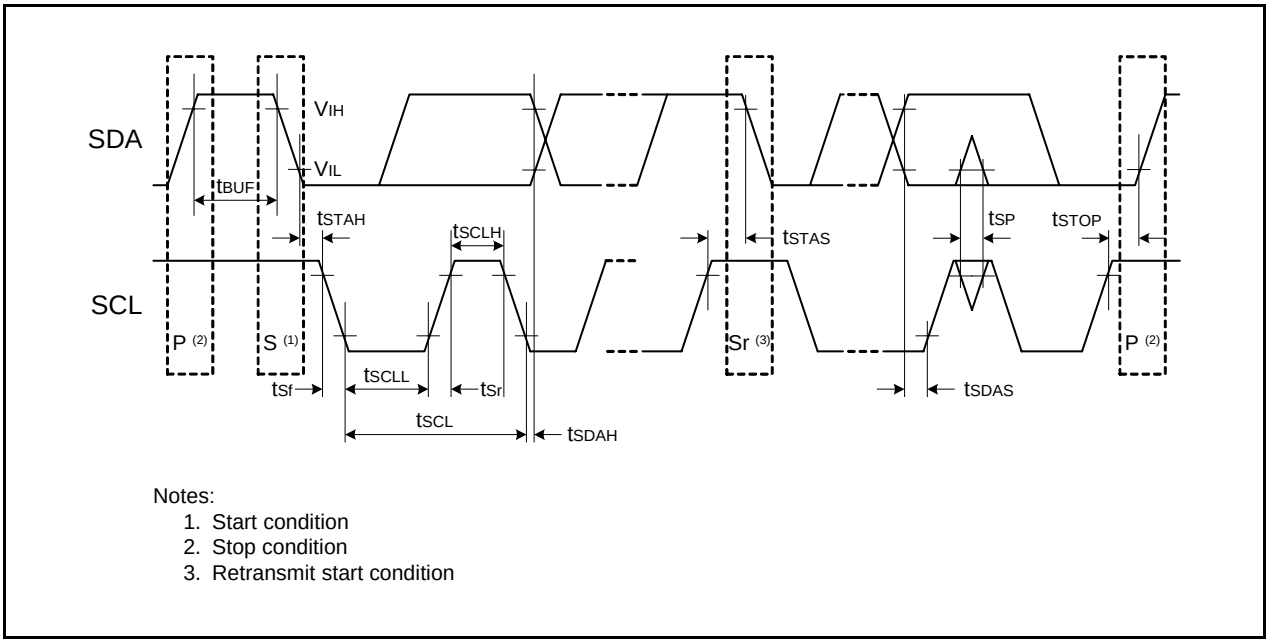


Figure 5.5 I/O Timing of Synchronous Serial Communication Unit (SSU) (Slave)

Table 5.12 Timing Requirements of I²C bus Interface

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t_{SCL}	SCL input cycle time		$12t_{CYC} + 600$ (2)	—	—	ns
t_{SCLH}	SCL input “H” width		$3t_{CYC} + 300$ (2)	—	—	ns
t_{SCLL}	SCL input “L” width		$5t_{CYC} + 500$ (2)	—	—	ns
t_{sf}	SCL, SDA input fall time		—	—	300	ns
t_{SP}	SCL, SDA input spike pulse rejection time		—	—	$1t_{CYC}$ (2)	ns
t_{BUF}	SDA input bus-free time		$5t_{CYC}$ (2)	—	—	ns
t_{STAH}	Start condition input hold time		$3t_{CYC}$ (2)	—	—	ns
t_{STAS}	Retransmit start condition input setup time		$3t_{CYC}$ (2)	—	—	ns
t_{STOP}	Stop condition input setup time		$3t_{CYC}$ (2)	—	—	ns
t_{SDAS}	Data input setup time		$1t_{CYC} + 40$ (2)	—	—	ns
t_{SDAH}	Data input hold time		10	—	—	ns

Notes:
1. V_{CC} = 1.8 V to 3.6 V and T_{opr} = –20°C to 85°C, unless otherwise specified.
2. $1t_{CYC} = 1/f1(s)$



Notes:
1. Start condition
2. Stop condition
3. Retransmit start condition

Figure 5.7 I/O Timing of I²C bus Interface

Table 5.17 External Interrupt $\overline{INTi}$ (i = 0, 1, 3) Input, Key Input Interrupt $\overline{KIi}$ (i = 0 to 7)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input “H” width, $\overline{KIi}$ input “H” width	380 (1)	—	ns
$t_{W(INL)}$	$\overline{INTi}$ input “L” width, $\overline{KIi}$ input “L” width	380 (2)	—	ns

Notes:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

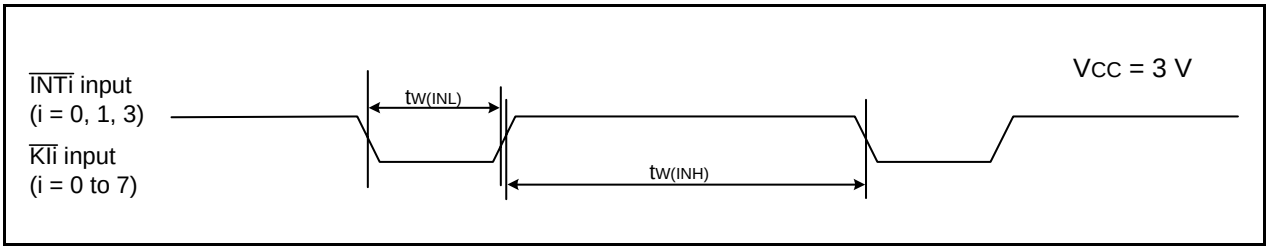
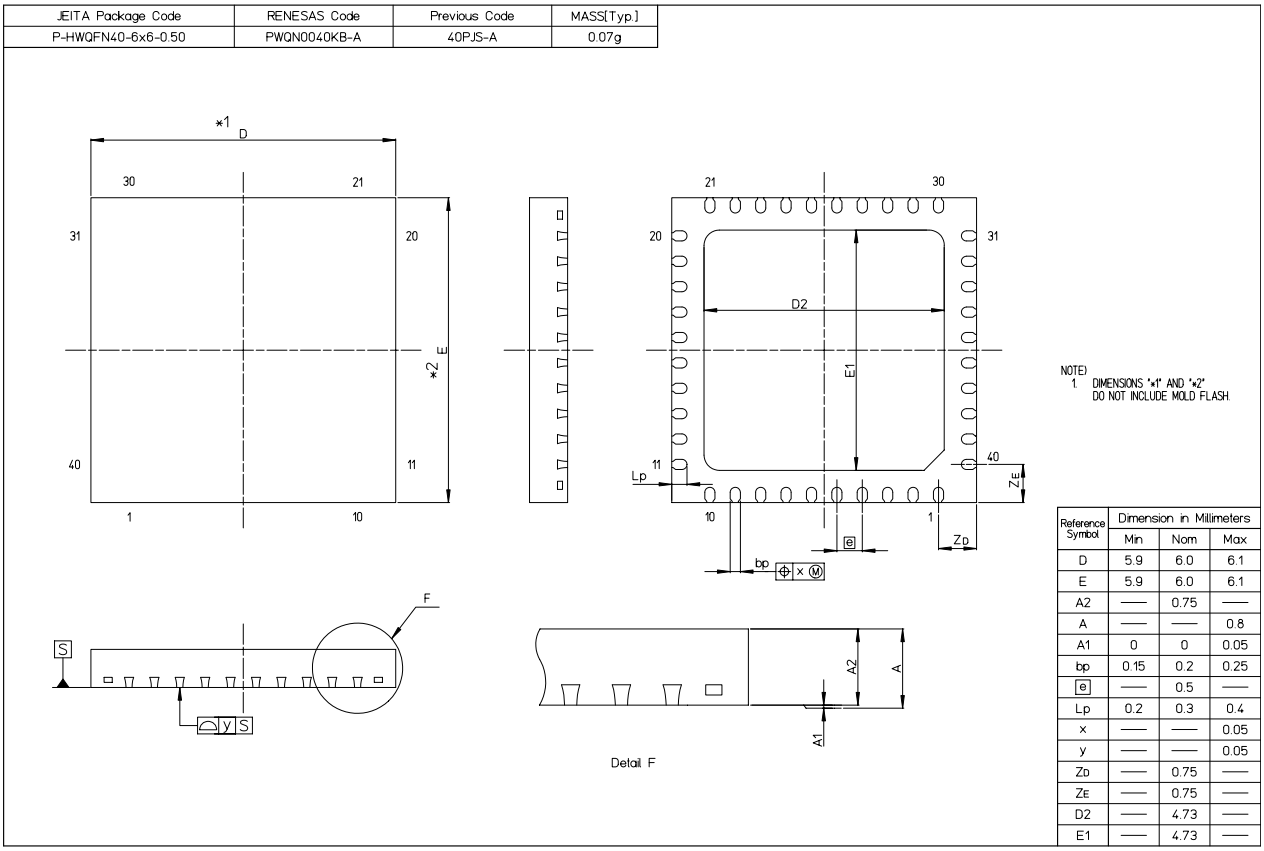


Figure 5.10 Input Timing Diagram for External Interrupt $\overline{INTi}$ and Key Input Interrupt $\overline{KIi}$ when Vcc = 3 V

Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Electronics website.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-HWQFN40-6x6-0.50	PWQN0040KB-A	40PJS-A	0.07g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	5.9	6.0	6.1
E	5.9	6.0	6.1
A2	—	0.75	—
A	—	—	0.8
A1	0	0	0.05
bp	0.15	0.2	0.25
e	—	0.5	—
Lp	0.2	0.3	0.4
x	—	—	0.05
y	—	—	0.05
Zp	—	0.75	—
ZE	—	0.75	—
D2	—	4.73	—
E1	—	4.73	—

REVISION HISTORY	R8C/3MQ Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.10	Nov 19, 2010	—	First Edition issued
1.00	Aug 11, 2011	All pages	“Preliminary”, “Under development” deleted
		4	Table 1.2 revised, Note 1 added
		5	Table 1.3 “(D): Under development”, (P): Under planning” deleted
		6	Figure 1.2 revised
		7	Figure 1.3 revised
		9, 10	Table 1.5, Table 1.6 revised
		12	2.4 revised
		14	3.1 revised
		16, 17	Table 4.2, Table 4.3 revised
		19	Table 4.5 Note 2 added
		20	Table 4.6 revised
		24, 25	Table 4.10, Table 4.11 revised
		32	Table 5.6 revised
		39	Table 5.13 revised
		46	Table 5.22, Table 5.23 revised, Table 5.22 Note 1 added
2.00	Jun 29, 2012	2	Table 1.1 “Voltage detection” revised, Table 1.2 “2.2 V” → “2.15 V”
		3, 4	Tables 1.2 and 1.3 “2.2 V” → “2.15 V”
		5	Table 1.4 and Figure 1.1 revised
		6	Figure 1.2 revised
		14	Figure 3.1 revised
		28	Table 5.2 “2.2 V” → “2.15 V”
		32	Table 5.5 revised, Note 4 added
		39	Table 5.13 “2.2 V” → “2.15 V”
		43	Table 5.18 “2.2 V” → “2.15 V”
		44, 45	Timing requirements, Figures 5.11 to 5.13, titles “2.2 V” → “2.15 V”
		46	Table 5.23 revised

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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