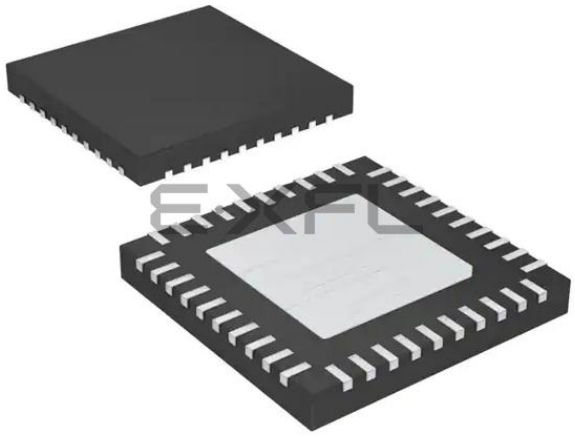
Renesas Electronics America Inc - R5F213M8QNNP#U0 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	R8C
Core Size	16-Bit
Speed	16MHz
Connectivity	I²C, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	18
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-WFQFN Exposed Pad
Supplier Device Package	40-HWQFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f213m8qnnp-u0

1.3 Block Diagram

Figure 1.2 shows a Block Diagram.

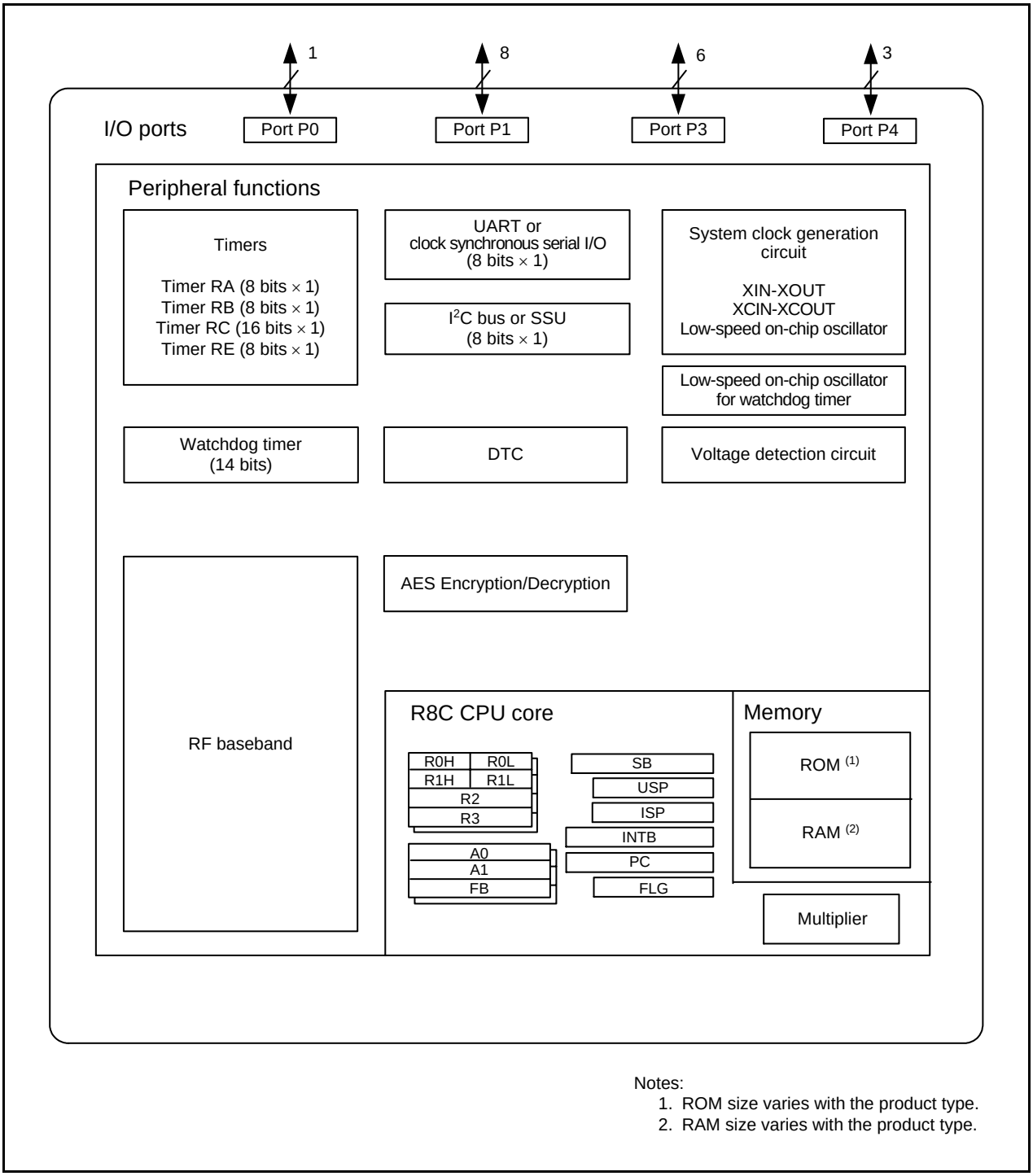
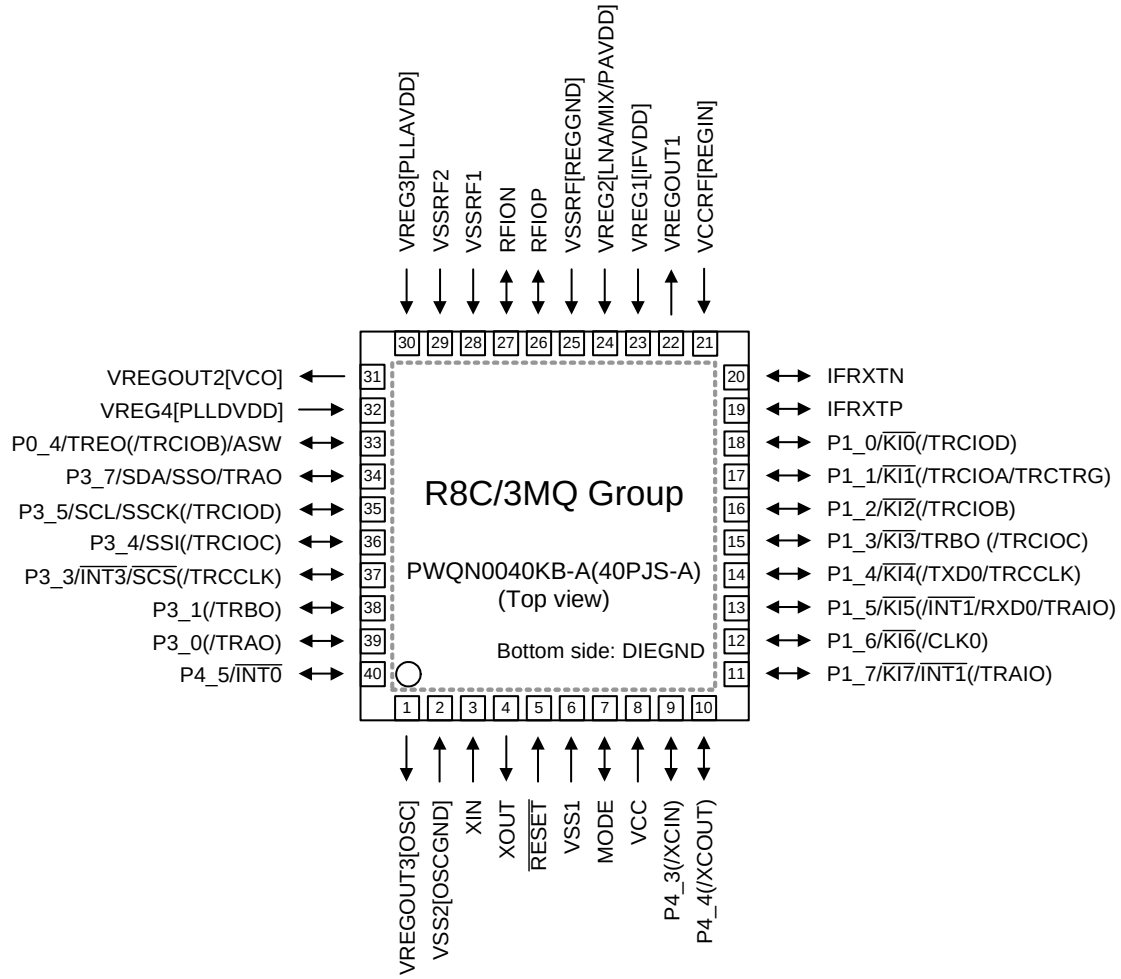


Figure 1.2 Block Diagram

1.4 Pin Assignment

Figure 1.3 shows Pin Assignment (Top View). Table 1.5 outlines Pin Name Information by Pin Number.



Notes:
1. The function in parentheses can be assigned to the pin by a program.
2. [ ] indicates the internal function name related to the pin.
3. Confirm the pin 1 position on the package by referring to the package dimensions.
4. Connect the metal pad (DIEGND) of the package's bottom side to the board's GND side.

Figure 1.3 Pin Assignment (Top View)

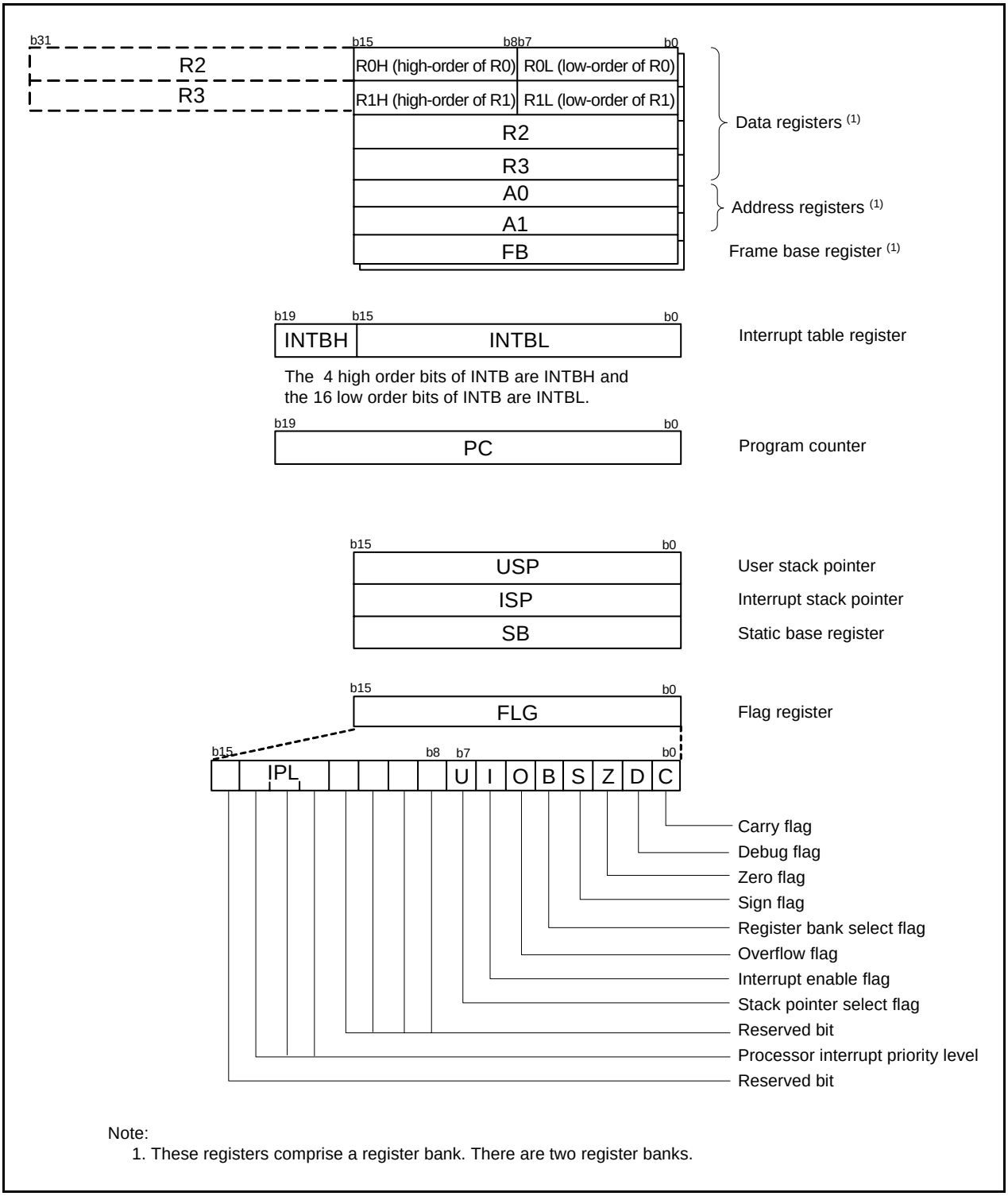
Table 1.5 Pin Name Information by Pin Number

Pin Number	Control Pin	Port	I/O Pin Functions for Peripheral Modules					
			Interrupt	Timer	Serial Interface	SSU	I²C bus	RF Pin Other
1	VREGOUT3							
2	VSS2							
3	XIN							
4	XOUT							
5	$\overline{\text{RESET}}$							
6	VSS1							
7	MODE							
8	VCC							
9	(XCIN)	P4_3						
10	(XCOUT)	P4_4						
11		P1_7	$\overline{\text{KI7}}$/$\overline{\text{INT1}}$	(TRAIO)				
12		P1_6	$\overline{\text{KI6}}$		(CLK0)			
13		P1_5	$\overline{\text{KI5}}$(/$\overline{\text{INT1}}$)	(TRAIO)	(RXD0)			
14		P1_4	$\overline{\text{KI4}}$	(TRCCLK)	(TXD0)			
15		P1_3	$\overline{\text{KI3}}$	TRBO(/TRCIOC)				
16		P1_2	$\overline{\text{KI2}}$	(TRCIOB)				
17		P1_1	$\overline{\text{KI1}}$	(TRCIOA/TRCTRG)				
18		P1_0	$\overline{\text{KI0}}$	(TRCIOD)				
19								IFRXTP
20								IFRXTN
21	VCCRF							
22	VREGOUT1							
23	VREG1							
24	VREG2							
25	VSSRF							
26								RFIOP
27								RFION
28	VSSRF1							
29	VSSRF2							
30	VREG3							
31	VREGOUT2							
32	VREG4							
33		P0_4		TREO(/TRCIOB)				ASW
34		P3_7		TRAO		SSO	SDA	
35		P3_5		(TRCIOD)		SSCK	SCL	
36		P3_4		(TRCIOC)		SSI		
37		P3_3	$\overline{\text{INT3}}$	(TRCCLK)		$\overline{\text{SCS}}$		
38		P3_1		(TRBO)				
39		P3_0		(TRAO)				
40		P4_5	$\overline{\text{INT0}}$					
Bottom side	DIEGND							

Note:
1. The function in parentheses can be assigned to the pin by a program.

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register bank.



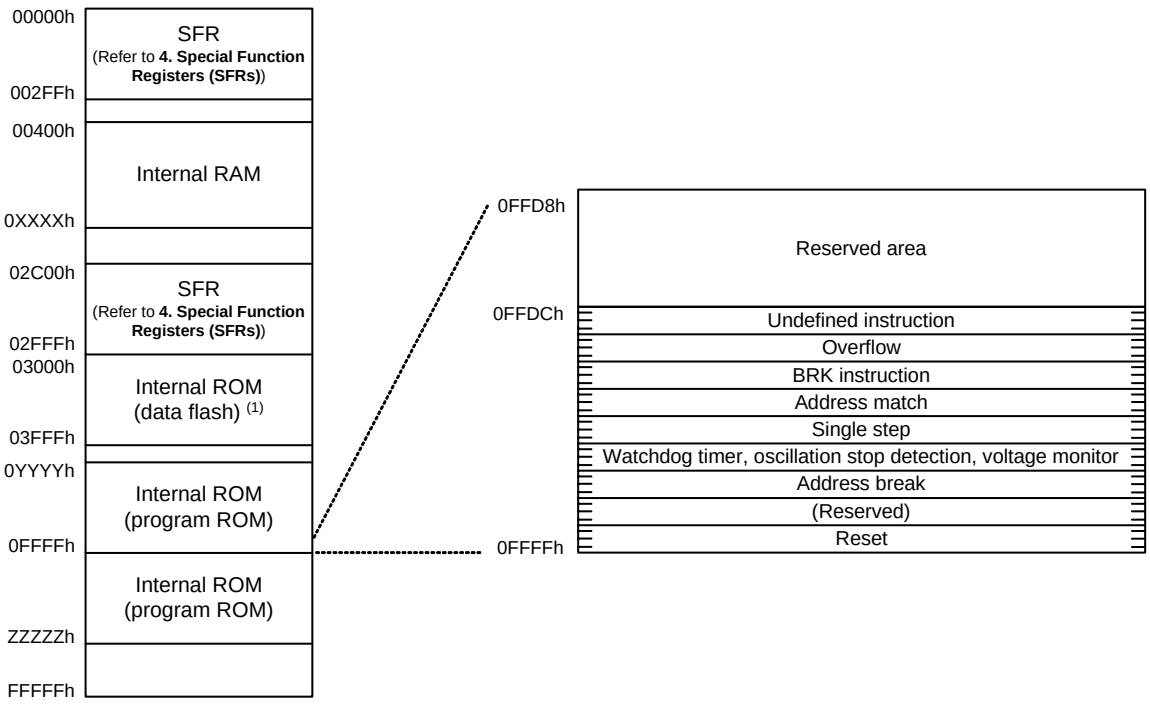
Note:
1. These registers comprise a register bank. There are two register banks.

Figure 2.1 CPU Registers

3. Memory

3.1 R8C/3MQ Group

Figure 3.1 is a Memory Map of R8C/3MQ Group. The R8C/3MQ Group has a 1-Mbyte address space from addresses 00000h to FFFFFh. The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. However, for products with internal ROM (program ROM) capacity of 64 Kbytes or more, the internal ROM is also allocated higher addresses, beginning with address 0FFFFh.
For example, a 32-Kbyte internal ROM area is allocated addresses 08000h to 0FFFFh, and a 96-Kbyte internal ROM is allocated addresses 04000h to 1BFFFh.
The fixed interrupt vector table is allocated addresses 08000h to 0FFFFh. The starting address of each interrupt routine is stored here.
The internal ROM (data flash) is allocated addresses 03000h to 03FFFh.
The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 2.5-Kbyte internal RAM area is allocated addresses 00400h to 00DFFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh and 02C00h to 02FFFh. Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.



Notes:
1. The data flash indicates block A (1 Kbyte), block B (1 Kbyte), block C (1 Kbyte), and block D (1 Kbyte).
2. The blank areas are reserved and cannot be accessed by users. Do not use the data flash as a program area.

Part Number	Internal ROM			Internal RAM	
	Size	Address 0YYYYh	Address ZZZZZh	Size	Address 0XXXXh
R5F213M6QNNP	32 Kbytes	08000h	–	2.5 Kbytes	00DFFh
R5F213M7QNNP	48 Kbytes	04000h	–	4 Kbytes	013FFh
R5F213M8QNNP	64 Kbytes	04000h	13FFFh	6 Kbytes	01BFFh
R5F213MAQNNP	96 Kbytes	04000h	1BFFFh	7 Kbytes	01FFFh
R5F213MCQNNP	112 Kbytes	04000h	1FFFFh	7.5 Kbytes	021FFh

Figure 3.1 Memory Map of R8C/3MQ Group

Table 4.6 SFR Information (6) (01A0h to 02FFh) (1)

Address	Register	Symbol	After Reset
01A0h			
:			
01B0h			
01B1h			
01B2h	Flash Memory Status Register	FST	10000X00b
01B3h			
01B4h	Flash Memory Control Register 0	FMR0	00h
01B5h	Flash Memory Control Register 1	FMR1	00h
01B6h	Flash Memory Control Register 2	FMR2	00h
01B7h			
01B8h			
01B9h			
01BAh			
01BBh			
01BCh			
01BDh			
01BEh			
01BFh			
01C0h	Address Match Interrupt Register 0	RMAD0	XXh
01C1h			XXh
01C2h			0000XXXXb
01C3h	Address Match Interrupt Enable Register 0	AIER0	00h
01C4h	Address Match Interrupt Register 1	RMAD1	XXh
01C5h			XXh
01C6h			0000XXXXb
01C7h	Address Match Interrupt Enable Register 1	AIER1	00h
01C8h			
:			
01DFh			
01E0h	Pull-Up Control Register 0	PUR0	00h
01E1h	Pull-Up Control Register 1	PUR1	00h
01E2h			
01E3h			
01E4h			
01E5h			
01E6h			
01E7h			
01E8h			
01E9h			
01EAh			
01EBh			
01ECh			
01EDh			
01EEh			
01EFh			
01F0h	Port P1 Drive Capacity Control Register	P1DRR	00h
01F1h			
01F2h	Drive Capacity Control Register 0	DRR0	00h
01F3h	Drive Capacity Control Register 1	DRR1	00h
01F4h			
01F5h	Input Threshold Control Register 0	VLT0	00h
01F6h	Input Threshold Control Register 1	VLT1	00h
01F7h			
01F8h			
01F9h			
01FAh	External Input Enable Register 0	INTEN	00h
01FBh			
01FCh	INT Input Filter Select Register 0	INTF	00h
01FDh			
01FEh	Key Input Enable Register 0	KIEN	00h
01FFh	Key Input Enable Register 1	KI1EN	00h
0200h			
:			
02FFh			

X: Undefined

Notes:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.7 SFR Information (7) (2C00h to 2C6Fh) (1)

Address	Register	Symbol	After Reset
2C00h	DTC Transfer Vector Area		XXh
2C01h	DTC Transfer Vector Area		XXh
2C02h	DTC Transfer Vector Area		XXh
2C03h	DTC Transfer Vector Area		XXh
2C04h	DTC Transfer Vector Area		XXh
2C05h	DTC Transfer Vector Area		XXh
2C06h	DTC Transfer Vector Area		XXh
2C07h	DTC Transfer Vector Area		XXh
2C08h	DTC Transfer Vector Area		XXh
2C09h	DTC Transfer Vector Area		XXh
2C0Ah	DTC Transfer Vector Area		XXh
:	DTC Transfer Vector Area		XXh
:	DTC Transfer Vector Area		XXh
2C3Ah	DTC Transfer Vector Area		XXh
2C3Bh	DTC Transfer Vector Area		XXh
2C3Ch	DTC Transfer Vector Area		XXh
2C3Dh	DTC Transfer Vector Area		XXh
2C3Eh	DTC Transfer Vector Area		XXh
2C3Fh	DTC Transfer Vector Area		XXh
2C40h	DTC Control Data 0	DTCD0	XXh
2C41h			XXh
2C42h			XXh
2C43h			XXh
2C44h			XXh
2C45h			XXh
2C46h			XXh
2C47h			XXh
2C48h	DTC Control Data 1	DTCD1	XXh
2C49h			XXh
2C4Ah			XXh
2C4Bh			XXh
2C4Ch			XXh
2C4Dh			XXh
2C4Eh			XXh
2C4Fh			XXh
2C50h	DTC Control Data 2	DTCD2	XXh
2C51h			XXh
2C52h			XXh
2C53h			XXh
2C54h			XXh
2C55h			XXh
2C56h			XXh
2C57h			XXh
2C58h	DTC Control Data 3	DTCD3	XXh
2C59h			XXh
2C5Ah			XXh
2C5Bh			XXh
2C5Ch			XXh
2C5Dh			XXh
2C5Eh			XXh
2C5Fh			XXh
2C60h	DTC Control Data 4	DTCD4	XXh
2C61h			XXh
2C62h			XXh
2C63h			XXh
2C64h			XXh
2C65h			XXh
2C66h			XXh
2C67h			XXh
2C68h	DTC Control Data 5	DTCD5	XXh
2C69h			XXh
2C6Ah			XXh
2C6Bh			XXh
2C6Ch			XXh
2C6Dh			XXh
2C6Eh			XXh
2C6Fh			XXh

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.8 SFR Information (8) (2C70h to 2CAFh) (1)

Address	Register	Symbol	After Reset
2C70h	DTC Control Data 6	DTCD6	XXh
2C71h			XXh
2C72h			XXh
2C73h			XXh
2C74h			XXh
2C75h			XXh
2C76h			XXh
2C77h			XXh
2C78h	DTC Control Data 7	DTCD7	XXh
2C79h			XXh
2C7Ah			XXh
2C7Bh			XXh
2C7Ch			XXh
2C7Dh			XXh
2C7Eh			XXh
2C7Fh			XXh
2C80h	DTC Control Data 8	DTCD8	XXh
2C81h			XXh
2C82h			XXh
2C83h			XXh
2C84h			XXh
2C85h			XXh
2C86h			XXh
2C87h			XXh
2C88h	DTC Control Data 9	DTCD9	XXh
2C89h			XXh
2C8Ah			XXh
2C8Bh			XXh
2C8Ch			XXh
2C8Dh			XXh
2C8Eh			XXh
2C8Fh			XXh
2C90h	DTC Control Data 10	DTCD10	XXh
2C91h			XXh
2C92h			XXh
2C93h			XXh
2C94h			XXh
2C95h			XXh
2C96h			XXh
2C97h			XXh
2C98h	DTC Control Data 11	DTCD11	XXh
2C99h			XXh
2C9Ah			XXh
2C9Bh			XXh
2C9Ch			XXh
2C9Dh			XXh
2C9Eh			XXh
2C9Fh			XXh
2CA0h	DTC Control Data 12	DTCD12	XXh
2CA1h			XXh
2CA2h			XXh
2CA3h			XXh
2CA4h			XXh
2CA5h			XXh
2CA6h			XXh
2CA7h			XXh
2CA8h	DTC Control Data 13	DTCD13	XXh
2CA9h			XXh
2CAAh			XXh
2CABh			XXh
2CACh			XXh
2CADh			XXh
2CAEh			XXh
2CAFh			XXh

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.9 SFR Information (9) (2CB0h to 2CEFh) (1)

Address	Register	Symbol	After Reset
2CB0h	DTC Control Data 14	DTCD14	XXh
2CB1h			XXh
2CB2h			XXh
2CB3h			XXh
2CB4h			XXh
2CB5h			XXh
2CB6h			XXh
2CB7h			XXh
2CB8h	DTC Control Data 15	DTCD15	XXh
2CB9h			XXh
2CBAh			XXh
2CBBh			XXh
2CBCh			XXh
2CBDh			XXh
2CBEh			XXh
2CBFh			XXh
2CC0h	DTC Control Data 16	DTCD16	XXh
2CC1h			XXh
2CC2h			XXh
2CC3h			XXh
2CC4h			XXh
2CC5h			XXh
2CC6h			XXh
2CC7h			XXh
2CC8h	DTC Control Data 17	DTCD17	XXh
2CC9h			XXh
2CCAh			XXh
2CCBh			XXh
2CCCh			XXh
2CCDh			XXh
2CCEh			XXh
2CCFh			XXh
2CD0h	DTC Control Data 18	DTCD18	XXh
2CD1h			XXh
2CD2h			XXh
2CD3h			XXh
2CD4h			XXh
2CD5h			XXh
2CD6h			XXh
2CD7h			XXh
2CD8h	DTC Control Data 19	DTCD19	XXh
2CD9h			XXh
2CDAh			XXh
2CDBh			XXh
2CDCh			XXh
2CDDh			XXh
2CDEh			XXh
2CDFh			XXh
2CE0h	DTC Control Data 20	DTCD20	XXh
2CE1h			XXh
2CE2h			XXh
2CE3h			XXh
2CE4h			XXh
2CE5h			XXh
2CE6h			XXh
2CE7h			XXh
2CE8h	DTC Control Data 21	DTCD21	XXh
2CE9h			XXh
2CEAh			XXh
2CEBh			XXh
2CECh			XXh
2CEDh			XXh
2CEEh			XXh
2CEFh			XXh

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.11 SFR Information (11) (2D30h to 2FFFh) (1)

Address	Register	Symbol	After Reset
2D30h	Time Stamp Register 0	BBTSTAMP0	00h
2D31h			00h
2D32h	Time Stamp Register 1	BBTSTAMP1	00h
2D33h			00h
2D34h	Timer Control Register	BBTIMECON	00h
2D35h	Backoff Period Register	BBBOFFPROD	00h
2D36h			
2D37h			
2D38h			
2D39h			
2D3Ah	PLL Division Register 0	BBPLLDIVL	65h
2D3Bh	PLL Division Register 1	BBPLLDIVH	09h
2D3Ch	Transmit Output Power Register	BBTXOUTPWR	00h
2D3Dh	RSSI Offset Register	BBRSSIOFS	F6h
2D3Eh			
2D3Fh			
2D40h			
:			
2D45h			
2D46h	Automatic ACK Response Timing Adjustment Register	BBACKRTNTIMG	22h
2D47h			
:			
2D63h			
2D64h			
2D65h			
2D66h			
2D67h			
2D68h	Verification Mode Set Register	BBEVAREG	00h
2D69h			
2D6Ah			
2D6Bh			
2D6Ch			
2D6Dh			
2D6Eh			
2D6Fh			
2D70h			
2D71h			
2D72h			
2D73h			
2D74h			
2D75h			
2D76h	IDLE Wait Set Register	BBIDELWAIT	01h
2D77h			
2D78h			
2D79h			
2D7Ah	ANTSW Output Timing Set Register	BBANTSWTIMG	72h
2D7Bh			
2D7Ch	RF Initial Set Register	BBRFINI	XXh
2D7Dh			XXh
2D7Eh			
2D7Fh			
2D80h			
2D81h			
2D82h	ANTSW Control Register	BBANTSWCON	00h
2D83h			
:			
2DFFh			
2E00h	Transmit RAM	TRANSMIT_RAM_START	
:	Transmit RAM		
2E7Eh	Transmit RAM	TRANSMIT_RAM_END	
2E7Fh			
2D80h	Receive RAM	RECIEVE_RAM_START	
:	Receive RAM		
2EFEh	Receive RAM	RECIEVE_RAM_END	
2EFFh			
2F00h			
:			
2FFFh			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.12 ID Code Areas and Option Function Select Area

Address	Area Name	Symbol	After Reset
:			
FFDBh	Option Function Select Register 2	OFS2	(Note 1)
:			
FFDFh	ID1		(Note 2)
:			
FFE3h	ID2		(Note 2)
:			
FFEBh	ID3		(Note 2)
:			
FFEFh	ID4		(Note 2)
:			
FFF3h	ID5		(Note 2)
:			
FFF7h	ID6		(Note 2)
:			
FFFBh	ID7		(Note 2)
:			
FFFFh	Option Function Select Register	OFS	(Note 1)

Notes:
1. The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the option function select area. If the block including the option function select area is erased, the option function select area is set to FFh.
   At shipment, the option function select area is set to FFh. It is set to the written value after written by the user.
2. The ID code areas are allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the ID code areas. If the block including the ID code areas is erased, the ID code areas are set to FFh.
   At shipment, the ID code areas are set to FFh. They are set to the written value after written by the user.

Table 5.2 Recommended Operating Conditions (1)

Symbol	Parameter				Conditions	Standard			Unit
						Min.	Typ.	Max.	
VCC	Digital supply voltage	(1) During MCU operation under the conditions other than (2) and (3) below.				1.8	3.3	3.6	V
		(2) During programming and erasing of the flash memory using a serial programmer or parallel programmer.				2.7	—	3.6	
		(3) During on-chip debugging with the E8a emulator connected				2.7	—	3.6	
VCCRF	Analog supply voltage					1.8	3.3	3.6	V
VSS/ VSS2/ VSSRF/ VSSRF1/ VSSRF2/ DIEGND	Supply voltage	VSS1, VSS2, VSSRF, VSSRF1, VSSRF2, DIEGND				—	0	—	V
V_{IH}	Input “H” voltage	Other than CMOS input				0.8 Vcc	—	Vcc	V
		CMOS input	Input level switching function (I/O port)	Input level selection: 0.35 Vcc	2.7 V ≤ Vcc ≤ 3.6 V	0.55 Vcc	—	Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0.65 Vcc	—	Vcc	V
				Input level selection: 0.5 Vcc	2.7 V ≤ Vcc ≤ 3.6 V	0.7 Vcc	—	Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0.8 Vcc	—	Vcc	V
				Input level selection: 0.7 Vcc	2.7 V ≤ Vcc ≤ 3.6 V	0.85 Vcc	—	Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0.85 Vcc	—	Vcc	V
V_{IL}	Input “L” voltage	Other than CMOS input				0	—	0.2 Vcc	V
		CMOS input	Input level switching function (I/O port)	Input level selection: 0.35 Vcc	2.7 V ≤ Vcc ≤ 3.6 V	0	—	0.2 Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0	—	0.2 Vcc	V
				Input level selection: 0.5 Vcc	2.7 V ≤ Vcc ≤ 3.6 V	0	—	0.3 Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0	—	0.2 Vcc	V
				Input level selection: 0.7 Vcc	2.7 V ≤ Vcc ≤ 3.6 V	0	—	0.45 Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0	—	0.35 Vcc	V
$I_{OH(sum)}$	Peak sum output “H” current	Sum of all pins $I_{OH(peak)}$				—	—	−160	mA
$I_{OH(sum)}$	Average sum output “H” current	Sum of all pins $I_{OH(avg)}$				—	—	−80	mA
$I_{OH(peak)}$	Peak output “H” current	Drive capacity Low				—	—	−10	mA
		Drive capacity High				—	—	−40	mA
$I_{OH(avg)}$	Average output “H” current	Drive capacity Low				—	—	−5	mA
		Drive capacity High				—	—	−20	mA
$I_{OL(sum)}$	Peak sum output “L” current	Sum of all pins $I_{OL(peak)}$				—	—	160	mA
$I_{OL(sum)}$	Average sum output “L” current	Sum of all pins $I_{OL(avg)}$				—	—	80	mA
$I_{OL(peak)}$	Peak output “L” current	Drive capacity Low				—	—	10	mA
		Drive capacity High				—	—	40	mA
$I_{OL(avg)}$	Average output “L” current	Drive capacity Low				—	—	5	mA
		Drive capacity High				—	—	20	mA
$f_{(XIN)}$	XIN clock input oscillation frequency				1.8 V ≤ Vcc ≤ 3.6 V	—	16	—	MHz
$f_{(XCIN)}$	XCIN clock input oscillation frequency				1.8 V ≤ Vcc ≤ 3.6 V	30	32.768	35	kHz
—	System clock frequency	f(XIN)=16 MHz			1.8 V ≤ Vcc ≤ 3.6 V	—	—	16	MHz
$f_{(BCLK)}$	CPU clock frequency	f(XIN)=16 MHz			2.7 V ≤ Vcc ≤ 3.6 V	—	—	16	MHz
					2.15 V ≤ Vcc < 2.7 V	—	—	8	
					1.8 V ≤ Vcc < 2.15 V	—	—	4	

Notes:
1. Vcc = 1.8 to 3.6 V and T_{opr} = −20°C to 85°C, unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.

Table 5.4 Flash Memory (Data flash Block A to Block D) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
—	Program/erase endurance (2)		10,000 (3)	—	—	times
—	Byte program time (program/erase endurance ≤ 1,000 times)		—	160	1500	µs
—	Byte program time (program/erase endurance > 1,000 times)		—	300	1500	µs
—	Block erase time (program/erase endurance ≤ 1,000 times)		—	0.2	1	s
—	Block erase time (program/erase endurance > 1,000 times)		—	0.3	1	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		—	—	5 + CPU clock × 3 cycles	ms
—	Interval from erase start/restart until following suspend request		0	—	—	µs
—	Time from suspend until erase restart		—	—	30 + CPU clock × 1 cycle	µs
$t_{d(CMDRST-READY)}$	Time from when command is forcibly stopped until reading is enabled		—	—	30 + CPU clock × 1 cycle	µs
—	Program, erase voltage	CPU rewrite mode	1.8	—	3.6	V
		Standard serial I/O mode	2.7	—	3.6	
		Parallel I/O mode	2.7	—	3.6	
—	Read voltage		1.8	—	3.6	V
—	Program, erase temperature	CPU rewrite mode	−20	—	85	°C
		Standard serial I/O mode	0	—	60	
		Parallel I/O mode	0	—	60	
—	Data hold time (7)	Ambient temperature = 55°C	20	—	—	year

Notes:
1. V_{CC} = 1.8 to 3.6 V and T_{opr} = −20°C to 85°C, unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one. However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed.)
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the erasure endurance between blocks A to D can further reduce the actual erasure endurance. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

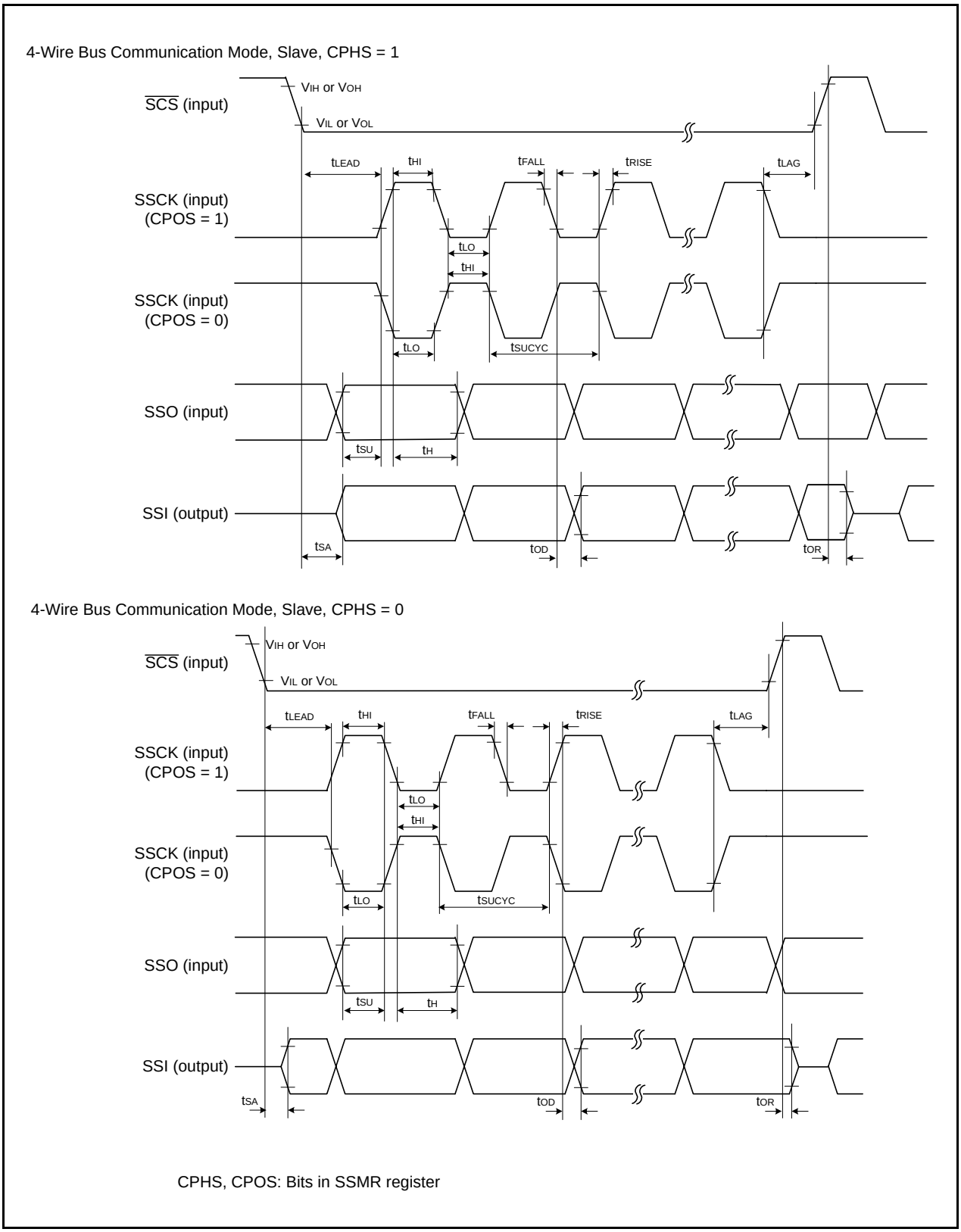


Figure 5.5 I/O Timing of Synchronous Serial Communication Unit (SSU) (Slave)

Table 5.14 Electrical Characteristics (2) [2.7 V ≤ Vcc ≤ 3.6 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” voltage	P0_4, P1, P3_0, P3_1, P3_3 to P3_5, P3_7, P4_3 to P4_5	Drive capacity High	I_{OH} = –5 mA	V_{CC} – 0.5	—	V_{CC}	V
			Drive capacity Low	I_{OH} = –1 mA	V_{CC} – 0.5	—	V_{CC}	V
V_{OL}	Output “L” voltage	P0_4, P1, P3_0, P3_1, P3_3 to P3_5, P3_7, P4_3 to P4_5	Drive capacity High	I_{OL} = 5 mA	—	—	0.5	V
			Drive capacity Low	I_{OL} = 1 mA	—	—	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, $\overline{KI4}$, $\overline{KI6}$, $\overline{KI7}$, TRAIO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRCTRG, TRCCLK, RXD0, CLK0, SSI, SCL, SDA, SSO	VCC = 3.0 V		0.1	0.4	—	V
		$\overline{RESET}$	VCC = 3.0 V		0.1	0.5	—	V
I_{IH}	Input “H” current		V_I = 3 V, V_{CC} = 3.0 V		—	—	4.0	µA
I_{IL}	Input “L” current		V_I = 0 V, V_{CC} = 3.0 V		—	—	–4.0	µA
R_{PULLUP}	Pull-up resistance		V_I = 0 V, V_{CC} = 3.0 V		42	84	168	kΩ
R_{fXIN}	Feedback resistance	XIN			—	0.3	—	MΩ
R_{fXCIN}	Feedback resistance	XCIN			—	8	—	MΩ
V_{RAM}	RAM hold voltage		During stop mode		1.8	—	3.6	V

Note:
1. 2.7 V ≤ V_{CC} ≤ 3.6 V, T_{opr} = –20°C to 85°C, and f(XIN) =16 MHz, unless otherwise specified.

Timing requirements (VCC = 3 V, Topr = −20°C to 85°C, unless otherwise specified)

Table 5.15 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	300	—	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	120	—	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	120	—	ns

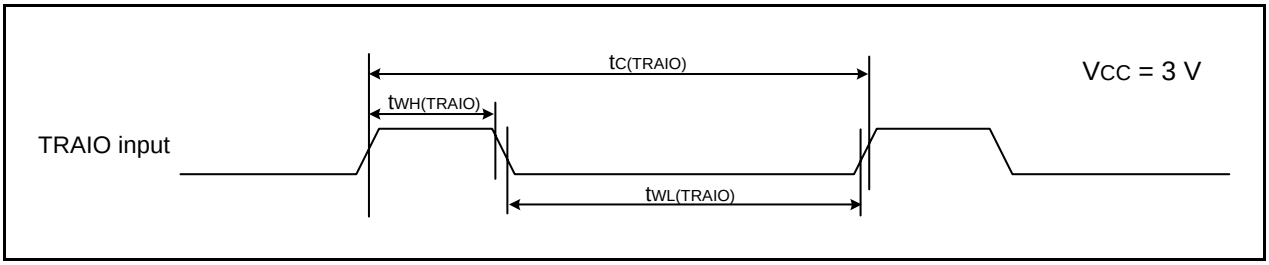


Figure 5.8 TRAIO Input Timing Diagram when VCC = 3 V

Table 5.16 Serial Interface

Symbol	Parameter		Standard		Unit
			Min.	Max.	
$t_{c(CK)}$	CLK0 input cycle time	When an external clock is selected	300	—	ns
$t_{W(CKH)}$	CLK0 input “H” width		150	—	ns
$t_{W(CKL)}$	CLK0 Input “L” width		150	—	ns
$t_{d(C-Q)}$	TXD0 output delay time		—	120	ns
$t_{h(C-Q)}$	TXD0 hold time		0	—	ns
$t_{su(D-C)}$	RXD0 input setup time		30	—	ns
$t_{h(C-D)}$	RXD0 input hold time		90	—	ns
$t_{h(C-Q)}$	TXD0 output delay time	When an internal clock is selected	—	30	ns
$t_{su(D-C)}$	RXD0 input setup time		120	—	ns
$t_{h(C-D)}$	RXD0 input hold time		90	—	ns

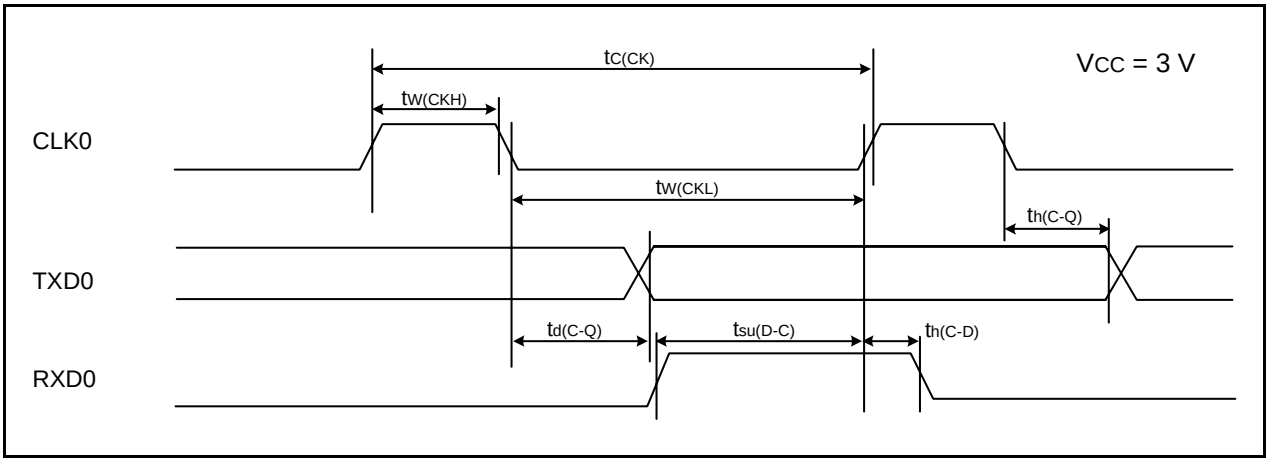


Figure 5.9 Serial Interface Timing Diagram when VCC = 3 V

Timing requirements (VCC = 2.15 V, Topr = –20°C to 85°C, unless otherwise specified)

Table 5.19 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	500	—	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	200	—	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	200	—	ns

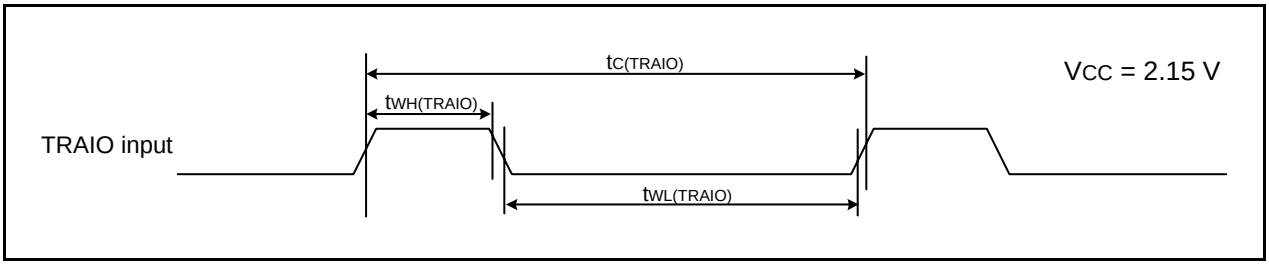


Figure 5.11 TRAIO Input Timing Diagram when VCC = 2.15 V

Table 5.20 Serial Interface

Symbol	Parameter		Standard		Unit
			Min.	Max.	
$t_{c(CK)}$	CLK0 input cycle time	When an external clock is selected	800	—	ns
$t_{W(CKH)}$	CLK0 input “H” width		400	—	ns
$t_{W(CKL)}$	CLK0 input “L” width		400	—	ns
$t_{d(C-Q)}$	TXD0 output delay time		—	200	ns
$t_{h(C-Q)}$	TXD0 hold time		0	—	ns
$t_{su(D-C)}$	RXD0 input setup time		150	—	ns
$t_{h(C-D)}$	RXD0 input hold time		90	—	ns
$t_{h(C-Q)}$	TXD0 output delay time	When an internal clock is selected	—	200	ns
$t_{su(D-C)}$	RXD0 input setup time		150	—	ns
$t_{h(C-D)}$	RXD0 input hold time		90	—	ns

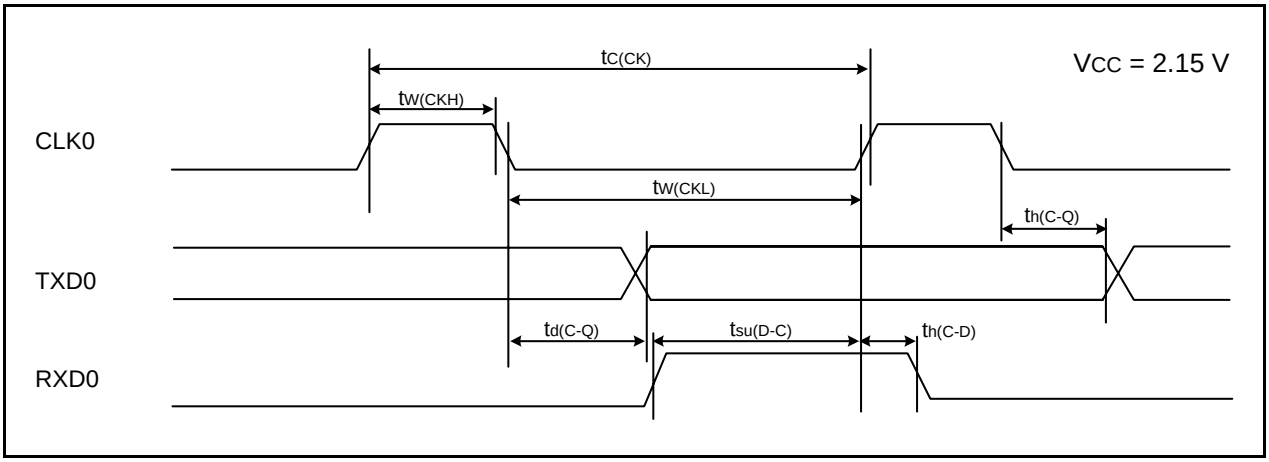
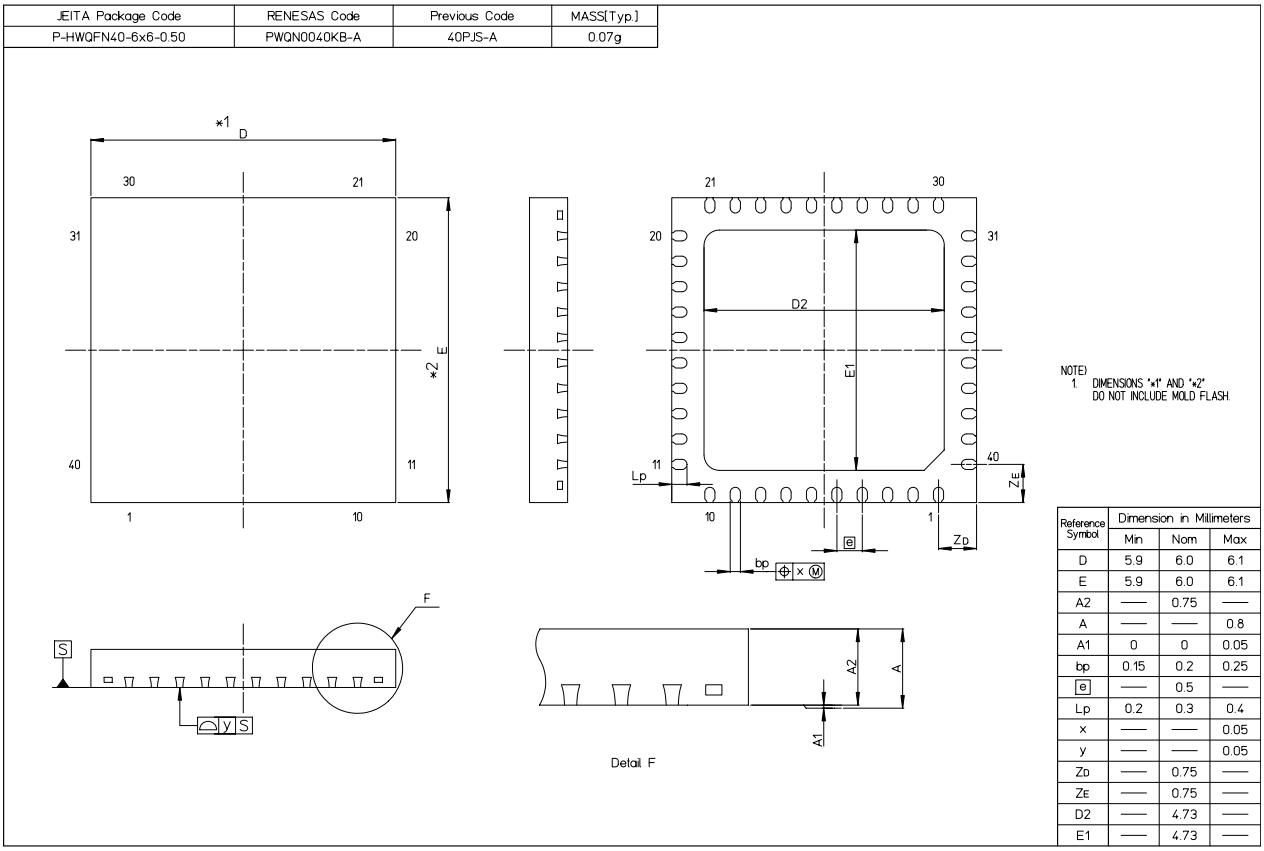


Figure 5.12 Serial Interface Timing Diagram when VCC = 2.15 V

Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Electronics website.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-HWQFN40-6x6-0.50	PWQN0040KB-A	40PJS-A	0.07g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	5.9	6.0	6.1
E	5.9	6.0	6.1
A2	—	0.75	—
A	—	—	0.8
A1	0	0	0.05
bp	0.15	0.2	0.25
e	—	0.5	—
Lp	0.2	0.3	0.4
x	—	—	0.05
y	—	—	0.05
Zp	—	0.75	—
ZE	—	0.75	—
D2	—	4.73	—
E1	—	4.73	—

REVISION HISTORY	R8C/3MQ Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.10	Nov 19, 2010	—	First Edition issued
1.00	Aug 11, 2011	All pages	“Preliminary”, “Under development” deleted
		4	Table 1.2 revised, Note 1 added
		5	Table 1.3 “(D): Under development”, (P): Under planning” deleted
		6	Figure 1.2 revised
		7	Figure 1.3 revised
		9, 10	Table 1.5, Table 1.6 revised
		12	2.4 revised
		14	3.1 revised
		16, 17	Table 4.2, Table 4.3 revised
		19	Table 4.5 Note 2 added
		20	Table 4.6 revised
		24, 25	Table 4.10, Table 4.11 revised
		32	Table 5.6 revised
		39	Table 5.13 revised
		46	Table 5.22, Table 5.23 revised, Table 5.22 Note 1 added
2.00	Jun 29, 2012	2	Table 1.1 “Voltage detection” revised, Table 1.2 “2.2 V” → “2.15 V”
		3, 4	Tables 1.2 and 1.3 “2.2 V” → “2.15 V”
		5	Table 1.4 and Figure 1.1 revised
		6	Figure 1.2 revised
		14	Figure 3.1 revised
		28	Table 5.2 “2.2 V” → “2.15 V”
		32	Table 5.5 revised, Note 4 added
		39	Table 5.13 “2.2 V” → “2.15 V”
		43	Table 5.18 “2.2 V” → “2.15 V”
		44, 45	Timing requirements, Figures 5.11 to 5.13, titles “2.2 V” → “2.15 V”
		46	Table 5.23 revised

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