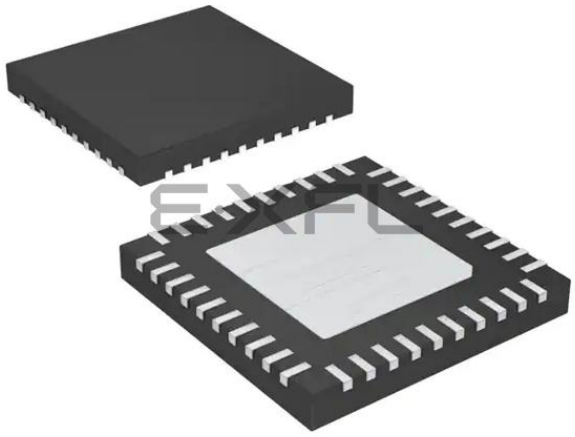
Renesas Electronics America Inc - R5F213MAQNNP#U0 Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	R8C
Core Size	16-Bit
Speed	16MHz
Connectivity	I²C, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	18
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	7K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-WFQFN Exposed Pad
Supplier Device Package	40-HWQFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f213maqnnp-u0

1.1.2 Specifications

Tables 1.1 and 1.2 outline the Specifications for R8C/3MQ Group.

Table 1.1 Specifications for R8C/3MQ Group (1)

Item	Function	Specification
CPU	Central processing unit	R8C CPU core • Number of fundamental instructions: 89 • Minimum instruction execution time: 62.5 ns (f(BCLK) = 16 MHz, VCC = 2.7 to 3.6 V) 125 ns (f(BCLK) = 8 MHz, VCC = 2.15 to 3.6 V) 250 ns (f(BCLK) = 4 MHz, VCC = 1.8 to 3.6 V) • Multiplier: 16 bits × 16 bits → 32 bits • Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits • Operation mode: Single-chip mode (address space: 1 Mbyte)
Memory	ROM, RAM, Data flash	Refer to **Table 1.4 Product List for R8C/3MQ Group**.
Power Supply Voltage Detection	Voltage detection circuit	• Power-on reset • Voltage detection 2 (detection level selectable)
I/O Ports	Programmable I/O ports	CMOS I/O ports: 18 (including XCIN and XCOUT), selectable pull-up resistor (for some ports)
Clock	Clock generation circuits	• 3 circuits: XIN clock oscillation circuit, XCIN clock oscillation circuit (32 kHz), Low-speed on-chip oscillator • Oscillation stop detection: XIN clock oscillation stop detection function • Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16 • Low power consumption modes: Standard operating mode (high-speed clock, low-speed clock, low-speed on-chip oscillator), wait mode, stop mode
		Real-time clock (timer RE)
Interrupts		• Interrupt Vectors: 69 • External: 11 sources ($\overline{\text{INT}}$ × 3, key input × 8) • Priority levels: 7 levels
Watchdog Timer		• 14 bits × 1 (with prescaler) • Reset start selectable • Low-speed on-chip oscillator for watchdog timer selectable
DTC (Data Transfer Controller)		• 1 channel • Activation sources: 17 • Transfer modes: 2 (normal mode, repeat mode)
Timer	Timer RA	8 bits × 1 (with 8-bit prescaler) Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
	Timer RB	8 bits × 1 (with 8-bit prescaler) Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode
	Timer RC	16 bits × 1 (with 4 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output 3 pins), PWM2 mode (PWM output pin)
	Timer RE	8 bits × 1 Real-time clock mode (count seconds, minutes, hours, days of week), output compare mode

Table 1.2 Specifications for R8C/3MQ Group (2)

Item	Function	Specification
Serial Interface (UART0)		Shared with clock synchronous serial I/O mode and clock asynchronous serial I/O
Synchronous Serial Communication Unit (SSU)		1 (shared with I²C bus)
I²C bus		1 (shared with SSU)
RF	RF frequency	2405 MHz to 2480 MHz
	Reception sensitivity	-95 dBm
	Transmission output level	0 dBm
Baseband		• 127-byte transmit RAM, 127-byte receive RAM × 2 • Automatic ACK response function • 26-bit timer: Compare function in 3 channels
Encryption	AES	AES Encryption/Decryption (Key length 128bits)
Flash Memory		• Programming and erasure voltage: VCC = 1.8 to 3.6 V (in CPU rewrite mode) • Programming and erasure endurance: 10,000 times (data flash) 1,000 times (program ROM) • Program security: ROM code protect, ID code check • Debug functions: On-chip debug, on-board flash rewrite function • Background operation (BGO) function
Operating Frequency/ Supply Voltage (in single mode)		f(BCLK) = 16 MHz, VCC = 2.7 to 3.6 V) f(BCLK) = 8 MHz (VCC = 2.15 to 3.6V) f(BCLK) = 4 MHz, VCC = 1.8 to 3.6 V) Note: f(XIN) = fixed at 16 MHz

1.2 Product List

Table 1.4 lists Product List for R8C/3MQ Group. Figure 1.1 shows a Part Number, Memory Size, and Package of R8C/3MQ Group.

Table 1.4 Product List for R8C/3MQ Group **Current of Jun 2012**

Part No.	ROM Capacity		RAM Capacity	Package Type	Remarks
	Program ROM	Data flash			
R5F213M6QNNP	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PWQN0040KB-A	N version
R5F213M7QNNP	48 Kbytes	1 Kbyte × 4	4 Kbytes		
R5F213M8QNNP	64 Kbytes	1 Kbyte × 4	6 Kbytes		
R5F213MAQNNP	96 Kbytes	1 Kbyte × 4	7 Kbytes		
R5F213MCQNNP	112 Kbytes	1 Kbyte × 4	7.5 Kbytes		

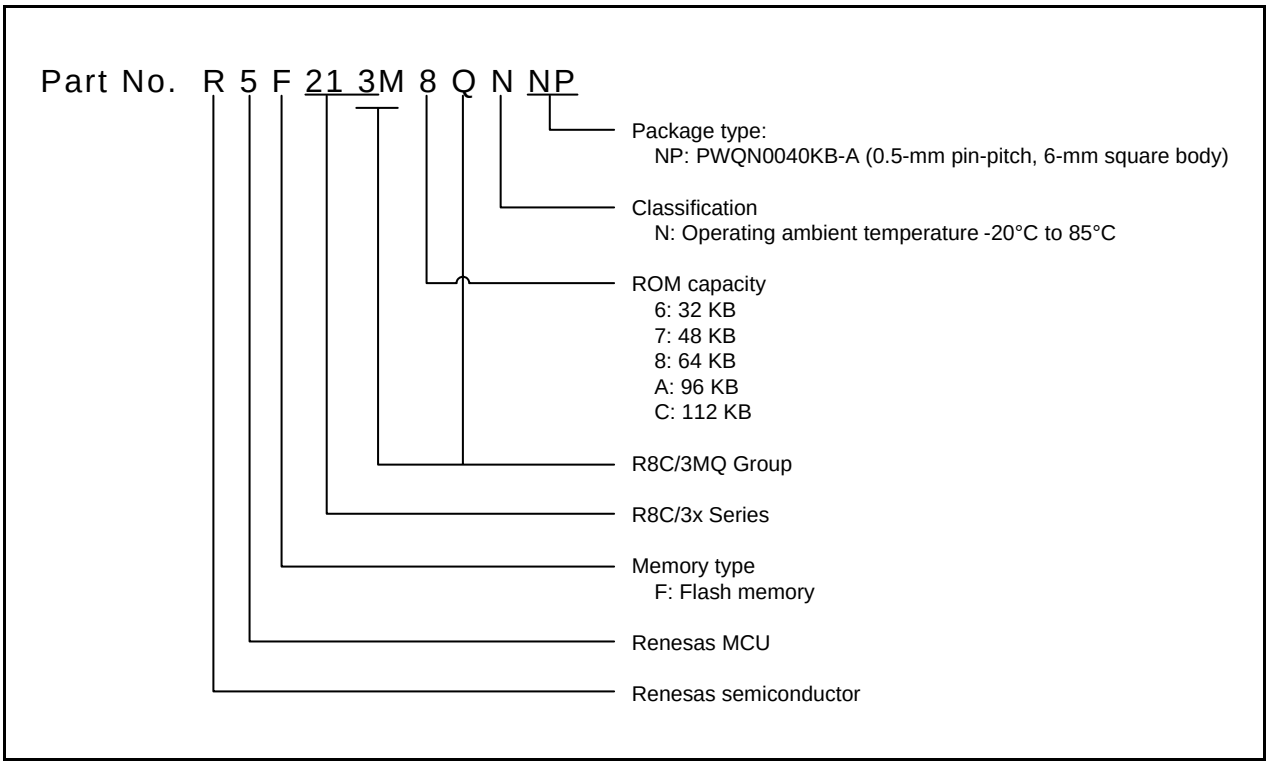
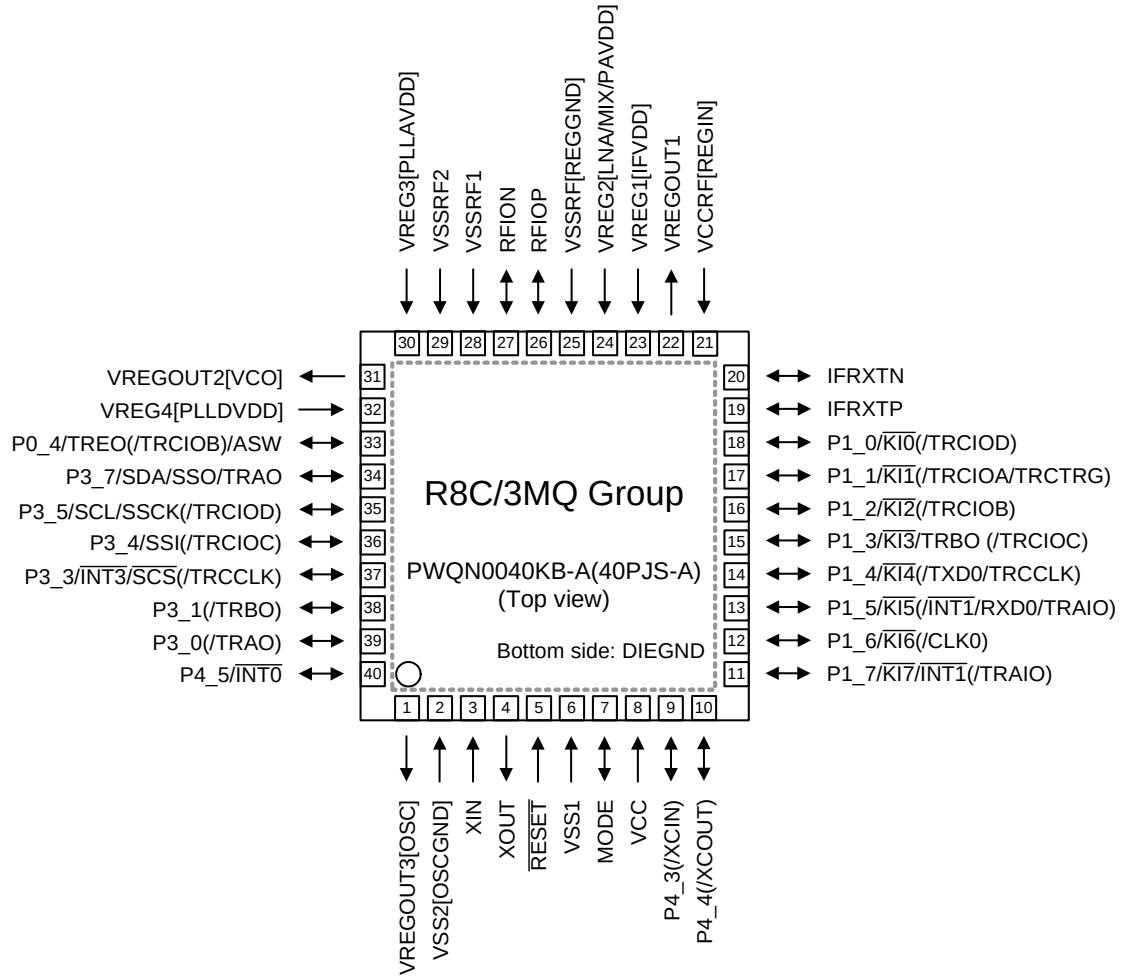


Figure 1.1 Part Number, Memory Size, and Package of R8C/3MQ Group

1.4 Pin Assignment

Figure 1.3 shows Pin Assignment (Top View). Table 1.5 outlines Pin Name Information by Pin Number.



Notes:
1. The function in parentheses can be assigned to the pin by a program.
2. [ ] indicates the internal function name related to the pin.
3. Confirm the pin 1 position on the package by referring to the package dimensions.
4. Connect the metal pad (DIEGND) of the package's bottom side to the board's GND side.

Figure 1.3 Pin Assignment (Top View)

Table 1.7 Pin Functions (2)

Item	Pin Name	I/O Type	Description
Analog power supply input	VCCRF, VSSRF, VSSRF1, VSSRF2, VSS2, DIEGND	—	Apply the same voltage as the VCC of 1.8 V to 3.6 V to VCCRF. Apply 0 V to VSSRF, VSSRF1, VSSRF2, VSS2, and DIEGND.
	VREG1	—	1.5 V IF VDD pin. Connect to the VREGOUT1 pin.
	VREG2	—	1.5 V LNA/MIX/PA VDD pin. Connect to the VREGOUT1 pin.
	VREG3	—	1.5 V PLL ANALOG VDD pin. Connect to the VREGOUT1 pin.
	VREG4	—	1.5 V PLL DIGITAL VDD pin. Connect to the VREGOUT1 pin.
Regulator output	VREGOUT1	—	On-chip regulator output (1.5 V) pin for the analog circuit. Connect only a bypass capacitor between pins VREGOUT1 and VSS. Use only as the power supply for pins VREG1, VREG2, VREG3, and VREGF4.
	VREGOUT2	—	Regulator output (1.5 V) pin for the VCO circuit. Connect only a bypass capacitor between pins VREGOUT2 and VSS. Do not use as the power supply for other circuits.
	VREGOUT3	—	Regulator output (1.5 V) pin for the XIN oscillation circuit. Connect only a bypass capacitor between pins VREGOUT3 and VSS. Do not use as the power supply for other circuits.
RF I/O	RFIOP, RFION	I/O	RF I/O pins
Test pins	IFRXTN, IFRXTP	I/O	Ports for testing. Leave open or apply 0 V.
External antenna switch control output	ASW	O	Signal output pin to control the external antenna switch. If antenna switch control is not required, leave open.

I: Input O: Output I/O: Input and output

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the starting address of a relocatable interrupt vector table.

2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.
Interrupts are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.
The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has higher priority than IPL, the interrupt is enabled.

2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.11 list the special function registers. Table 4.12 lists the ID Code Areas and Option Function Select Area.

Table 4.1 SFR Information (1) (0000h to 002Fh) (1)

Address	Register	Symbol	After Reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	00101000b
0007h	System Clock Control Register 1	CM1	00101000b
0008h	Module Standby Control Register	MSTCR	00h
0009h	System Clock Control Register 3	CM3	00h
000Ah	Protect Register	PRCR	00h
000Bh	Reset Source Determination Register	RSTFR	0XXXXXXXb (2)
000Ch	Oscillation Stop Detection Register	OCD	00000100b
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDTC	00111111b
0010h			
0011h			
0012h			
0013h			
0014h			
0015h			
0016h			
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	00h 10000000b (3)
001Dh			
001Eh			
001Fh			
0020h			
0021h			
0022h			
0023h			
0024h			
0025h			
0026h			
0027h			
0028h	Clock Prescaler Reset Flag	CPSRF	00h
0029h			
002Ah			
002Bh			
002Ch			
002Dh			
002Eh			
002Fh			

X: Undefined

Notes:

1. The blank areas are reserved and cannot be accessed by users.
2. The CWR bit in the RSTFR register is set to 0 after power-on and voltage monitor 0 reset. Hardware reset, software reset, or watchdog timer reset does not affect this bit.
3. The CSPROINI bit in the OFS register is set to 0.

Table 4.2 SFR Information (2) (0030h to 006Fh) (1)

Address	Register	Symbol	After Reset
0030h	Voltage Monitor Circuit Control Register	CMPA	00h
0031h	Voltage Monitor Circuit Edge Select Register	VCAC	00h
0032h			
0033h			
0034h	Voltage detection Register 2	VCA2	00h (3) 00100000b (4)
0035h			
0036h	Voltage Detection 1 Level Select Register	VD1LS	00000111b
0037h			
0038h	Voltage Monitor 0 Circuit Control Register	VW0C	1100X010b (3) 1100X011b (4)
0039h	Voltage Monitor 1 Circuit Control Register	VW1C	10001010b
003Ah	WDT Detection Flag	VW2C	10000010b
003Bh			
003Ch			
003Dh			
003Eh			
003Fh			
0040h			
0041h	Flash Memory Ready Interrupt Control Register	FMRDYIC	XXXXX000b
0042h	BB Timer Compare 2 Interrupt Control Register	BBTIM2IC	XXXXX000b
0043h			
0044h			
0045h			
0046h			
0047h	Timer RC Interrupt Control Register	TRCIC	XXXXX000b
0048h			
0049h			
004Ah	Timer RE Interrupt Control Register	TREIC	XXXXX000b
004Bh			
004Ch			
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh			
004Fh	SSU Interrupt Control Register/IIC bus Interrupt Control Register (2)	SSUIC/IICIC	XXXXX000b
0050h			
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXXX000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXXX000b
0053h			
0054h	Bank 0 Reception Complete/IDLE Interrupt Control Register (5)	BBRX0IC/BBIDELIC	XXXXX000b
0055h			
0056h	Timer RA Interrupt Control Register	TRAIC	XXXXX000b
0057h			
0058h	Timer RB Interrupt Control Register	TRBIC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Ah	INT3 Interrupt Control Register	INT3IC	XX00X000b
005Bh			
005Ch	BB Timer Compare 1 Interrupt Control Register	BBTIM1IC	XX00X000b
005Dh	INT0 Interrupt Control Register	INT0IC	XX00X000b
005Eh	CCA Complete Interrupt Control Register	BBCCAIC	XXXXX000b
005Fh	BB Timer Compare 0 Interrupt Control Register	BBTIM0IC	XXXXX000b
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah			
006Bh			
006Ch	Address Filter Interrupt Control Register	BBADFIC	XXXXX000b
006Dh	Transmit Overrun Interrupt Control Register	BBTXORIC	XXXXX000b
006Eh	Transmission Complete Interrupt Control Register	BBTXIC	XX00XX00b
006Fh	Receive Overrun 1 Interrupt Control Register	BBRXOR1IC	XXXXX000b

X: Undefined

Notes:

1. The blank areas are reserved and cannot be accessed by users.
2. Selectable by the IICSEL bit in the SSUIICSR register.
3. The LVDAS bit in the OFS register is set to 1.
4. The LVDAS bit in the OFS register is set to 0.
5. Can be selected by the BANK0INTSEL bit in the BBTXRXMODE4 register.

Table 4.3 SFR Information (3) (0070h to 00AFh) (1)

Address	Register	Symbol	After Reset
0070h	PLL Lock Detection Interrupt Control Register	BBPLLIC	XXXXX000b
0071h	Receive Overrun 0/Calibration Complete Interrupt Control Register (3)	BBRXOR0IC/BBCALIC	XXXXX000b
0072h	Voltage Monitor 1 Interrupt Control Register	VCMP1IC	XXXXX000b
0073h	Bank 1 Reception Complete/Clock Regulator Interrupt Control Register (2)	BBRX1IC/BBCREGIC	XXXXX000b
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			
0080h	DTC Activation Control Register	DTCTL	00h
0081h			
0082h			
0083h			
0084h			
0085h			
0086h			
0087h			
0088h	DTC Activation Enable Register 0	DTCEN0	00h
0089h	DTC Activation Enable Register 1	DTCEN1	00h
008Ah	DTC Activation Enable Register 2	DTCEN2	00h
008Bh	DTC Activation Enable Register 3	DTCEN3	00h
008Ch			
008Dh	DTC Activation Enable Register 5	DTCEN5	00h
008Eh	DTC Activation Enable Register 6	DTCEN6	00h
008Fh			
0090h			
0091h			
0092h			
0093h			
0094h			
0095h			
0096h			
0097h			
0098h			
0099h			
009Ah			
009Bh			
009Ch			
009Dh			
009Eh			
009Fh			
00A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h			XXh
00A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00A5h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00A6h	UART0 Receive Buffer Register	U0RB	XXh
00A7h			XXh
00A8h			
00A9h			
00AAh			
00ABh			
00ACh			
00ADh			
00AEh			
00AFh			

X: Undefined

Notes:

1. The blank areas are reserved and cannot be accessed by users.
2. Can be selected by the BANK1INTSEL bit in the BBTXRXMODE4 register.
3. Can be selected by the ROR0INTSEL bit in the BBTXRXMODE4 register.

Table 4.6 SFR Information (6) (01A0h to 02FFh) (1)

Address	Register	Symbol	After Reset
01A0h			
:			
01B0h			
01B1h			
01B2h	Flash Memory Status Register	FST	10000X00b
01B3h			
01B4h	Flash Memory Control Register 0	FMR0	00h
01B5h	Flash Memory Control Register 1	FMR1	00h
01B6h	Flash Memory Control Register 2	FMR2	00h
01B7h			
01B8h			
01B9h			
01BAh			
01BBh			
01BCh			
01BDh			
01BEh			
01BFh			
01C0h	Address Match Interrupt Register 0	RMAD0	XXh
01C1h			XXh
01C2h			0000XXXXb
01C3h	Address Match Interrupt Enable Register 0	AIER0	00h
01C4h	Address Match Interrupt Register 1	RMAD1	XXh
01C5h			XXh
01C6h			0000XXXXb
01C7h	Address Match Interrupt Enable Register 1	AIER1	00h
01C8h			
:			
01DFh			
01E0h	Pull-Up Control Register 0	PUR0	00h
01E1h	Pull-Up Control Register 1	PUR1	00h
01E2h			
01E3h			
01E4h			
01E5h			
01E6h			
01E7h			
01E8h			
01E9h			
01EAh			
01EBh			
01ECh			
01EDh			
01EEh			
01EFh			
01F0h	Port P1 Drive Capacity Control Register	P1DRR	00h
01F1h			
01F2h	Drive Capacity Control Register 0	DRR0	00h
01F3h	Drive Capacity Control Register 1	DRR1	00h
01F4h			
01F5h	Input Threshold Control Register 0	VLT0	00h
01F6h	Input Threshold Control Register 1	VLT1	00h
01F7h			
01F8h			
01F9h			
01FAh	External Input Enable Register 0	INTEN	00h
01FBh			
01FCh	INT Input Filter Select Register 0	INTF	00h
01FDh			
01FEh	Key Input Enable Register 0	KIEN	00h
01FFh	Key Input Enable Register 1	KI1EN	00h
0200h			
:			
02FFh			

X: Undefined

Notes:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.7 SFR Information (7) (2C00h to 2C6Fh) (1)

Address	Register	Symbol	After Reset
2C00h	DTC Transfer Vector Area		XXh
2C01h	DTC Transfer Vector Area		XXh
2C02h	DTC Transfer Vector Area		XXh
2C03h	DTC Transfer Vector Area		XXh
2C04h	DTC Transfer Vector Area		XXh
2C05h	DTC Transfer Vector Area		XXh
2C06h	DTC Transfer Vector Area		XXh
2C07h	DTC Transfer Vector Area		XXh
2C08h	DTC Transfer Vector Area		XXh
2C09h	DTC Transfer Vector Area		XXh
2C0Ah	DTC Transfer Vector Area		XXh
:	DTC Transfer Vector Area		XXh
:	DTC Transfer Vector Area		XXh
2C3Ah	DTC Transfer Vector Area		XXh
2C3Bh	DTC Transfer Vector Area		XXh
2C3Ch	DTC Transfer Vector Area		XXh
2C3Dh	DTC Transfer Vector Area		XXh
2C3Eh	DTC Transfer Vector Area		XXh
2C3Fh	DTC Transfer Vector Area		XXh
2C40h	DTC Control Data 0	DTCD0	XXh
2C41h			XXh
2C42h			XXh
2C43h			XXh
2C44h			XXh
2C45h			XXh
2C46h			XXh
2C47h			XXh
2C48h	DTC Control Data 1	DTCD1	XXh
2C49h			XXh
2C4Ah			XXh
2C4Bh			XXh
2C4Ch			XXh
2C4Dh			XXh
2C4Eh			XXh
2C4Fh			XXh
2C50h	DTC Control Data 2	DTCD2	XXh
2C51h			XXh
2C52h			XXh
2C53h			XXh
2C54h			XXh
2C55h			XXh
2C56h			XXh
2C57h			XXh
2C58h	DTC Control Data 3	DTCD3	XXh
2C59h			XXh
2C5Ah			XXh
2C5Bh			XXh
2C5Ch			XXh
2C5Dh			XXh
2C5Eh			XXh
2C5Fh			XXh
2C60h	DTC Control Data 4	DTCD4	XXh
2C61h			XXh
2C62h			XXh
2C63h			XXh
2C64h			XXh
2C65h			XXh
2C66h			XXh
2C67h			XXh
2C68h	DTC Control Data 5	DTCD5	XXh
2C69h			XXh
2C6Ah			XXh
2C6Bh			XXh
2C6Ch			XXh
2C6Dh			XXh
2C6Eh			XXh
2C6Fh			XXh

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.9 SFR Information (9) (2CB0h to 2CEFh) (1)

Address	Register	Symbol	After Reset
2CB0h	DTC Control Data 14	DTCD14	XXh
2CB1h			XXh
2CB2h			XXh
2CB3h			XXh
2CB4h			XXh
2CB5h			XXh
2CB6h			XXh
2CB7h			XXh
2CB8h	DTC Control Data 15	DTCD15	XXh
2CB9h			XXh
2CBAh			XXh
2CBBh			XXh
2CBCh			XXh
2CBDh			XXh
2CBEh			XXh
2CBFh			XXh
2CC0h	DTC Control Data 16	DTCD16	XXh
2CC1h			XXh
2CC2h			XXh
2CC3h			XXh
2CC4h			XXh
2CC5h			XXh
2CC6h			XXh
2CC7h			XXh
2CC8h	DTC Control Data 17	DTCD17	XXh
2CC9h			XXh
2CCAh			XXh
2CCBh			XXh
2CCCh			XXh
2CCDh			XXh
2CCEh			XXh
2CCFh			XXh
2CD0h	DTC Control Data 18	DTCD18	XXh
2CD1h			XXh
2CD2h			XXh
2CD3h			XXh
2CD4h			XXh
2CD5h			XXh
2CD6h			XXh
2CD7h			XXh
2CD8h	DTC Control Data 19	DTCD19	XXh
2CD9h			XXh
2CDAh			XXh
2CDBh			XXh
2CDCh			XXh
2CDDh			XXh
2CDEh			XXh
2CDFh			XXh
2CE0h	DTC Control Data 20	DTCD20	XXh
2CE1h			XXh
2CE2h			XXh
2CE3h			XXh
2CE4h			XXh
2CE5h			XXh
2CE6h			XXh
2CE7h			XXh
2CE8h	DTC Control Data 21	DTCD21	XXh
2CE9h			XXh
2CEAh			XXh
2CEBh			XXh
2CECh			XXh
2CEDh			XXh
2CEEh			XXh
2CEFh			XXh

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.12 ID Code Areas and Option Function Select Area

Address	Area Name	Symbol	After Reset
:			
FFDBh	Option Function Select Register 2	OFS2	(Note 1)
:			
FFDFh	ID1		(Note 2)
:			
FFE3h	ID2		(Note 2)
:			
FFEBh	ID3		(Note 2)
:			
FFEFh	ID4		(Note 2)
:			
FFF3h	ID5		(Note 2)
:			
FFF7h	ID6		(Note 2)
:			
FFFBh	ID7		(Note 2)
:			
FFFFh	Option Function Select Register	OFS	(Note 1)

Notes:
1. The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the option function select area. If the block including the option function select area is erased, the option function select area is set to FFh.
   At shipment, the option function select area is set to FFh. It is set to the written value after written by the user.
2. The ID code areas are allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the ID code areas. If the block including the ID code areas is erased, the ID code areas are set to FFh.
   At shipment, the ID code areas are set to FFh. They are set to the written value after written by the user.

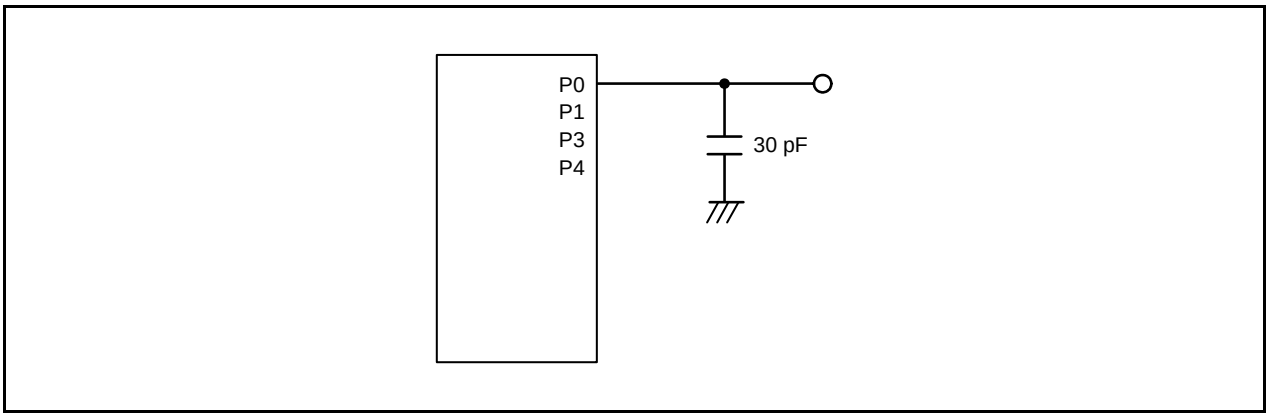


Figure 5.1 Ports P0, P1, P3 and P4 Timing Measurement Circuit

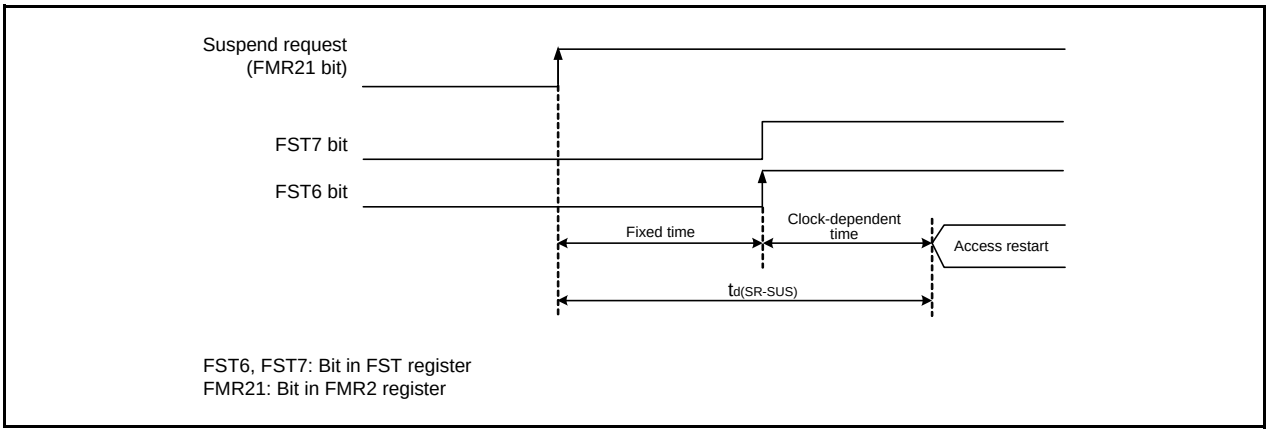


Figure 5.2 Time delay until Suspend

Table 5.5 Voltage Detection 0 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det0}	Voltage detection level Vdet0_0 (4)		1.80	1.90	2.05	V
	Voltage detection level Vdet0_1 (4)		2.15	2.35	2.50	V
	Voltage detection level Vdet0_2 (4)		2.70	2.85	3.05	V
—	Voltage detection 0 circuit response time (3)	At the falling of V_{CC} from 3.6 V to (Vdet0_0 – 0.1) V	—	6	150	µs
—	Voltage detection circuit self power consumption	VCA25 = 1, V_{CC} = 3.0 V	—	1.5	—	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts (2)		—	—	100	µs

Notes:
1. The measurement condition is V_{CC} = 1.8 V to 3.6 V and T_{opr} = –20°C to 85°C.
2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.
3. Time until the voltage monitor 0 reset is generated after the voltage passes V_{det0}.
4. Select the voltage detection level with bits VDSEL0 and VDSEL1 in the OFS register.

Table 5.6 Voltage Detection 1 Circuit Electrical Characteristics

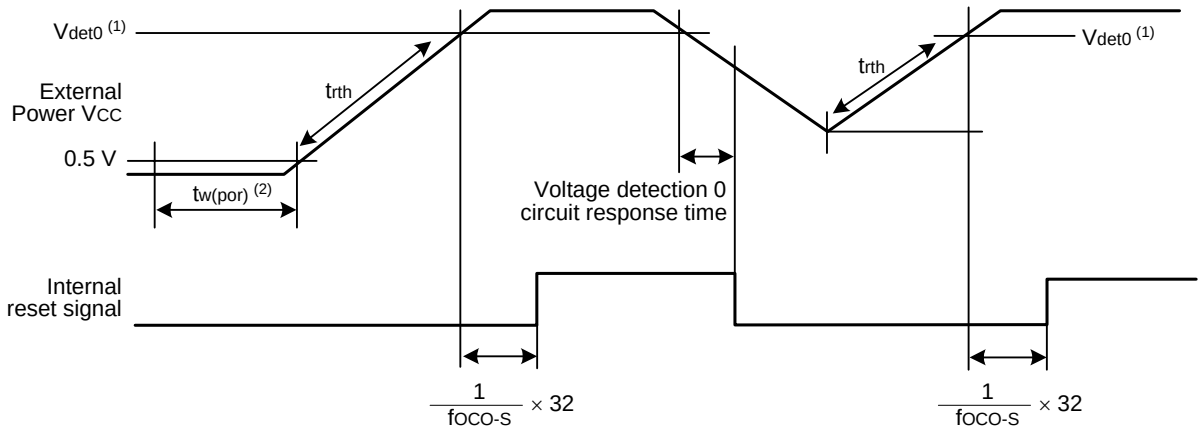
Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det1}	Voltage detection level Vdet1_2 (2)	At the falling of V_{CC}	2.30	2.50	2.70	V
	Voltage detection level Vdet1_5 (2)	At the falling of V_{CC}	2.75	2.95	3.15	V
—	Hysteresis width at the rising of V_{CC} in voltage detection 1 circuit		—	0.07	—	V
—	Voltage detection 1 circuit response time (3)	At the falling of V_{CC} from 3.6 V to (Vdet1_0 – 0.1) V	—	60	150	µs
—	Voltage detection circuit self power consumption	VCA26 = 1, V_{CC} = 3.0 V	—	1.7	—	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts (4)		—	—	100	µs

Notes:
1. The measurement condition is V_{CC} = 1.8 V to 3.6 V and T_{opr} = –20°C to 85°C.
2. Select the voltage detection level with bits VD1S0 to VD1S3 in the VD1LS register.
3. Time until the voltage monitor 1 interrupt request is generated after the voltage passes V_{det1}.
4. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

Table 5.7 Power-on Reset Circuit (2)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t_{rth}	External power V_{CC} rise gradient	(1)	0	—	50,000	mV/msec

Notes:
1. The measurement condition is T_{opr} = –20°C to 85°C, unless otherwise specified.
2. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.



Notes:
1. V_{det0} indicates the voltage detection level of the voltage detection 0 circuit. Refer to **6. Voltage Detection Circuit** of User's Manual: Hardware for details.
2. $t_{w(por)}$ indicates the duration the external power V_{CC} must be held below the valid voltage (0.5 V) to enable a power-on reset. When turning on the power after it falls with voltage monitor 0 reset disabled, maintain $t_{w(por)}$ for 1 ms or more.

Figure 5.3 Power-on Reset Circuit Electrical Characteristics

Table 5.13 Electrical Characteristics (1) [1.8 V ≤ Vcc ≤ 3.6 V]
(Topr = –20°C to 85°C, unless otherwise specified)

Symbol	Parameter	Condition			Standard			Unit
					Min.	Typ.	Max.	
ICC	Power supply current Single-chip mode, output pins are open, other pins are VSS	High-speed clock mode XIN clock oscillator on f(XIN) = 16 MHz XCIN clock oscillator on f(XCIN) = 32 kHz Low-speed on-chip oscillator on fOCO-S = 125 kHz System clock = XIN	CPU clock = Divide-by-4, (f(BCLK) = 4 MHz) 1.8 V ≤ VCC ≤ 3.6 V	RF = off	—	2.5	—	mA
				RF = idle	—	4.0	—	mA
				RF = Tx	—	18	—	mA
				RF = Rx (reception standby)	—	24	—	mA
				RF = Rx (reception in progress)	—	25	—	mA
			CPU clock = Divide-by-2, (f(BCLK) = 8 MHz) 2.15 V ≤ VCC ≤ 3.6 V	RF = off	—	3.5	—	mA
				RF = idle	—	5.0	—	mA
				RF = Tx	—	19	—	mA
				RF = Rx (reception standby)	—	25	—	mA
				RF = Rx (reception in progress)	—	26	—	mA
			CPU clock = No division (f(BCLK) = 16 MHz) 2.7 V ≤ VCC ≤ 3.6 V	RF = off	—	6.0	—	mA
				RF = idle	—	7.5	—	mA
				RF = Tx	—	21.5	—	mA
				RF = Rx (reception standby)	—	27.5	—	mA
				RF = Rx (reception in progress)	—	28.5	—	mA
		Low-speed on-chip oscillator mode XIN clock off, XCIN clock off, Low-speed on-chip oscillator on: fOCO-S = 125 kHz System clock = fOCO-S, CPU clock = Divide-by-8 FMR27 = 1, VCA20 = 0 (flash memory low-current-consumption read mode)		RF = off	—	80	—	µA
		Low-speed clock mode XIN clock off XCIN clock oscillator on f(XCIN) = 32 kHz Low-speed on-chip oscillator off System clock = XCIN CPU clock = No division	FMR27 = 1 VCA20 = 0 (flash memory low-current-consumption read mode)	RF = off	—	95	—	µA
			FMSTP = 1 VCA20 = 0 (Flash memory off, program operation on RAM)	RF = off	—	45	—	µA
		Wait mode XIN clock oscillator on: f(XIN) = 16 MHz XCIN clock oscillator on: f(XCIN) = 32 kHz Low-speed on-chip oscillator on: fOCO-S = 125 kHz System clock = XIN While a WAIT instruction is executed		RF = Rx (reception standby)	—	23	—	mA
		Wait mode XIN clock off XCIN clock oscillator on f(XCIN) = 32 kHz Low-speed on-chip oscillator off System clock = XCIN While a WAIT instruction is executed	Peripheral function clock on VCA26 = VCA25 = 0 VCA20 = 1 (voltage detection circuit stopped, internal power consumption enabled)	RF = off	—	6.0	—	µA
			Peripheral function clock off VCA26 = VCA25 = 0 VCA20 = 1 (voltage detection circuit stopped, internal power consumption enabled)	RF = off	—	4.5	—	µA
		Wait mode XIN clock off XCIN clock oscillator on Low-speed on-chip oscillator on fOCO-S = 125 kHz System clock = fOCO-S While a WAIT instruction is executed	Peripheral function clock on VCA26 = VCA25 = 0 VCA20 = 1 (voltage detection circuit stopped, internal low power consumption enabled)	RF = off	—	13.0	—	µA
			Peripheral function clock off VCA26 = VCA25 = 0 VCA20 = 1 (voltage detection circuit stopped, internal low power consumption enabled)	RF = off	—	7.5	—	µA
		Stop mode (Topr = 25°C) XIN clock off, XCIN clock off, Low-speed on-chip oscillator off, VCA26 = VCA25 = 0 (voltage detection circuit stopped)		RF = off	—	2.0	—	µA

Timing requirements (VCC = 2.15 V, Topr = –20°C to 85°C, unless otherwise specified)

Table 5.19 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	500	—	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	200	—	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	200	—	ns

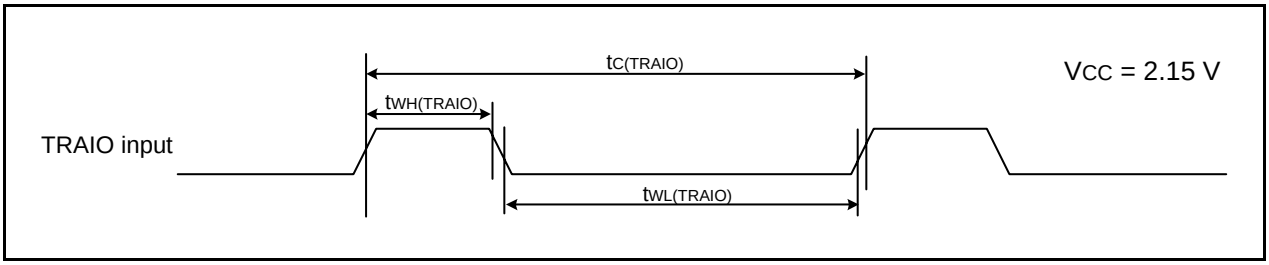


Figure 5.11 TRAIO Input Timing Diagram when VCC = 2.15 V

Table 5.20 Serial Interface

Symbol	Parameter		Standard		Unit
			Min.	Max.	
$t_{c(CK)}$	CLK0 input cycle time	When an external clock is selected	800	—	ns
$t_{W(CKH)}$	CLK0 input “H” width		400	—	ns
$t_{W(CKL)}$	CLK0 input “L” width		400	—	ns
$t_{d(C-Q)}$	TXD0 output delay time		—	200	ns
$t_{h(C-Q)}$	TXD0 hold time		0	—	ns
$t_{su(D-C)}$	RXD0 input setup time		150	—	ns
$t_{h(C-D)}$	RXD0 input hold time		90	—	ns
$t_{h(C-Q)}$	TXD0 output delay time	When an internal clock is selected	—	200	ns
$t_{su(D-C)}$	RXD0 input setup time		150	—	ns
$t_{h(C-D)}$	RXD0 input hold time		90	—	ns

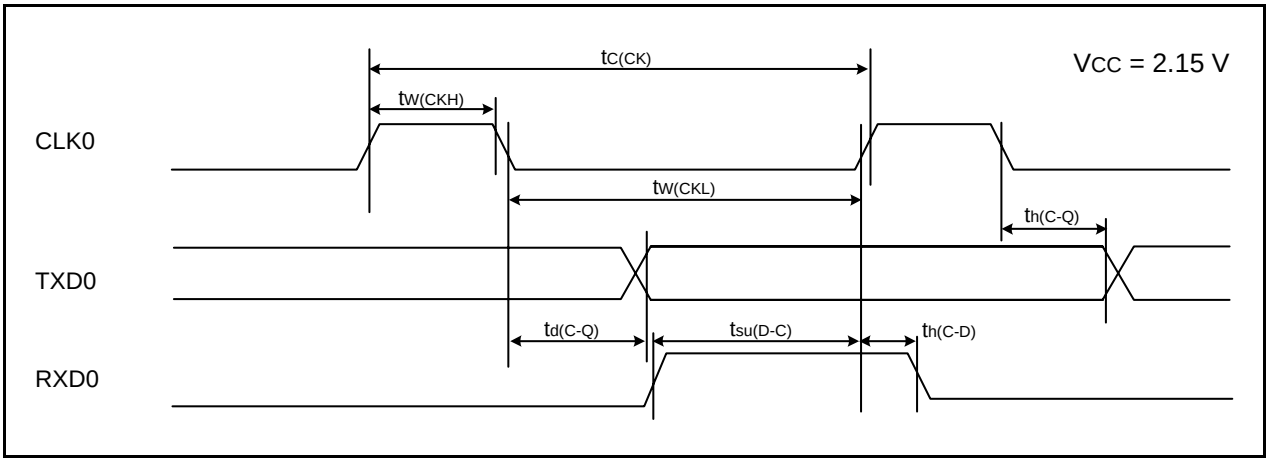


Figure 5.12 Serial Interface Timing Diagram when VCC = 2.15 V

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