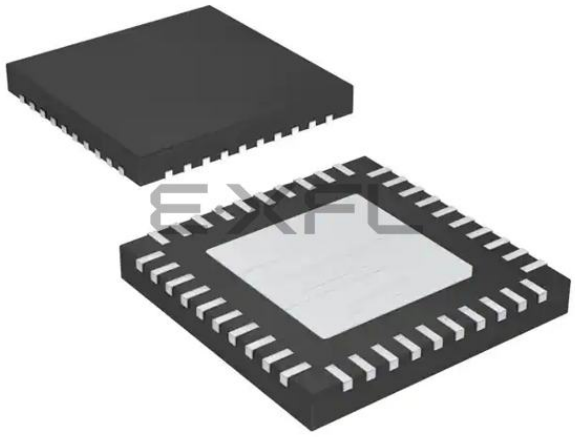
Renesas Electronics America Inc - R5F213MCQNNP#U0 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	R8C
Core Size	16-Bit
Speed	16MHz
Connectivity	I²C, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	18
Program Memory Size	112KB (112K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	7.5K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-WFQFN Exposed Pad
Supplier Device Package	40-HWQFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f213mcqnnp-u0

1.1.2 Specifications

Tables 1.1 and 1.2 outline the Specifications for R8C/3MQ Group.

Table 1.1 Specifications for R8C/3MQ Group (1)

Item	Function	Specification
CPU	Central processing unit	R8C CPU core • Number of fundamental instructions: 89 • Minimum instruction execution time: 62.5 ns (f(BCLK) = 16 MHz, VCC = 2.7 to 3.6 V) 125 ns (f(BCLK) = 8 MHz, VCC = 2.15 to 3.6 V) 250 ns (f(BCLK) = 4 MHz, VCC = 1.8 to 3.6 V) • Multiplier: 16 bits × 16 bits → 32 bits • Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits • Operation mode: Single-chip mode (address space: 1 Mbyte)
Memory	ROM, RAM, Data flash	Refer to **Table 1.4 Product List for R8C/3MQ Group**.
Power Supply Voltage Detection	Voltage detection circuit	• Power-on reset • Voltage detection 2 (detection level selectable)
I/O Ports	Programmable I/O ports	CMOS I/O ports: 18 (including XCIN and XCOUT), selectable pull-up resistor (for some ports)
Clock	Clock generation circuits	• 3 circuits: XIN clock oscillation circuit, XCIN clock oscillation circuit (32 kHz), Low-speed on-chip oscillator • Oscillation stop detection: XIN clock oscillation stop detection function • Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16 • Low power consumption modes: Standard operating mode (high-speed clock, low-speed clock, low-speed on-chip oscillator), wait mode, stop mode
		Real-time clock (timer RE)
Interrupts		• Interrupt Vectors: 69 • External: 11 sources ($\overline{\text{INT}}$ × 3, key input × 8) • Priority levels: 7 levels
Watchdog Timer		• 14 bits × 1 (with prescaler) • Reset start selectable • Low-speed on-chip oscillator for watchdog timer selectable
DTC (Data Transfer Controller)		• 1 channel • Activation sources: 17 • Transfer modes: 2 (normal mode, repeat mode)
Timer	Timer RA	8 bits × 1 (with 8-bit prescaler) Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
	Timer RB	8 bits × 1 (with 8-bit prescaler) Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode
	Timer RC	16 bits × 1 (with 4 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output 3 pins), PWM2 mode (PWM output pin)
	Timer RE	8 bits × 1 Real-time clock mode (count seconds, minutes, hours, days of week), output compare mode

Table 1.5 Pin Name Information by Pin Number

Pin Number	Control Pin	Port	I/O Pin Functions for Peripheral Modules					
			Interrupt	Timer	Serial Interface	SSU	I^2C bus	RF Pin Other
1	VREGOUT3							
2	VSS2							
3	XIN							
4	XOUT							
5	$\overline{\text{RESET}}$							
6	VSS1							
7	MODE							
8	VCC							
9	(XCIN)	P4_3						
10	(XCOUT)	P4_4						
11		P1_7	$\overline{\text{KI7}}$/$\overline{\text{INT1}}$	(TRAIO)				
12		P1_6	$\overline{\text{KI6}}$		(CLK0)			
13		P1_5	$\overline{\text{KI5}}$(/$\overline{\text{INT1}}$)	(TRAIO)	(RXD0)			
14		P1_4	$\overline{\text{KI4}}$	(TRCCLK)	(TXD0)			
15		P1_3	$\overline{\text{KI3}}$	TRBO(/TRCIOC)				
16		P1_2	$\overline{\text{KI2}}$	(TRCIOB)				
17		P1_1	$\overline{\text{KI1}}$	(TRCIOA/TRCTRG)				
18		P1_0	$\overline{\text{KI0}}$	(TRCIOD)				
19								IFRXTP
20								IFRXTN
21	VCCRF							
22	VREGOUT1							
23	VREG1							
24	VREG2							
25	VSSRF							
26								RFIOP
27								RFION
28	VSSRF1							
29	VSSRF2							
30	VREG3							
31	VREGOUT2							
32	VREG4							
33		P0_4		TREO(/TRCIOB)				ASW
34		P3_7		TRAO		SSO	SDA	
35		P3_5		(TRCIOD)		SSCK	SCL	
36		P3_4		(TRCIOC)		SSI		
37		P3_3	$\overline{\text{INT3}}$	(TRCCLK)		$\overline{\text{SCS}}$		
38		P3_1		(TRBO)				
39		P3_0		(TRAO)				
40		P4_5	$\overline{\text{INT0}}$					
Bottom side	DIEGND							

Note:
1. The function in parentheses can be assigned to the pin by a program.

1.5 Pin Functions

Tables 1.6 and 1.7 list Pin Functions.

Table 1.6 Pin Functions (1)

Item	Pin Name	I/O Type	Description
Power supply input	VCC, VSS1	—	Apply 1.8 to 3.6 V to the VCC pin. Apply 0 V to the VSS1 pin.
Reset input	$\overline{\text{RESET}}$	I	Input “L” on this pin resets the MCU.
MODE	MODE	I	Connect this pin to VCC via a resistor.
XIN clock input	XIN	I	These pins are provided for XIN clock oscillation circuit I/O. Connect a crystal oscillator between the XIN and XOUT pins.
XIN clock output	XOUT	I/O	
XCIN clock input	XCIN	I	These pins are provided for XCIN clock oscillation circuit I/O. Connect a crystal oscillator between the XCIN and XCOUT pins.
XCIN clock output	XCOUT	O	
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$, $\overline{\text{INT1}}$, $\overline{\text{INT3}}$	I	$\overline{\text{INT}}$ interrupt input pins. $\overline{\text{INT0}}$ is used as an input pin for timer RB and timer RC.
Key input interrupt input	$\overline{\text{KI0}}$ to $\overline{\text{KI7}}$	I	Key input interrupt input pins.
Timer RA	TRAIO	I/O	Timer RA I/O pin.
	TRAO	O	Timer RA output pin.
Timer RB	TRBO	O	Timer RB output pin.
Timer RC	TRCCLK	I	External clock input pin.
	TRCTRG	I	External trigger input pin.
	TRCIOA, TRCIOB, TRCIOC, TRCIOD	I/O	Timer RC I/O pins.
Timer RE	TREO	O	Divided clock output pin.
Serial interface	CLK0	I/O	Transfer clock I/O pin.
	RXD0	I	Serial data input pin.
	TXD0	O	Serial data output pin.
SSU	SSI	I/O	Data I/O pin.
	$\overline{\text{SCS}}$	I/O	Chip-select signal I/O pin.
	SSCK	I/O	Clock I/O pin.
	SSO	I/O	Data I/O pin.
I^2C bus	SCL	I/O	Clock I/O pin
	SDA	I/O	Data I/O pin
I/O ports	P0_4, P1_0 to P1_7, P3_0, P3_1, P3_3 to P3_5, P3_7, P4_3 to P4_5	I/O	CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program.

I: Input O: Output I/O: Input and output

Table 4.6 SFR Information (6) (01A0h to 02FFh) (1)

Address	Register	Symbol	After Reset
01A0h			
:			
01B0h			
01B1h			
01B2h	Flash Memory Status Register	FST	10000X00b
01B3h			
01B4h	Flash Memory Control Register 0	FMR0	00h
01B5h	Flash Memory Control Register 1	FMR1	00h
01B6h	Flash Memory Control Register 2	FMR2	00h
01B7h			
01B8h			
01B9h			
01BAh			
01BBh			
01BCh			
01BDh			
01BEh			
01BFh			
01C0h	Address Match Interrupt Register 0	RMAD0	XXh
01C1h			XXh
01C2h			0000XXXXb
01C3h	Address Match Interrupt Enable Register 0	AIER0	00h
01C4h	Address Match Interrupt Register 1	RMAD1	XXh
01C5h			XXh
01C6h			0000XXXXb
01C7h	Address Match Interrupt Enable Register 1	AIER1	00h
01C8h			
:			
01DFh			
01E0h	Pull-Up Control Register 0	PUR0	00h
01E1h	Pull-Up Control Register 1	PUR1	00h
01E2h			
01E3h			
01E4h			
01E5h			
01E6h			
01E7h			
01E8h			
01E9h			
01EAh			
01EBh			
01ECh			
01EDh			
01EEh			
01EFh			
01F0h	Port P1 Drive Capacity Control Register	P1DRR	00h
01F1h			
01F2h	Drive Capacity Control Register 0	DRR0	00h
01F3h	Drive Capacity Control Register 1	DRR1	00h
01F4h			
01F5h	Input Threshold Control Register 0	VLT0	00h
01F6h	Input Threshold Control Register 1	VLT1	00h
01F7h			
01F8h			
01F9h			
01FAh	External Input Enable Register 0	INTEN	00h
01FBh			
01FCh	INT Input Filter Select Register 0	INTF	00h
01FDh			
01FEh	Key Input Enable Register 0	KIEN	00h
01FFh	Key Input Enable Register 1	KI1EN	00h
0200h			
:			
02FFh			

X: Undefined

Notes:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.7 SFR Information (7) (2C00h to 2C6Fh) (1)

Address	Register	Symbol	After Reset
2C00h	DTC Transfer Vector Area		XXh
2C01h	DTC Transfer Vector Area		XXh
2C02h	DTC Transfer Vector Area		XXh
2C03h	DTC Transfer Vector Area		XXh
2C04h	DTC Transfer Vector Area		XXh
2C05h	DTC Transfer Vector Area		XXh
2C06h	DTC Transfer Vector Area		XXh
2C07h	DTC Transfer Vector Area		XXh
2C08h	DTC Transfer Vector Area		XXh
2C09h	DTC Transfer Vector Area		XXh
2C0Ah	DTC Transfer Vector Area		XXh
:	DTC Transfer Vector Area		XXh
:	DTC Transfer Vector Area		XXh
2C3Ah	DTC Transfer Vector Area		XXh
2C3Bh	DTC Transfer Vector Area		XXh
2C3Ch	DTC Transfer Vector Area		XXh
2C3Dh	DTC Transfer Vector Area		XXh
2C3Eh	DTC Transfer Vector Area		XXh
2C3Fh	DTC Transfer Vector Area		XXh
2C40h	DTC Control Data 0	DTCD0	XXh
2C41h			XXh
2C42h			XXh
2C43h			XXh
2C44h			XXh
2C45h			XXh
2C46h			XXh
2C47h			XXh
2C48h	DTC Control Data 1	DTCD1	XXh
2C49h			XXh
2C4Ah			XXh
2C4Bh			XXh
2C4Ch			XXh
2C4Dh			XXh
2C4Eh			XXh
2C4Fh			XXh
2C50h	DTC Control Data 2	DTCD2	XXh
2C51h			XXh
2C52h			XXh
2C53h			XXh
2C54h			XXh
2C55h			XXh
2C56h			XXh
2C57h			XXh
2C58h	DTC Control Data 3	DTCD3	XXh
2C59h			XXh
2C5Ah			XXh
2C5Bh			XXh
2C5Ch			XXh
2C5Dh			XXh
2C5Eh			XXh
2C5Fh			XXh
2C60h	DTC Control Data 4	DTCD4	XXh
2C61h			XXh
2C62h			XXh
2C63h			XXh
2C64h			XXh
2C65h			XXh
2C66h			XXh
2C67h			XXh
2C68h	DTC Control Data 5	DTCD5	XXh
2C69h			XXh
2C6Ah			XXh
2C6Bh			XXh
2C6Ch			XXh
2C6Dh			XXh
2C6Eh			XXh
2C6Fh			XXh

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.10 SFR Information (10) (2CF0h to 2D2Fh) (1)

Address	Register	Symbol	After Reset
2CF0h	DTC Control Data 22	DTCD22	XXh
2CF1h			XXh
2CF2h			XXh
2CF3h			XXh
2CF4h			XXh
2CF5h			XXh
2CF6h			XXh
2CF7h			XXh
2CF8h	DTC Control Data 23	DTCD23	XXh
2CF9h			XXh
2CFAh			XXh
2CFBh			XXh
2CFCh			XXh
2CFDh			XXh
2CFEh			XXh
2CFFh			XXh
2D00h	Baseband Control Register	BBCON	00h
2D01h	Transmit/Receive Reset Register	BBTXRXRST	00h
2D02h	Transmit/Receive Mode Register 0	BBTXRXMODE0	00h
2D03h	Transmit/Receive Mode Register 1	BBTXRXMODE1	00h
2D04h	Receive Frame Length Register	BBRXFLEN	00h
2D05h	Receive Data Counter Register	BBRXCOUNT	00h
2D06h	RSSI/CCA Result Register	BBRSSICCARSLT	00h
2D07h	Transmit/Receive Status Register 0	BBTXRXST0	80h
2D08h	Transmit Frame Length Register	BBTXFLEN	00h
2D09h	Transmit/Receive Mode Register 2	BBTXRXMODE2	30h
2D0Ah	Transmit/Receive Mode Register 3	BBTXRXMODE3	00h
2D0Bh	Receive Level Threshold Set Register	BBLVLVTH	80h
2D0Ch	Transmit/Receive Control Register	BBTXRXCON	00h
2D0Dh	CSMA Control Register 0	BBCSMACON0	00h
2D0Eh	CCA Level Threshold Set Register	BBCCAVTH	80h
2D0Fh	Transmit/Receive Status Register 1	BBTXRXST1	00h
2D10h	RF Control Register	BBRFCON	00h
2D11h	Transmit/Receive Mode Register 4	BBTXRXMODE4	00h
2D12h	CSMA Control Register 1	BBCSMACON1	9Ch
2D13h	CSMA Control Register 2	BBCSMACON2	05h
2D14h	PAN Identifier Register	BBPANID	00h
2D15h			00h
2D16h	Short Address Register	BBSHORTAD	00h
2D17h			00h
2D18h	Extended Address Register	BBEXTENDAD0	00h
2D19h			00h
2D1Ah		BBEXTENDAD1	00h
2D1Bh			00h
2D1Ch		BBEXTENDAD2	00h
2D1Dh			00h
2D1Eh		BBEXTENDAD3	00h
2D1Fh			00h
2D20h	Timer Read-Out Register 0	BBTIMEREAD0	00h
2D21h			00h
2D22h	Timer Read-Out Register 1	BBTIMEREAD1	00h
2D23h			00h
2D24h	Timer Compare 0 Register 0	BBCOMP0REG0	00h
2D25h			00h
2D26h	Timer Compare 0 Register 1	BBCOMP0REG1	00h
2D27h			00h
2D28h	Timer Compare 1 Register 0	BBCOMP1REG0	00h
2D29h			00h
2D2Ah	Timer Compare 1 Register 1	BBCOMP1REG1	00h
2D2Bh			00h
2D2Ch	Timer Compare 2 Register 0	BBCOMP2REG0	00h
2D2Dh			00h
2D2Eh	Timer Compare 2 Register 1	BBCOMP2REG1	00h
2D2Fh			00h

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.11 SFR Information (11) (2D30h to 2FFFh) (1)

Address	Register	Symbol	After Reset
2D30h	Time Stamp Register 0	BBTSTAMP0	00h
2D31h			00h
2D32h	Time Stamp Register 1	BBTSTAMP1	00h
2D33h			00h
2D34h	Timer Control Register	BBTIMECON	00h
2D35h	Backoff Period Register	BBBOFFPROD	00h
2D36h			
2D37h			
2D38h			
2D39h			
2D3Ah	PLL Division Register 0	BBPLLDIVL	65h
2D3Bh	PLL Division Register 1	BBPLLDIVH	09h
2D3Ch	Transmit Output Power Register	BBTXOUTPWR	00h
2D3Dh	RSSI Offset Register	BBRSSIOFS	F6h
2D3Eh			
2D3Fh			
2D40h			
:			
2D45h			
2D46h	Automatic ACK Response Timing Adjustment Register	BBACKRTNTIMG	22h
2D47h			
:			
2D63h			
2D64h			
2D65h			
2D66h			
2D67h			
2D68h	Verification Mode Set Register	BBEVAREG	00h
2D69h			
2D6Ah			
2D6Bh			
2D6Ch			
2D6Dh			
2D6Eh			
2D6Fh			
2D70h			
2D71h			
2D72h			
2D73h			
2D74h			
2D75h			
2D76h	IDLE Wait Set Register	BBIDELWAIT	01h
2D77h			
2D78h			
2D79h			
2D7Ah	ANTSW Output Timing Set Register	BBANTSWTIMG	72h
2D7Bh			
2D7Ch	RF Initial Set Register	BBRFINI	XXh
2D7Dh			XXh
2D7Eh			
2D7Fh			
2D80h			
2D81h			
2D82h	ANTSW Control Register	BBANTSWCON	00h
2D83h			
:			
2DFFh			
2E00h	Transmit RAM	TRANSMIT_RAM_START	
:	Transmit RAM		
2E7Eh	Transmit RAM	TRANSMIT_RAM_END	
2E7Fh			
2D80h	Receive RAM	RECIEVE_RAM_START	
:	Receive RAM		
2EFEh	Receive RAM	RECIEVE_RAM_END	
2EFFh			
2F00h			
:			
2FFFh			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 5.2 Recommended Operating Conditions (1)

Symbol	Parameter				Conditions	Standard			Unit
						Min.	Typ.	Max.	
VCC	Digital supply voltage	(1) During MCU operation under the conditions other than (2) and (3) below.				1.8	3.3	3.6	V
		(2) During programming and erasing of the flash memory using a serial programmer or parallel programmer.				2.7	—	3.6	
		(3) During on-chip debugging with the E8a emulator connected				2.7	—	3.6	
VCCRF	Analog supply voltage					1.8	3.3	3.6	V
VSS/ VSS2/ VSSRF/ VSSRF1/ VSSRF2/ DIEGND	Supply voltage	VSS1, VSS2, VSSRF, VSSRF1, VSSRF2, DIEGND				—	0	—	V
V_{IH}	Input “H” voltage	Other than CMOS input				0.8 Vcc	—	Vcc	V
		CMOS input	Input level switching function (I/O port)	Input level selection: 0.35 Vcc	2.7 V ≤ Vcc ≤ 3.6 V	0.55 Vcc	—	Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0.65 Vcc	—	Vcc	V
				Input level selection: 0.5 Vcc	2.7 V ≤ Vcc ≤ 3.6 V	0.7 Vcc	—	Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0.8 Vcc	—	Vcc	V
				Input level selection: 0.7 Vcc	2.7 V ≤ Vcc ≤ 3.6 V	0.85 Vcc	—	Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0.85 Vcc	—	Vcc	V
V_{IL}	Input “L” voltage	Other than CMOS input				0	—	0.2 Vcc	V
		CMOS input	Input level switching function (I/O port)	Input level selection: 0.35 Vcc	2.7 V ≤ Vcc ≤ 3.6 V	0	—	0.2 Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0	—	0.2 Vcc	V
				Input level selection: 0.5 Vcc	2.7 V ≤ Vcc ≤ 3.6 V	0	—	0.3 Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0	—	0.2 Vcc	V
				Input level selection: 0.7 Vcc	2.7 V ≤ Vcc ≤ 3.6 V	0	—	0.45 Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0	—	0.35 Vcc	V
$I_{OH(sum)}$	Peak sum output “H” current	Sum of all pins $I_{OH(peak)}$				—	—	−160	mA
$I_{OH(sum)}$	Average sum output “H” current	Sum of all pins $I_{OH(avg)}$				—	—	−80	mA
$I_{OH(peak)}$	Peak output “H” current	Drive capacity Low				—	—	−10	mA
		Drive capacity High				—	—	−40	mA
$I_{OH(avg)}$	Average output “H” current	Drive capacity Low				—	—	−5	mA
		Drive capacity High				—	—	−20	mA
$I_{OL(sum)}$	Peak sum output “L” current	Sum of all pins $I_{OL(peak)}$				—	—	160	mA
$I_{OL(sum)}$	Average sum output “L” current	Sum of all pins $I_{OL(avg)}$				—	—	80	mA
$I_{OL(peak)}$	Peak output “L” current	Drive capacity Low				—	—	10	mA
		Drive capacity High				—	—	40	mA
$I_{OL(avg)}$	Average output “L” current	Drive capacity Low				—	—	5	mA
		Drive capacity High				—	—	20	mA
$f_{(XIN)}$	XIN clock input oscillation frequency				1.8 V ≤ Vcc ≤ 3.6 V	—	16	—	MHz
$f_{(XCIN)}$	XCIN clock input oscillation frequency				1.8 V ≤ Vcc ≤ 3.6 V	30	32.768	35	kHz
—	System clock frequency	f(XIN)=16 MHz			1.8 V ≤ Vcc ≤ 3.6 V	—	—	16	MHz
$f_{(BCLK)}$	CPU clock frequency	f(XIN)=16 MHz			2.7 V ≤ Vcc ≤ 3.6 V	—	—	16	MHz
					2.15 V ≤ Vcc < 2.7 V	—	—	8	
					1.8 V ≤ Vcc < 2.15 V	—	—	4	

Notes:
1. Vcc = 1.8 to 3.6 V and T_{opr} = −20°C to 85°C, unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.

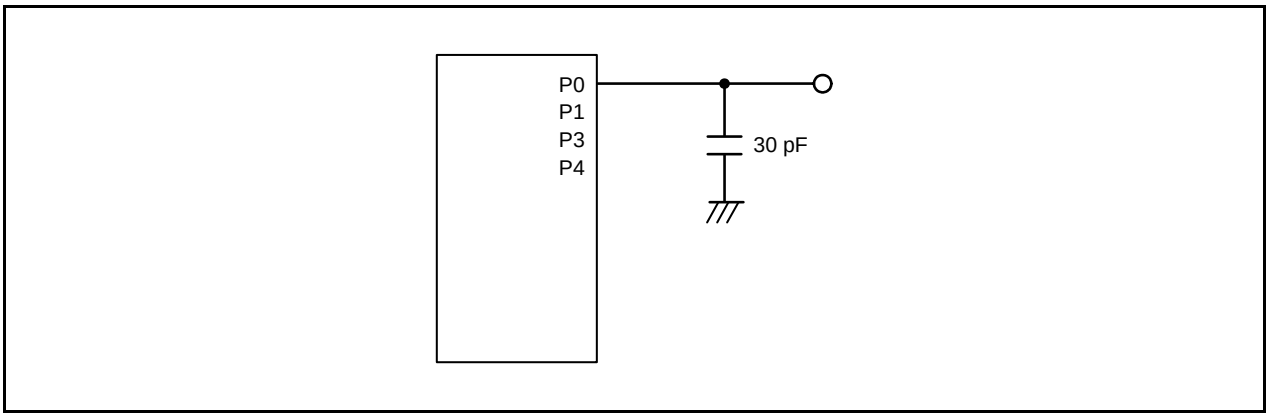


Figure 5.1 Ports P0, P1, P3 and P4 Timing Measurement Circuit

Table 5.4 Flash Memory (Data flash Block A to Block D) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
—	Program/erase endurance (2)		10,000 (3)	—	—	times
—	Byte program time (program/erase endurance ≤ 1,000 times)		—	160	1500	µs
—	Byte program time (program/erase endurance > 1,000 times)		—	300	1500	µs
—	Block erase time (program/erase endurance ≤ 1,000 times)		—	0.2	1	s
—	Block erase time (program/erase endurance > 1,000 times)		—	0.3	1	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		—	—	5 + CPU clock × 3 cycles	ms
—	Interval from erase start/restart until following suspend request		0	—	—	µs
—	Time from suspend until erase restart		—	—	30 + CPU clock × 1 cycle	µs
$t_{d(CMDRST-READY)}$	Time from when command is forcibly stopped until reading is enabled		—	—	30 + CPU clock × 1 cycle	µs
—	Program, erase voltage	CPU rewrite mode	1.8	—	3.6	V
		Standard serial I/O mode	2.7	—	3.6	
		Parallel I/O mode	2.7	—	3.6	
—	Read voltage		1.8	—	3.6	V
—	Program, erase temperature	CPU rewrite mode	−20	—	85	°C
		Standard serial I/O mode	0	—	60	
		Parallel I/O mode	0	—	60	
—	Data hold time (7)	Ambient temperature = 55°C	20	—	—	year

Notes:
1. V_{CC} = 1.8 to 3.6 V and T_{opr} = −20°C to 85°C, unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one. However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed.)
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the erasure endurance between blocks A to D can further reduce the actual erasure endurance. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

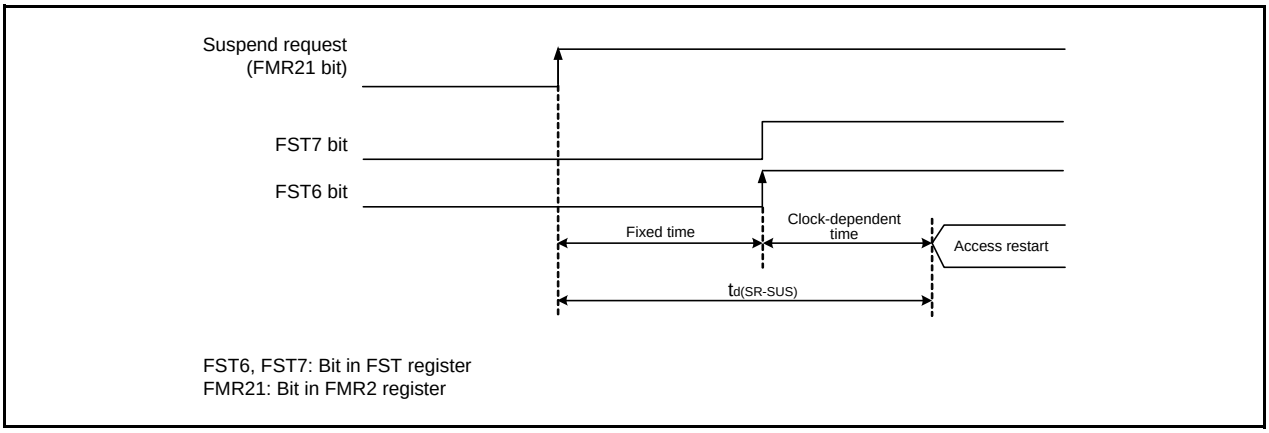


Figure 5.2 Time delay until Suspend

Table 5.5 Voltage Detection 0 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det0}	Voltage detection level Vdet0_0 (4)		1.80	1.90	2.05	V
	Voltage detection level Vdet0_1 (4)		2.15	2.35	2.50	V
	Voltage detection level Vdet0_2 (4)		2.70	2.85	3.05	V
—	Voltage detection 0 circuit response time (3)	At the falling of V_{CC} from 3.6 V to (Vdet0_0 – 0.1) V	—	6	150	µs
—	Voltage detection circuit self power consumption	VCA25 = 1, V_{CC} = 3.0 V	—	1.5	—	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts (2)		—	—	100	µs

Notes:
1. The measurement condition is V_{CC} = 1.8 V to 3.6 V and T_{opr} = –20°C to 85°C.
2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.
3. Time until the voltage monitor 0 reset is generated after the voltage passes V_{det0}.
4. Select the voltage detection level with bits VDSEL0 and VDSEL1 in the OFS register.

Table 5.6 Voltage Detection 1 Circuit Electrical Characteristics

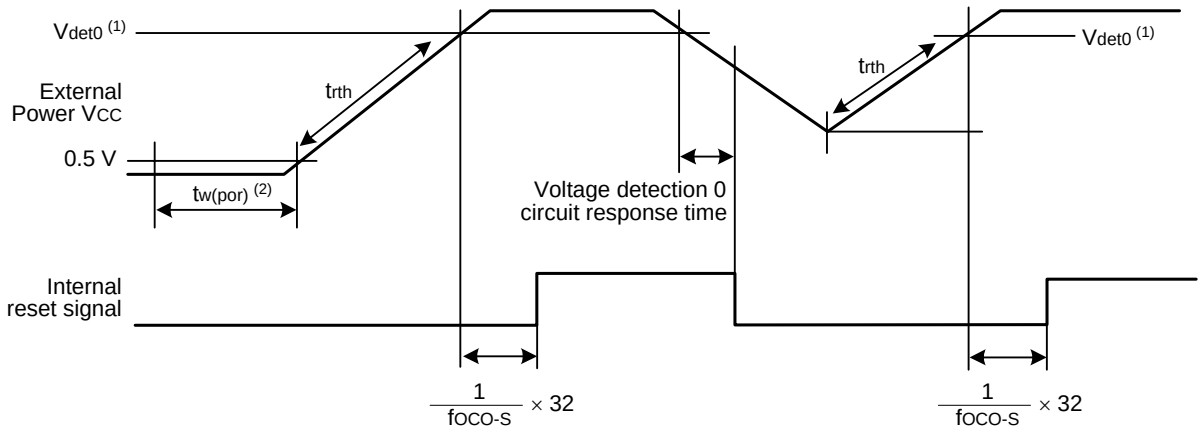
Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det1}	Voltage detection level Vdet1_2 (2)	At the falling of V_{CC}	2.30	2.50	2.70	V
	Voltage detection level Vdet1_5 (2)	At the falling of V_{CC}	2.75	2.95	3.15	V
—	Hysteresis width at the rising of V_{CC} in voltage detection 1 circuit		—	0.07	—	V
—	Voltage detection 1 circuit response time (3)	At the falling of V_{CC} from 3.6 V to (Vdet1_0 – 0.1) V	—	60	150	µs
—	Voltage detection circuit self power consumption	VCA26 = 1, V_{CC} = 3.0 V	—	1.7	—	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts (4)		—	—	100	µs

Notes:
1. The measurement condition is V_{CC} = 1.8 V to 3.6 V and T_{opr} = –20°C to 85°C.
2. Select the voltage detection level with bits VD1S0 to VD1S3 in the VD1LS register.
3. Time until the voltage monitor 1 interrupt request is generated after the voltage passes V_{det1}.
4. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

Table 5.7 Power-on Reset Circuit (2)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t_{rth}	External power V_{CC} rise gradient	(1)	0	—	50,000	mV/msec

Notes:
1. The measurement condition is T_{opr} = –20°C to 85°C, unless otherwise specified.
2. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.



Notes:
1. V_{det0} indicates the voltage detection level of the voltage detection 0 circuit. Refer to **6. Voltage Detection Circuit** of User's Manual: Hardware for details.
2. $t_{w(por)}$ indicates the duration the external power V_{CC} must be held below the valid voltage (0.5 V) to enable a power-on reset. When turning on the power after it falls with voltage monitor 0 reset disabled, maintain $t_{w(por)}$ for 1 ms or more.

Figure 5.3 Power-on Reset Circuit Electrical Characteristics

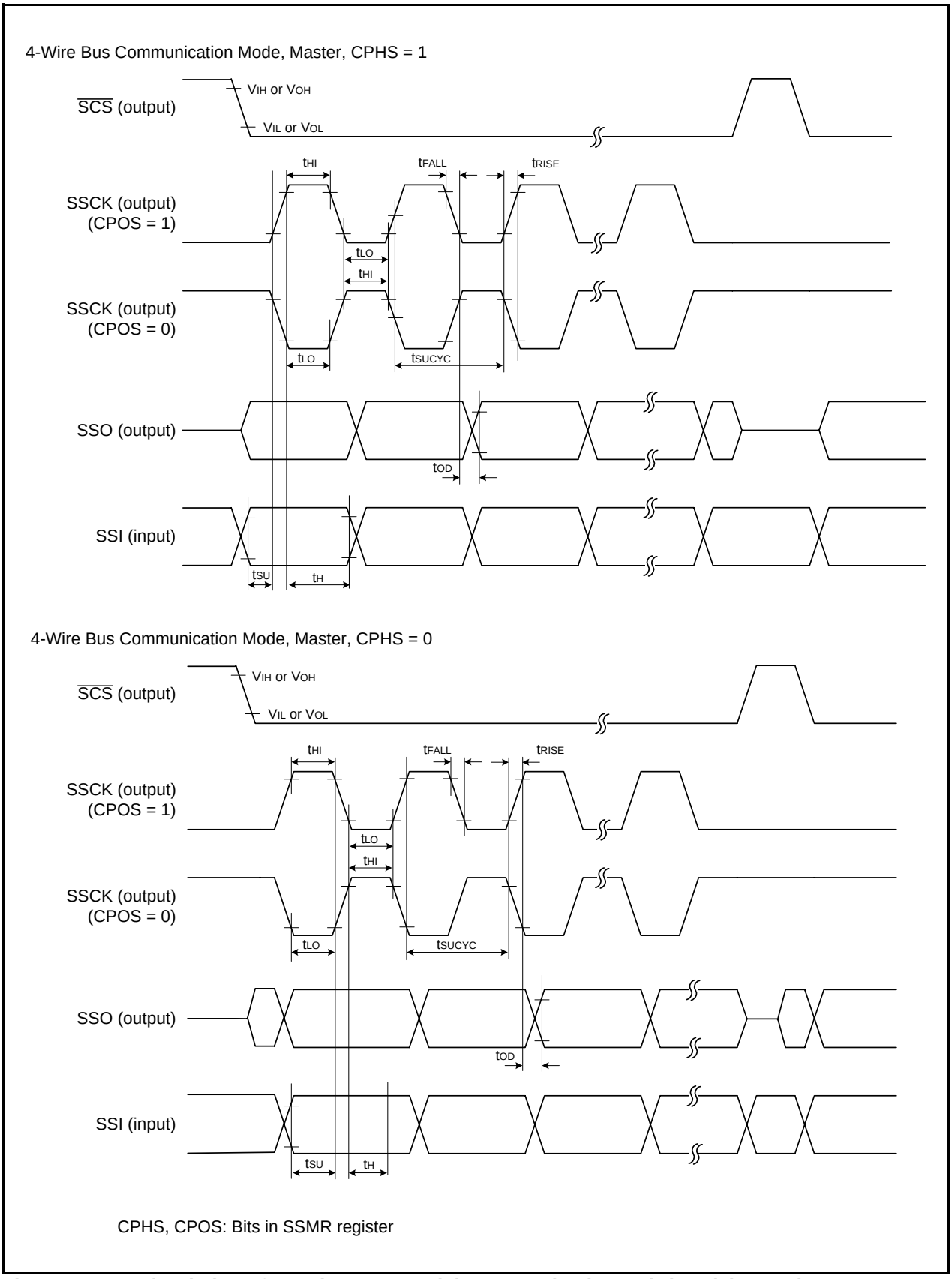


Figure 5.4 I/O Timing of Synchronous Serial Communication Unit (SSU) (Master)

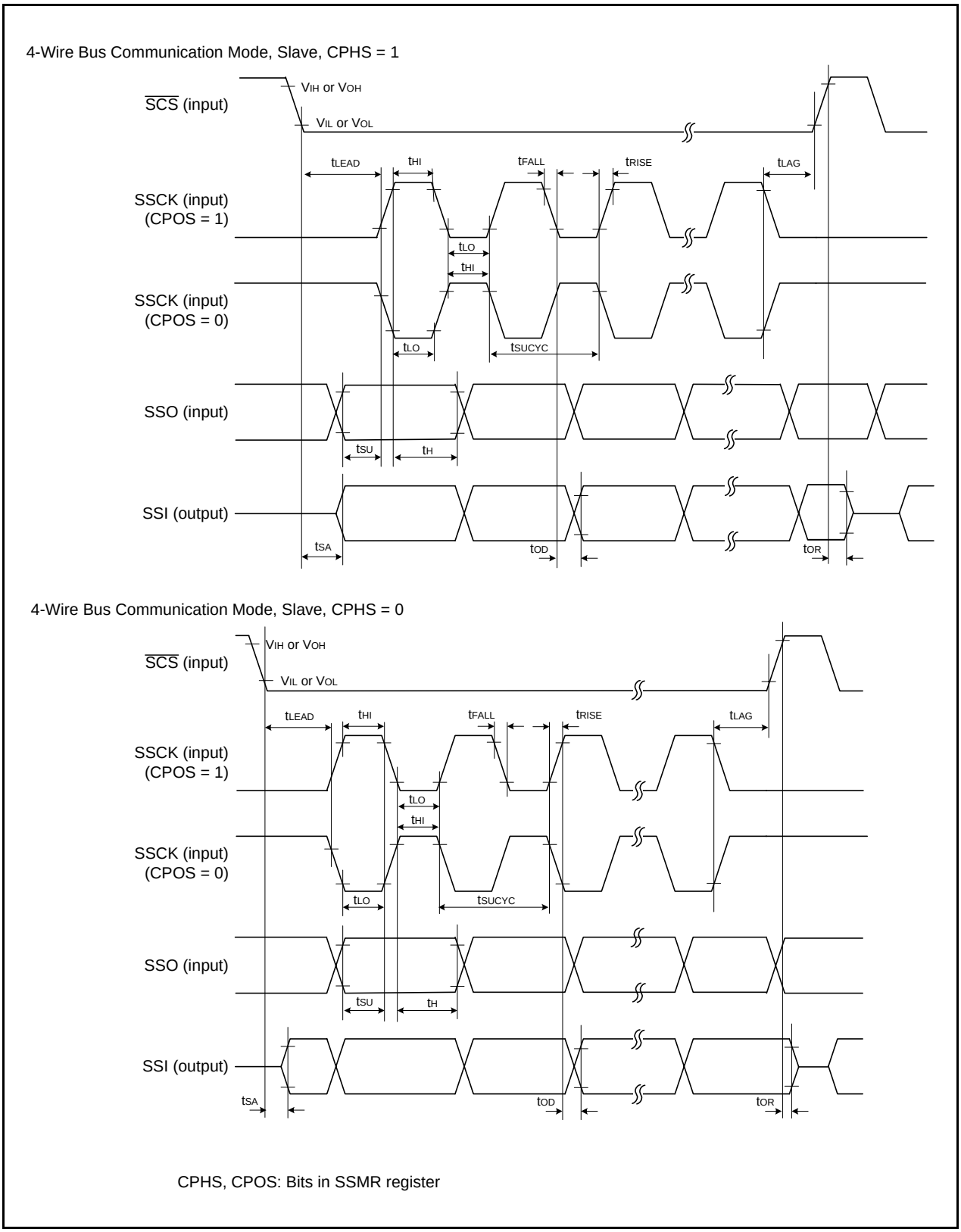


Figure 5.5 I/O Timing of Synchronous Serial Communication Unit (SSU) (Slave)

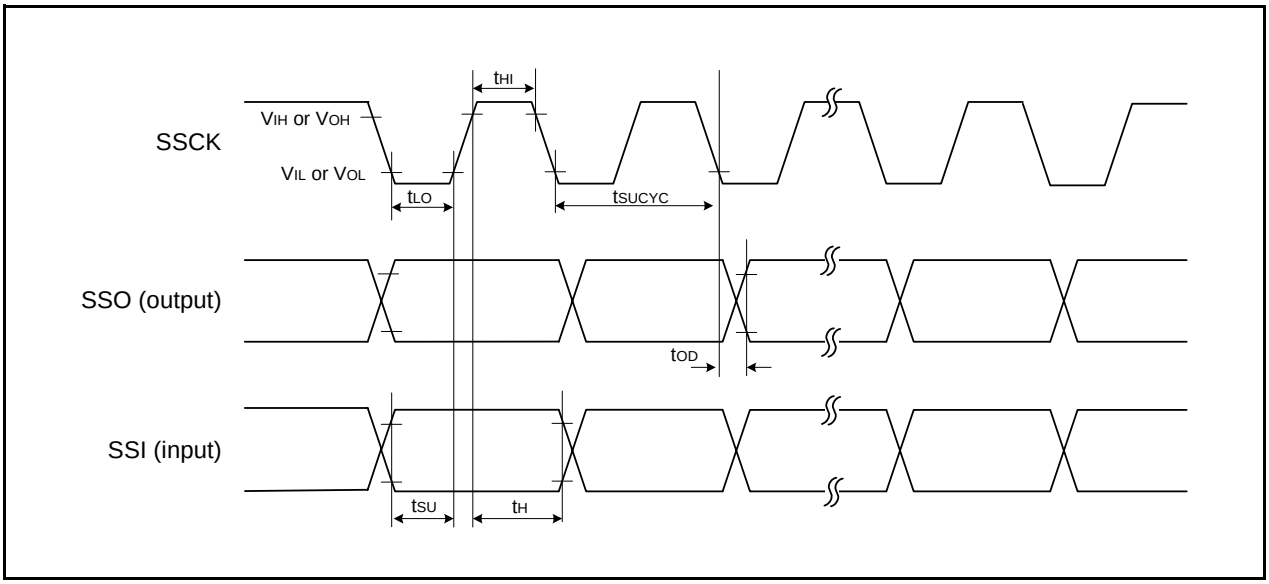


Figure 5.6 I/O Timing of Synchronous Serial Communication Unit (SSU) (Clock Synchronous Communication Mode)

Table 5.13 Electrical Characteristics (1) [1.8 V ≤ Vcc ≤ 3.6 V]
(Topr = –20°C to 85°C, unless otherwise specified)

Symbol	Parameter	Condition			Standard			Unit
					Min.	Typ.	Max.	
ICC	Power supply current Single-chip mode, output pins are open, other pins are VSS	High-speed clock mode XIN clock oscillator on f(XIN) = 16 MHz XCIN clock oscillator on f(XCIN) = 32 kHz Low-speed on-chip oscillator on fOCO-S = 125 kHz System clock = XIN	CPU clock = Divide-by-4, (f(BCLK) = 4 MHz) 1.8 V ≤ VCC ≤ 3.6 V	RF = off	—	2.5	—	mA
				RF = idle	—	4.0	—	mA
				RF = Tx	—	18	—	mA
				RF = Rx (reception standby)	—	24	—	mA
				RF = Rx (reception in progress)	—	25	—	mA
			CPU clock = Divide-by-2, (f(BCLK) = 8 MHz) 2.15 V ≤ VCC ≤ 3.6 V	RF = off	—	3.5	—	mA
				RF = idle	—	5.0	—	mA
				RF = Tx	—	19	—	mA
				RF = Rx (reception standby)	—	25	—	mA
				RF = Rx (reception in progress)	—	26	—	mA
			CPU clock = No division (f(BCLK) = 16 MHz) 2.7 V ≤ VCC ≤ 3.6 V	RF = off	—	6.0	—	mA
				RF = idle	—	7.5	—	mA
				RF = Tx	—	21.5	—	mA
				RF = Rx (reception standby)	—	27.5	—	mA
				RF = Rx (reception in progress)	—	28.5	—	mA
		Low-speed on-chip oscillator mode XIN clock off, XCIN clock off, Low-speed on-chip oscillator on: fOCO-S = 125 kHz System clock = fOCO-S, CPU clock = Divide-by-8 FMR27 = 1, VCA20 = 0 (flash memory low-current-consumption read mode)		RF = off	—	80	—	µA
		Low-speed clock mode XIN clock off XCIN clock oscillator on f(XCIN) = 32 kHz Low-speed on-chip oscillator off System clock = XCIN CPU clock = No division	FMR27 = 1 VCA20 = 0 (flash memory low-current-consumption read mode)	RF = off	—	95	—	µA
			FMSTP = 1 VCA20 = 0 (Flash memory off, program operation on RAM)	RF = off	—	45	—	µA
		Wait mode XIN clock oscillator on: f(XIN) = 16 MHz XCIN clock oscillator on: f(XCIN) = 32 kHz Low-speed on-chip oscillator on: fOCO-S = 125 kHz System clock = XIN While a WAIT instruction is executed		RF = Rx (reception standby)	—	23	—	mA
		Wait mode XIN clock off XCIN clock oscillator on f(XCIN) = 32 kHz Low-speed on-chip oscillator off System clock = XCIN While a WAIT instruction is executed	Peripheral function clock on VCA26 = VCA25 = 0 VCA20 = 1 (voltage detection circuit stopped, internal power consumption enabled)	RF = off	—	6.0	—	µA
			Peripheral function clock off VCA26 = VCA25 = 0 VCA20 = 1 (voltage detection circuit stopped, internal power consumption enabled)	RF = off	—	4.5	—	µA
		Wait mode XIN clock off XCIN clock oscillator on Low-speed on-chip oscillator on fOCO-S = 125 kHz System clock = fOCO-S While a WAIT instruction is executed	Peripheral function clock on VCA26 = VCA25 = 0 VCA20 = 1 (voltage detection circuit stopped, internal low power consumption enabled)	RF = off	—	13.0	—	µA
			Peripheral function clock off VCA26 = VCA25 = 0 VCA20 = 1 (voltage detection circuit stopped, internal low power consumption enabled)	RF = off	—	7.5	—	µA
		Stop mode (Topr = 25°C) XIN clock off, XCIN clock off, Low-speed on-chip oscillator off, VCA26 = VCA25 = 0 (voltage detection circuit stopped)		RF = off	—	2.0	—	µA

Table 5.14 Electrical Characteristics (2) [2.7 V ≤ Vcc ≤ 3.6 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” voltage	P0_4, P1, P3_0, P3_1, P3_3 to P3_5, P3_7, P4_3 to P4_5	Drive capacity High	I_{OH} = –5 mA	V_{CC} – 0.5	—	V_{CC}	V
			Drive capacity Low	I_{OH} = –1 mA	V_{CC} – 0.5	—	V_{CC}	V
V_{OL}	Output “L” voltage	P0_4, P1, P3_0, P3_1, P3_3 to P3_5, P3_7, P4_3 to P4_5	Drive capacity High	I_{OL} = 5 mA	—	—	0.5	V
			Drive capacity Low	I_{OL} = 1 mA	—	—	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, $\overline{KI4}$, $\overline{KI6}$, $\overline{KI7}$, TRAIO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRCTRG, TRCCLK, RXD0, CLK0, SSI, SCL, SDA, SSO	VCC = 3.0 V		0.1	0.4	—	V
		$\overline{RESET}$	VCC = 3.0 V		0.1	0.5	—	V
I_{IH}	Input “H” current		V_I = 3 V, V_{CC} = 3.0 V		—	—	4.0	µA
I_{IL}	Input “L” current		V_I = 0 V, V_{CC} = 3.0 V		—	—	–4.0	µA
R_{PULLUP}	Pull-up resistance		V_I = 0 V, V_{CC} = 3.0 V		42	84	168	kΩ
R_{fXIN}	Feedback resistance	XIN			—	0.3	—	MΩ
R_{fXCIN}	Feedback resistance	XCIN			—	8	—	MΩ
V_{RAM}	RAM hold voltage		During stop mode		1.8	—	3.6	V

Note:
1. 2.7 V ≤ V_{CC} ≤ 3.6 V, T_{opr} = –20°C to 85°C, and f(XIN) =16 MHz, unless otherwise specified.

Timing requirements (VCC = 3 V, Topr = −20°C to 85°C, unless otherwise specified)

Table 5.15 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	300	—	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	120	—	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	120	—	ns

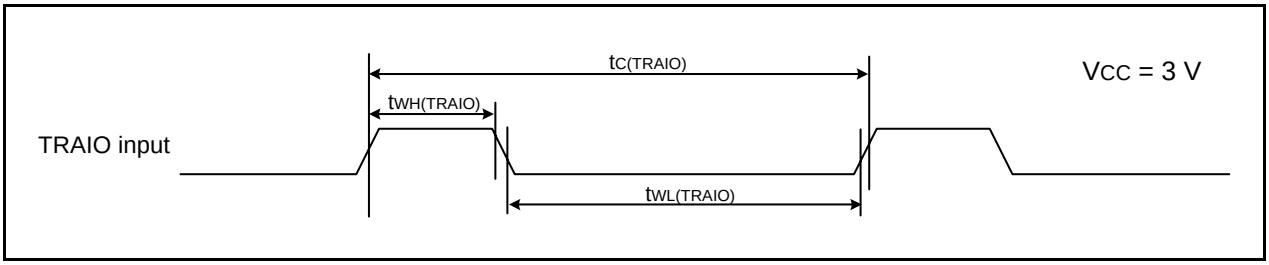


Figure 5.8 TRAIO Input Timing Diagram when VCC = 3 V

Table 5.16 Serial Interface

Symbol	Parameter		Standard		Unit
			Min.	Max.	
$t_{c(CK)}$	CLK0 input cycle time	When an external clock is selected	300	—	ns
$t_{W(CKH)}$	CLK0 input “H” width		150	—	ns
$t_{W(CKL)}$	CLK0 Input “L” width		150	—	ns
$t_{d(C-Q)}$	TXD0 output delay time		—	120	ns
$t_{h(C-Q)}$	TXD0 hold time		0	—	ns
$t_{su(D-C)}$	RXD0 input setup time		30	—	ns
$t_{h(C-D)}$	RXD0 input hold time		90	—	ns
$t_{h(C-Q)}$	TXD0 output delay time	When an internal clock is selected	—	30	ns
$t_{su(D-C)}$	RXD0 input setup time		120	—	ns
$t_{h(C-D)}$	RXD0 input hold time		90	—	ns

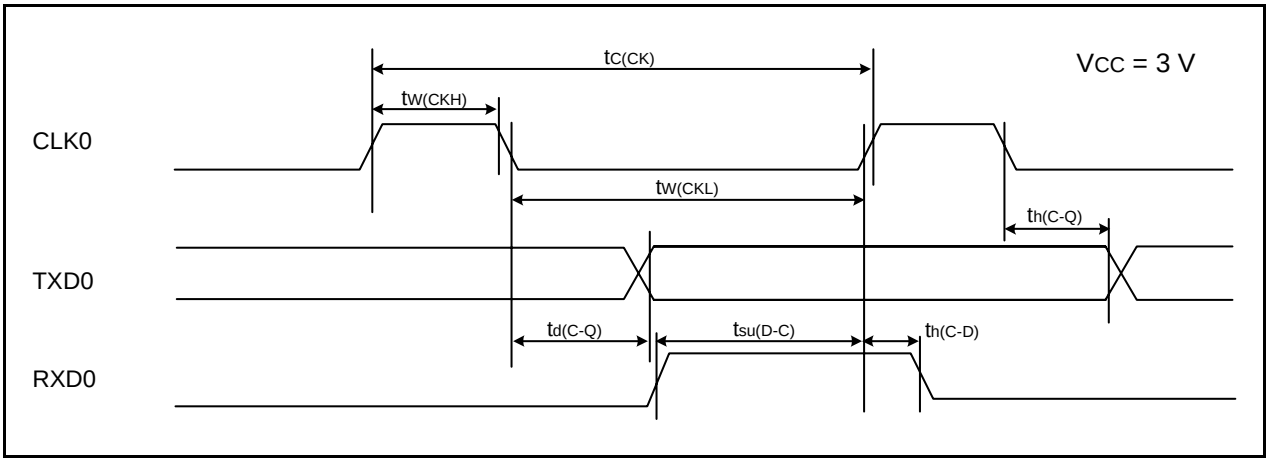


Figure 5.9 Serial Interface Timing Diagram when VCC = 3 V

Timing requirements (VCC = 2.15 V, Topr = –20°C to 85°C, unless otherwise specified)

Table 5.19 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	500	—	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	200	—	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	200	—	ns

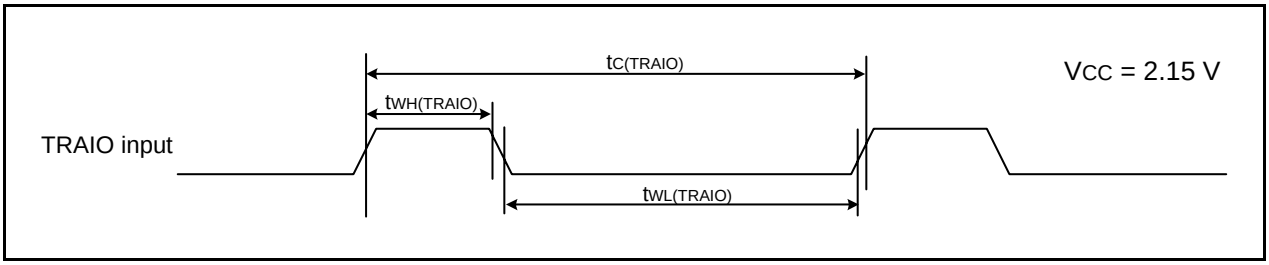


Figure 5.11 TRAIO Input Timing Diagram when VCC = 2.15 V

Table 5.20 Serial Interface

Symbol	Parameter		Standard		Unit
			Min.	Max.	
$t_{c(CK)}$	CLK0 input cycle time	When an external clock is selected	800	—	ns
$t_{W(CKH)}$	CLK0 input “H” width		400	—	ns
$t_{W(CKL)}$	CLK0 input “L” width		400	—	ns
$t_{d(C-Q)}$	TXD0 output delay time		—	200	ns
$t_{h(C-Q)}$	TXD0 hold time		0	—	ns
$t_{su(D-C)}$	RXD0 input setup time		150	—	ns
$t_{h(C-D)}$	RXD0 input hold time		90	—	ns
$t_{h(C-Q)}$	TXD0 output delay time	When an internal clock is selected	—	200	ns
$t_{su(D-C)}$	RXD0 input setup time		150	—	ns
$t_{h(C-D)}$	RXD0 input hold time		90	—	ns

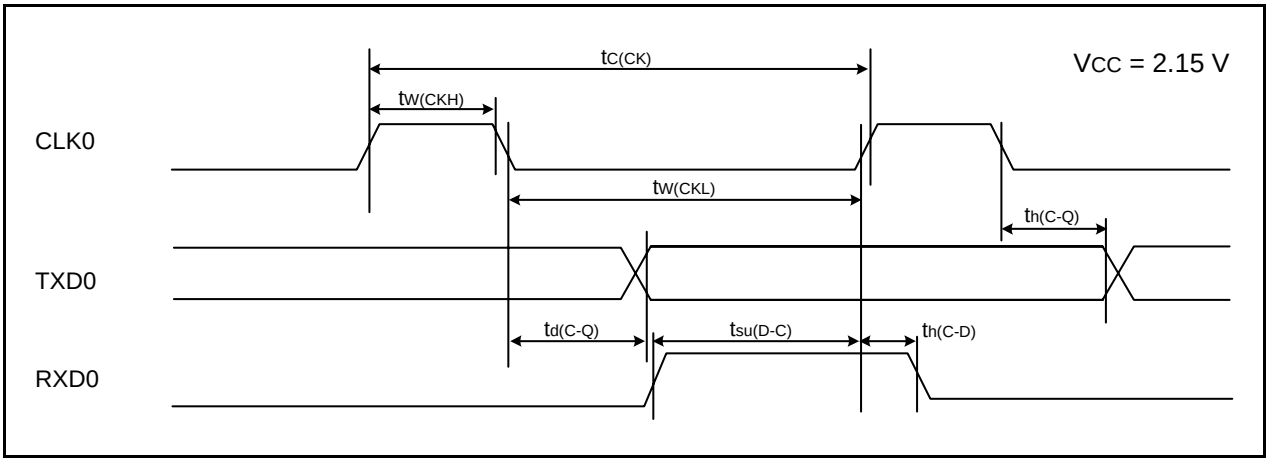


Figure 5.12 Serial Interface Timing Diagram when VCC = 2.15 V

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