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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

|                            |   |
|----------------------------|---|
| Product Status             | Active  |
| Core Processor             | AVR   |
| Core Size                  | 8-Bit   |
| Speed                      | 12MHz   |
| Connectivity               | I <sup>2</sup> C, SPI   |
| Peripherals                | Brown-out Detect/Reset, POR, PWM, WDT   |
| Number of I/O              | 18  |
| Program Memory Size        | 4KB (2K x 16)   |
| Program Memory Type        | FLASH   |
| EEPROM Size                | -   |
| RAM Size                   | 256 x 8   |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 5.5V   |
| Data Converters            | A/D 12x10b  |
| Oscillator Type            | Internal  |
| Operating Temperature      | -40°C ~ 85°C (TA)   |
| Mounting Type              | Surface Mount   |
| Package / Case             | 20-SOIC (0.295", 7.50mm Width)  |
| Supplier Device Package    | 20-SOIC   |
| Purchase URL               | <a href="https://www.e-xfl.com/product-detail/atmel/attiny40-su">https://www.e-xfl.com/product-detail/atmel/attiny40-su</a> |



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# 8-bit Atmel tinyAVR Microcontroller with 4K Bytes In-System Programmable Flash

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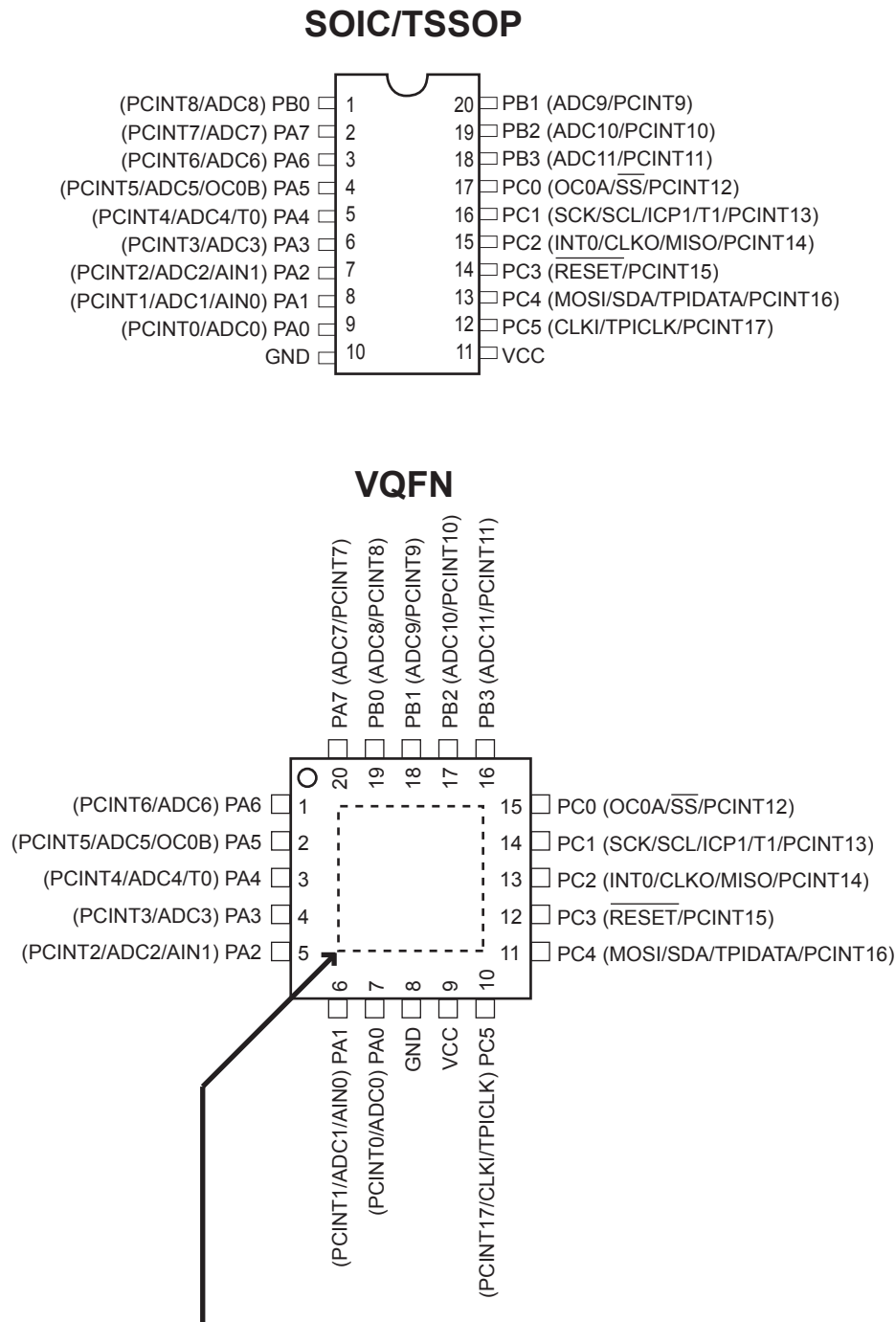
## ATtiny40 SUMMARY DATASHEET

### Features

- High Performance, Low Power AVR® 8-Bit Microcontroller
- Advanced RISC Architecture
  - 54 Powerful Instructions – Most Single Clock Cycle Execution
  - 16 x 8 General Purpose Working Registers
  - Fully Static Operation
  - Up to 12 MIPS Throughput at 12 MHz
- Non-volatile Program and Data Memories
  - 4K Bytes of In-System Programmable Flash Program Memory
  - 256 Bytes Internal SRAM
  - Flash Write/Erase Cycles: 10,000
  - Data Retention: 20 Years at 85°C / 100 Years at 25°C
- Peripheral Features
  - One 8-bit Timer/Counter with Two PWM Channels
  - One 8/16-bit Timer/Counter
  - 10-bit Analog to Digital Converter
    - 12 Single-Ended Channels
  - Programmable Watchdog Timer with Separate On-chip Oscillator
  - On-chip Analog Comparator
  - Master/Slave SPI Serial Interface
  - Slave TWI Serial Interface
- Special Microcontroller Features
  - In-System Programmable
  - External and Internal Interrupt Sources
  - Low Power Idle, ADC Noise Reduction, Stand-by and Power-down Modes
  - Enhanced Power-on Reset Circuit
  - Internal Calibrated Oscillator
- I/O and Packages
  - 20-pin SOIC: 18 Programmable I/O Lines
  - 20-pin TSSOP: 18 Programmable I/O Lines
  - 20-pad VQFN: 18 Programmable I/O Lines
- Operating Voltage:
  - 1.8 – 5.5V
- Programming Voltage:
  - 5V
- Speed Grade
  - 0 – 4 MHz @ 1.8 – 5.5V
  - 0 – 8 MHz @ 2.7 – 5.5V
  - 0 – 12 MHz @ 4.5 – 5.5V
- Industrial Temperature Range
- Low Power Consumption
  - Active Mode:
    - 200 µA at 1 MHz and 1.8V
  - Idle Mode:
    - 25 µA at 1 MHz and 1.8V
  - Power-down Mode:
    - < 0.1 µA at 1.8V

# 1. Pin Configurations

Figure 1-1. Pinout of ATtiny40



## 1.1 Pin Description

### 1.1.1 VCC

Supply voltage.

### 1.1.2 GND

Ground.

### 1.1.3 $\overline{\text{RESET}}$

Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running and provided the reset pin has not been disabled. The minimum pulse length is given in [Table 20-4 on page 155](#). Shorter pulses are not guaranteed to generate a reset.

The reset pin can also be used as a (weak) I/O pin.

### 1.1.4 Port A (PA7:PA0)

Port A is a 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port A output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port A pins that are externally pulled low will source current if the pull-up resistors are activated. The Port A pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port A has alternate functions as analog inputs for the ADC, analog comparator and pin change interrupt as described in [“Alternate Port Functions” on page 47](#).

### 1.1.5 Port B (PB3:PB0)

Port B is a 4-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

The port also serves the functions of various special features of the ATtiny40, as listed on [page 37](#).

### 1.1.6 Port C (PC5:PC0)

Port C is a 6-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port C output buffers have symmetrical drive characteristics with both high sink and source capability except PC3 which has the  $\overline{\text{RESET}}$  capability. To use pin PC3 as an I/O pin, instead of RESET pin, program ('0') RSTDISBL fuse. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. The Port C pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port C has alternate functions as analog inputs for the ADC, analog comparator and pin change interrupt as described in [“Alternate Port Functions” on page 47](#).

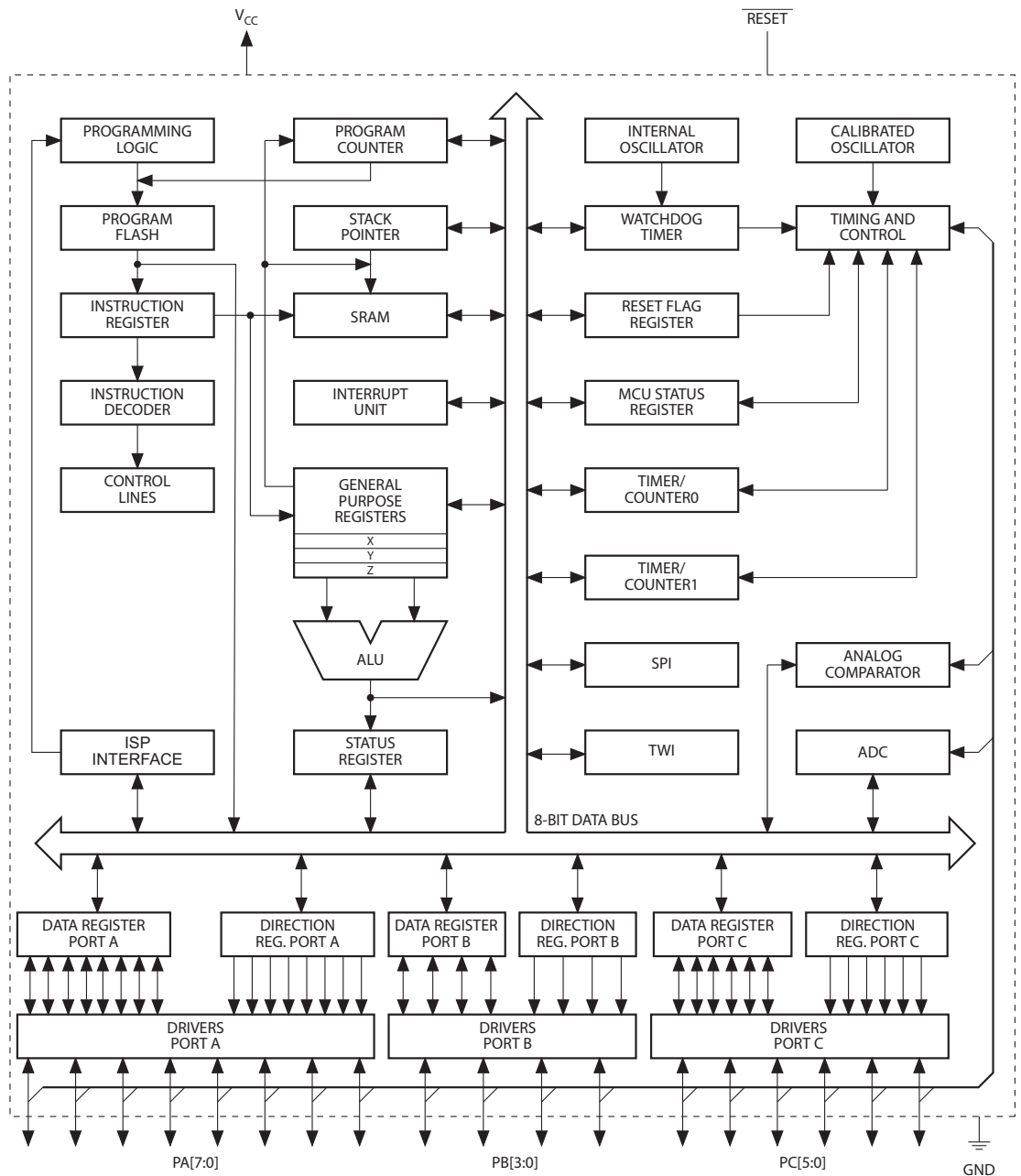
The port also serves the functions of various special features of the ATtiny40, as listed on [page 37](#).

## 2. Overview

ATtiny40 is a low-power CMOS 8-bit microcontroller based on the compact AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATtiny40 achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

### Figure 2-1. Block Diagram

The AVR core combines a rich instruction set with 16 general purpose working registers and system registers. All registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be



accessed in one single instruction executed in one clock cycle. The resulting architecture is compact and code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATtiny40 provides the following features: 4K bytes of In-System Programmable Flash, 256 bytes of SRAM, twelve general purpose I/O lines, 16 general purpose working registers, an 8-bit Timer/Counter with two PWM channels, a 8/16-bit Timer/Counter, Internal and External Interrupts, an eight-channel, 10-bit ADC, a programmable Watchdog Timer with internal oscillator, a slave two-wire interface, a master/slave serial peripheral interface, an internal calibrated oscillator, and four software selectable power saving modes.

Idle mode stops the CPU while allowing the Timer/Counter, ADC, Analog Comparator, SPI, TWI, and interrupt system to continue functioning. ADC Noise Reduction mode minimizes switching noise during ADC conversions by stopping the CPU and all I/O modules except the ADC. In Power-down mode registers keep their contents and all chip functions are disabled until the next interrupt or hardware reset. In Standby mode, the oscillator is running while the rest of the device is sleeping, allowing very fast start-up combined with low power consumption.

The device is manufactured using Atmel's high density non-volatile memory technology. The on-chip, in-system programmable Flash allows program memory to be re-programmed in-system by a conventional, non-volatile memory programmer.

The ATtiny40 AVR is supported by a suite of program and system development tools, including macro assemblers and evaluation kits.

## 3. General Information

### 3.1 Resources

A comprehensive set of drivers, application notes, data sheets and descriptions on development tools are available for download at <http://www.atmel.com/avr>.

### 3.2 Code Examples

This documentation contains simple code examples that briefly show how to use various parts of the device. These code examples assume that the part specific header file is included before compilation. Be aware that not all C compiler vendors include bit definitions in the header files and interrupt handling in C is compiler dependent. Please confirm with the C compiler documentation for more details.

### 3.3 Capacitive Touch Sensing

Atmel QTouch Library provides a simple to use solution for touch sensitive interfaces on Atmel AVR microcontrollers. The QTouch Library includes support for QTouch<sup>®</sup> and QMatrix<sup>®</sup> acquisition methods.

Touch sensing is easily added to any application by linking the QTouch Library and using the Application Programming Interface (API) of the library to define the touch channels and sensors. The application then calls the API to retrieve channel information and determine the state of the touch sensor.

The QTouch Library is free and can be downloaded from the Atmel website. For more information and details of implementation, refer to the QTouch Library User Guide – also available from the Atmel website.

### 3.4 Data Retention

Reliability Qualification results show that the projected data retention failure rate is much less than 1 PPM over 20 years at 85°C or 100 years at 25°C.

### 3.5 Disclaimer

Typical values contained in this datasheet are based on simulations and characterization of other AVR microcontrollers manufactured on the same process technology.

## 4. CPU Core

This section discusses the AVR core architecture in general. The main function of the CPU core is to ensure correct program execution. The CPU must therefore be able to access memories, perform calculations, control peripherals, and handle interrupts.

## 5. Register Summary

| Address | Name     | Bit 7                                       | Bit 6      | Bit 5                | Bit 4   | Bit 3   | Bit 2   | Bit 1      | Bit 0   | Page          |
|---------|----------|---|------------|----------------------|---------|---------|---------|------------|---------|---------------|
| 0x3F    | SREG     | I   | T          | H                    | S       | V       | N       | Z          | C       | Page 12       |
| 0x3E    | SPH      | Stack Pointer High Byte                     |            |                      |         |         |         |            |         | Page 12       |
| 0x3D    | SPL      | Stack Pointer Low Byte                      |            |                      |         |         |         |            |         | Page 12       |
| 0x3C    | CCP      | CPU Change Protection Register              |            |                      |         |         |         |            |         | Page 11       |
| 0x3B    | RSTFLR   | –   | –          | –                    | –       | WDRF    | BORF    | EXTRF      | PORF    | Page 35       |
| 0x3A    | MCUCR    | ISC01                                       | ISC00      | –                    | BODS    | SM2     | SM1     | SM0        | SE      | Pages 26, 38  |
| 0x39    | OSCCAL   | Oscillator Calibration Register             |            |                      |         |         |         |            |         | Page 23       |
| 0x38    | Reserved | –   |            |                      |         |         |         |            |         |               |
| 0x37    | CLKMSR   | –   | –          | –                    | –       | –       | –       | CLKMS1     | CLKMS0  | Page 21       |
| 0x36    | CLKPSR   | –   | –          | –                    | –       | CLKPS3  | CLKPS2  | CLKPS1     | CLKPS0  | Page 22       |
| 0x35    | PRR      | –   | –          | –                    | PRTWI   | PRSPI   | PRTIM1  | PRTIM0     | PRADC   | Page 27       |
| 0x34    | QTCR     | QTouch Control and Status Register          |            |                      |         |         |         |            |         | Page 5        |
| 0x33    | NVMCMD   | –   | –          | NVM Command Register |         |         |         |            |         | Page 151      |
| 0x32    | NVMCSR   | NVMBSY                                      | –          | –                    | –       | –       | –       | –          | –       | Page 151      |
| 0x31    | WDTCR    | WDIF  | WDIE       | WDP3                 | –       | WDE     | WDP2    | WDP1       | WDP0    | Page 33       |
| 0x30    | SPCR     | SPIE  | SPE        | DORD                 | MSTR    | CPOL    | CPHA    | SPR1       | SPR0    | Page 120      |
| 0x2F    | SPSR     | SPIF  | WCOL       | –                    | –       | –       | –       | –          | SPI2X   | Page 121      |
| 0x2E    | SPDR     | SPI Data Register                           |            |                      |         |         |         |            |         | Page 122      |
| 0x2D    | TWSCRA   | TWSHE                                       | –          | TWDIE                | TWASIE  | TWEN    | TWSIE   | TWPME      | TWSME   | Page 130      |
| 0x2C    | TWSCR    | –   | –          | –                    | –       | –       | TWAA    | TWCMD[1,0] |         | Page 130      |
| 0x2B    | TWSSRA   | TWDIF                                       | TWASIF     | TWCH                 | TWRA    | TWC     | TWBE    | TWDIR      | TWAS    | Page 131      |
| 0x2A    | TWSA     | TWI Slave Address Register                  |            |                      |         |         |         |            |         | Page 133      |
| 0x29    | TWSAM    | TWI Slave Address Mask Register             |            |                      |         |         |         |            |         | Page 133      |
| 0x28    | TWSD     | TWI Slave Data Register                     |            |                      |         |         |         |            |         | Page 133      |
| 0x27    | TCNT1H   | Timer/Counter1 – Counter Register High Byte |            |                      |         |         |         |            |         | Page 89       |
| 0x26    | TIMSK    | ICIE1                                       | –          | OCIE1B               | OCIE1A  | TOIE1   | OCIE0B  | OCIE0A     | TOIE0   | Pages 75, 90  |
| 0x25    | TIFR     | ICF1  | –          | OCF1B                | OCF1A   | TOV1    | OCF0B   | OCF0A      | TOV0    | Pages 76, 90  |
| 0x24    | TCCR1A   | TCW1  | ICEN1      | ICNC1                | ICES1   | CTC1    | CS12    | CS11       | CS10    | Page 88       |
| 0x23    | TCNT1L   | Timer/Counter1 – Counter Register Low Byte  |            |                      |         |         |         |            |         | Page 89       |
| 0x22    | OCR1A    | Timer/Counter1 – Compare Register A         |            |                      |         |         |         |            |         | Page 89       |
| 0x21    | OCR1B    | Timer/Counter1 – Compare Register B         |            |                      |         |         |         |            |         | Page 89       |
| 0x20    | RAMAR    | RAM Address Register                        |            |                      |         |         |         |            |         | Page 17       |
| 0x1F    | RAMDR    | RAM Data Register                           |            |                      |         |         |         |            |         | Page 17       |
| 0x1E    | PUEC     | –   | –          | PUEC5                | PUEC4   | PUEC3   | PUEC2   | PUEC1      | PUEC0   | Page 59       |
| 0x1D    | PORTC    | –   | –          | PORTC5               | PORTC4  | PORTC3  | PORTC2  | PORTC1     | PORTC0  | Page 59       |
| 0x1C    | DDRC     | –   | –          | DDRC5                | DDRC4   | DDRC3   | DDRC2   | DDRC1      | DDRC0   | Page 59       |
| 0x1B    | PINC     | –   | –          | PINC5                | PINC4   | PINC3   | PINC2   | PINC1      | PINC0   | Page 59       |
| 0x1A    | PCMSK2   | –   | –          | PCINT17              | PCINT16 | PCINT15 | PCINT14 | PCINT13    | PCINT12 | Page 40       |
| 0x19    | TCCR0A   | COM0A1                                      | COM0A0     | COM0B1               | COM0B0  | –       | –       | WGM01      | WGM00   | Page 71       |
| 0x18    | TCCR0B   | FOC0A                                       | FOC0B      | TSM                  | PSR     | WGM02   | CS02    | CS01       | CS00    | Pages 74, 93  |
| 0x17    | TCNT0    | Timer/Counter0 – Counter Register           |            |                      |         |         |         |            |         | Page 75       |
| 0x16    | OCR0A    | Timer/Counter0 – Compare Register A         |            |                      |         |         |         |            |         | Page 75       |
| 0x15    | OCR0B    | Timer/Counter0 – Compare Register B         |            |                      |         |         |         |            |         | Page 75       |
| 0x14    | ACSR     | ACD   | ACBG/ACIRE | ACO                  | ACI     | ACIE    | ACIC    | ACIS1      | ACIS0   | Page 95       |
| 0x13    | ACSRB    | HSEL  | HLEV       | ACLP                 | –       | ACCE    | ACME    | ACIRS1     | ACIRS0  | Page 96       |
| 0x12    | ADCSRA   | ADEN  | ADSC       | ADATE                | ADIF    | ADIE    | ADPS2   | ADPS1      | ADPS0   | Page 111      |
| 0x11    | ADCSRB   | VDEN  | VDPD       | –                    | –       | ADLAR   | ADTS2   | ADTS1      | ADTS0   | Page 112      |
| 0x10    | ADMUX    | –   | REFS       | REFEN                | ADC0EN  | MUX3    | MUX2    | MUX1       | MUX0    | Page 109      |
| 0x0F    | ADCH     | ADC Conversion Result – High Byte           |            |                      |         |         |         |            |         | Page 111      |
| 0x0E    | ADCL     | ADC Conversion Result – Low Byte            |            |                      |         |         |         |            |         | Page 111      |
| 0x0D    | DIDR0    | ADC7D                                       | ADC6D      | ADC5D                | ADC4D   | ADC3D   | ADC2D   | ADC1D      | ADC0D   | Pages 97, 113 |
| 0x0C    | GIMSK    | –   | PCIE2      | PCIE1                | PCIE0   | –       | –       | –          | INT0    | Page 39       |
| 0x0B    | GIFR     | –   | PCIF2      | PCIF1                | PCIF0   | –       | –       | –          | INTF0   | Page 40       |
| 0x0A    | PCMSK1   | –   | –          | –                    | –       | PCINT11 | PCINT10 | PCINT9     | PCINT8  | Page 41       |
| 0x09    | PCMSK0   | PCINT7                                      | PCINT6     | PCINT5               | PCINT4  | PCINT3  | PCINT2  | PCINT1     | PCINT0  | Page 41       |
| 0x08    | PORTCR   | ADC11D                                      | ADC10D     | ADC9D                | ADC8D   | –       | BBMC    | BBMB       | BBMA    | Pages 58, 113 |
| 0x07    | PUEB     | –   | –          | –                    | –       | PUEB3   | PUEB2   | PUEB1      | PUEB0   | Page 59       |
| 0x06    | PORTB    | –   | –          | –                    | –       | PORTB3  | PORTB2  | PORTB1     | PORTB0  | Page 59       |
| 0x05    | DDRB     | –   | –          | –                    | –       | DDRB3   | DDRB2   | DDRB1      | DDRB0   | Page 59       |
| 0x04    | PINB     | –   | –          | –                    | –       | PINB3   | PINB2   | PINB1      | PINB0   | Page 59       |
| 0x03    | PUEA     | PUEA7                                       | PUEA6      | PUEA5                | PUEA4   | PUEA3   | PUEA2   | PUEA1      | PUEA0   | Page 58       |
| 0x02    | PORTA    | PORTA7                                      | PORTA6     | PORTA5               | PORTA4  | PORTA3  | PORTA2  | PORTA1     | PORTA0  | Page 58       |
| 0x01    | DDRA     | DDRA7                                       | DDRA6      | DDRA5                | DDRA4   | DDRA3   | DDRA2   | DDRA1      | DDRA0   | Page 58       |
| 0x00    | PINA     | PINA7                                       | PINA6      | PINA5                | PINA4   | PINA3   | PINA2   | PINA1      | PINA0   | Page 59       |

Note: 1. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses

should never be written.

2. I/O Registers within the address range 0x00 - 0x1F are directly bit-accessible using the SBI and CBI instructions. In these registers, the value of single bits can be checked by using the SBIS and SBIC instructions.
3. Some of the Status Flags are cleared by writing a logical one to them. Note that, unlike most other AVR's, the CBI and SBI instructions will only operation the specified bit, and can therefore be used on registers containing such Status Flags. The CBI and SBI instructions work with registers 0x00 to 0x1F only.

## 6. Ordering Information

| Speed (MHz) | Power Supply | Ordering Code <sup>(1)</sup>  | Package <sup>(2)</sup>   | Operational Range                             |
|-------------|--------------|---|--|---|
| 12          | 1.8 - 5.5V   | ATtiny40-SU<br>ATtiny40-SUR<br>ATtiny40-XU<br>ATtiny40-XUR<br>ATtiny40-MMH <sup>(3)</sup><br>ATtiny40-MMHR <sup>(3)</sup> | 20S2<br>20S2<br>20X<br>20X<br>20M2 <sup>(3)</sup><br>20M2 <sup>(3)</sup> | Industrial<br>(-40°C to +85°C) <sup>(4)</sup> |

Notes: 1. Code indicators:

- H: NiPdAu lead finish
- U: matte tin
- R: tape & reel

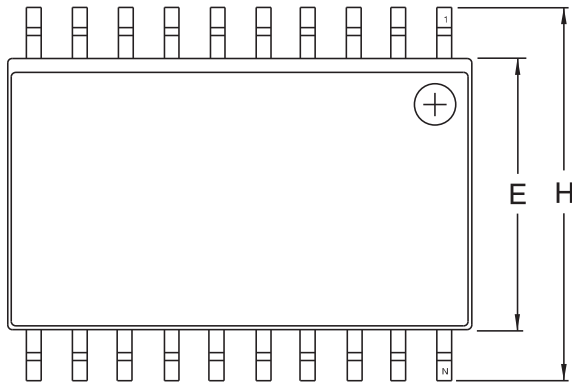
2. All packages are Pb-free, halide-free and fully green and they comply with the European directive for Restriction of Hazardous Substances (RoHS).
3. Topside marking for ATtiny40:
  - 1st Line: T40
  - 2nd & 3rd Line: manufacturing data
4. These devices can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.

| Package Type |   |
|--------------|---|
| <b>20S2</b>  | 20-lead, 0.300" Wide Body, Plastic Gull Wing Small Outline Package (SOIC) |
| <b>20X</b>   | 20-lead, 4.4 mm Body, Plastic Thin Shrink Small Outline Package (TSSOP)   |
| <b>20M2</b>  | 20-pad, 3 x 3 x 0.85 mm Body, Very Thin Quad Flat No Lead Package (VQFN)  |

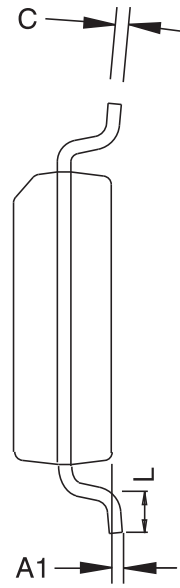


## 7. Packaging Information

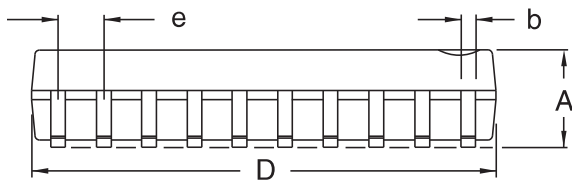
### 7.1 20S2



Top View



End View



Side View

COMMON DIMENSIONS  
(Unit of Measure – mm)

| SYMBOL | MIN      | NOM | MAX   | NOTE |
|--------|----------|-----|-------|------|
| A      | 2.35     |     | 2.65  |      |
| A1     | 0.10     |     | 0.30  |      |
| b      | 0.33     |     | 0.51  | 4    |
| C      | 0.23     |     | 0.32  |      |
| D      | 12.60    |     | 13.00 | 1    |
| E      | 7.40     |     | 7.60  | 2    |
| H      | 10.00    |     | 10.65 |      |
| L      | 0.40     |     | 1.27  | 3    |
| e      | 1.27 BSC |     |       |      |

- Notes.
1. This drawing is for general information only; refer to JEDEC Drawing MS-013, Variation AC for additional information.
  2. Dimension 'D' does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15 mm (0.006') per side.
  3. Dimension 'E' does not include inter-lead Flash or protrusion. Inter-lead Flash and protrusions shall not exceed 0.25 mm (0.010') per side.
  4. 'L' is the length of the terminal for soldering to a substrate.
  5. The lead width 'b', as measured 0.36 mm (0.014') or greater above the seating plane, shall not exceed a maximum value of 0.61 mm (0.024') per side.

11/6/06



2325 Orchard Parkway  
San Jose, CA 95131

**TITLE**

**20S2**, 20-lead, 0.300' Wide Body, Plastic Gull Wing Small Outline Package (SOIC)

**DRAWING NO.**

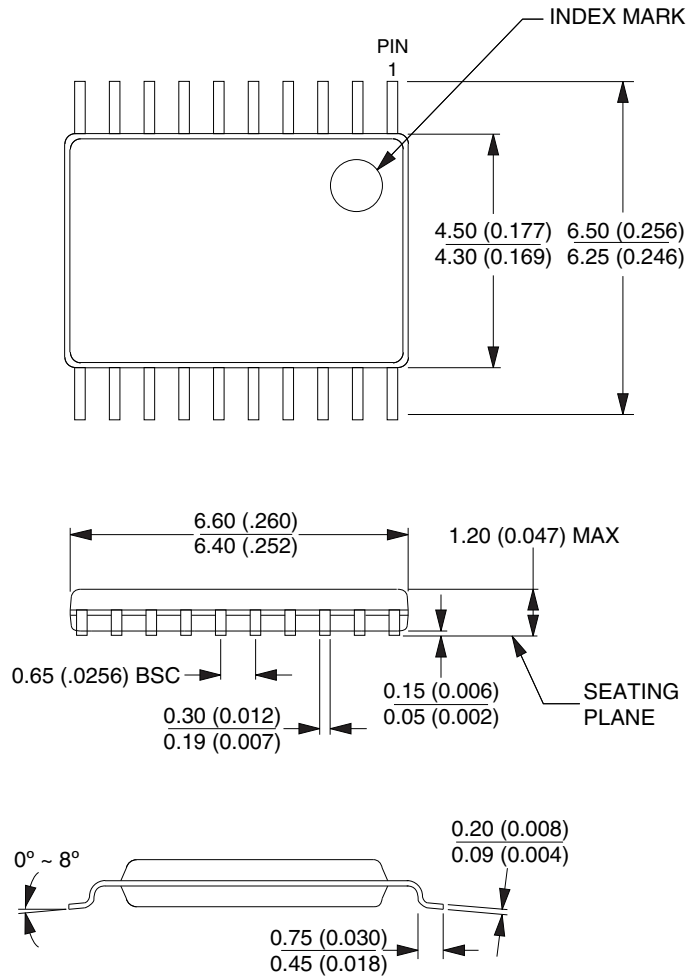
20S2

**REV.**

B

7.2 20X

Dimensions in Millimeters and (Inches).  
 Controlling dimension: Millimeters.  
 JEDEC Standard MO-153 AC



10/23/03



2325 Orchard Parkway  
 San Jose, CA 95131

**TITLE**

**20X**, (Formerly 20T), 20-lead, 4.4 mm Body Width,  
 Plastic Thin Shrink Small Outline Package (TSSOP)

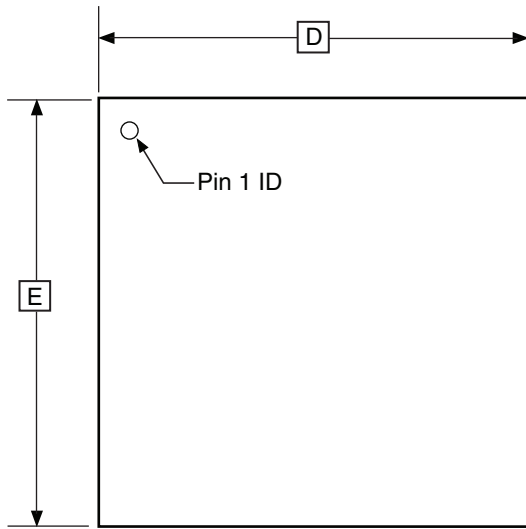
**DRAWING NO.**

20X

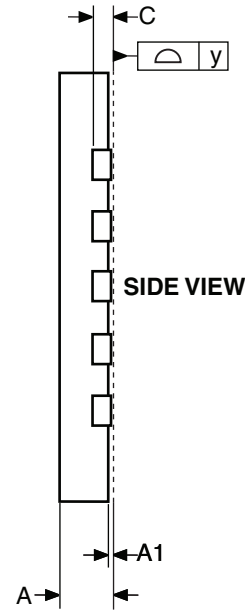
**REV.**

C

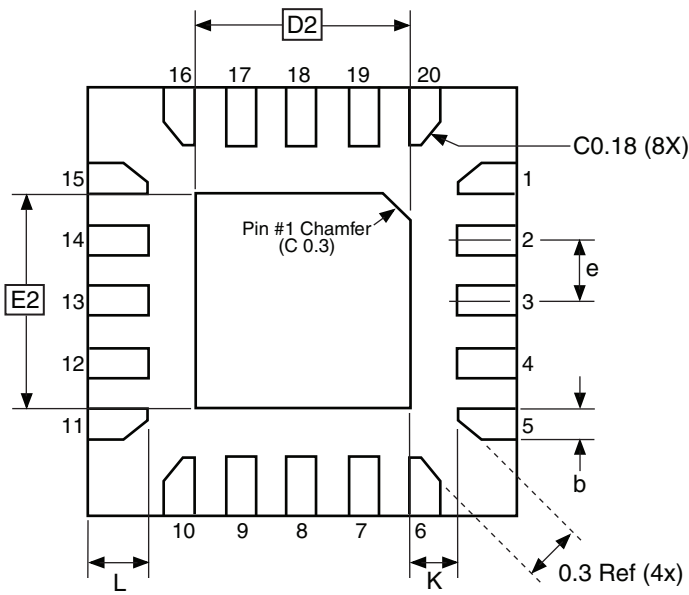
7.3 20M2



TOP VIEW



SIDE VIEW



BOTTOM VIEW

COMMON DIMENSIONS  
(Unit of Measure = mm)

| SYMBOL | MIN   | NOM  | MAX  | NOTE |
|--------|-------|------|------|------|
| A      | 0.75  | 0.80 | 0.85 |      |
| A1     | 0.00  | 0.02 | 0.05 |      |
| b      | 0.17  | 0.22 | 0.27 |      |
| C      | 0.152 |      |      |      |
| D      | 2.90  | 3.00 | 3.10 |      |
| D2     | 1.40  | 1.55 | 1.70 |      |
| E      | 2.90  | 3.00 | 3.10 |      |
| E2     | 1.40  | 1.55 | 1.70 |      |
| e      | -     | 0.45 | -    |      |
| L      | 0.35  | 0.40 | 0.45 |      |
| K      | 0.20  | -    | -    |      |
| y      | 0.00  | -    | 0.08 |      |

10/24/08



Package Drawing Contact:  
packagedrawings@atmel.com

**TITLE**  
20M2, 20-pad, 3 x 3 x 0.85 mm Body, Lead Pitch 0.45 mm,  
1.55 x 1.55 mm Exposed Pad, Thermally Enhanced  
Plastic Very Thin Quad Flat No Lead Package (VQFN)

**GPC**

ZFC

**DRAWING NO.**

20M2

**REV.**

B

## 8. Errata

The revision letters in this section refer to the revision of the corresponding ATtiny40 device.

### 8.1 Rev. B

- MISO output driver is not disabled by Slave Select ( $\overline{SS}$ ) signal.
- Current consumption in sleep modes may exceed specifications.

#### 1. MISO output driver is not disabled by Slave Select ( $\overline{SS}$ ) signal.

When SPI is configured as a slave and the MISO pin is configured as an output the pin output driver is constantly enabled, even when the  $\overline{SS}$  pin is high. If other slave devices are connected to the same MISO line this behaviour may cause drive contention.

##### **Problem Fix / Workaround**

Monitor  $\overline{SS}$  pin by software and use the DDRC2 bit of DDRC to control the MISO pin driver.

#### 2. Current consumption in sleep mode may exceed specifications.

Some settings of register R27 may increase current consumption in sleep mode.

##### **Problem Fix / Workaround**

Before entering sleep mode, make sure register R27 is not loaded with 0x00 or 0x01.

### 8.2 Rev. A

Not sampled.



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