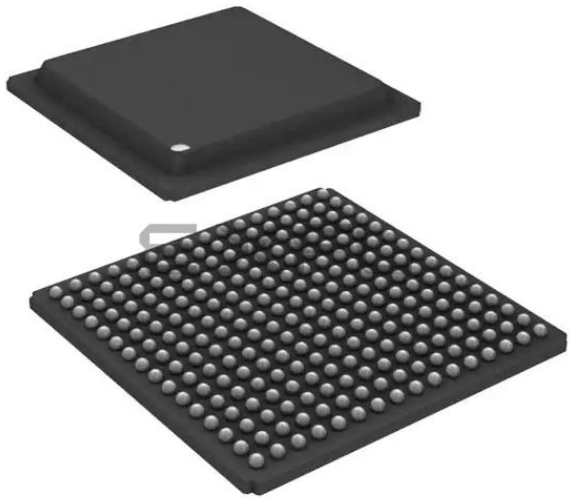

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	100MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 95°C (TA)
Security Features	-
Package / Case	256-BBGA
Supplier Device Package	256-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc852tvr100

2 Features

The MPC852T is comprised of three modules that each use the 32-bit internal bus: the MPC8xx core, the system integration unit (SIU), and the communication processor module (CPM). Figure 1 shows the MPC852T block diagram.

The following list summarizes the key MPC852T features:

- Embedded MPC8xx core up to 100 MHz
- Maximum frequency operation of the external bus is 66 MHz
  - The 50 MHz / 66 MHz core frequencies support both 1:1 and 2:1 modes.
  - The 80 MHz / 100 MHz core frequencies support 2:1 mode only.
- Single-issue, 32-bit core (compatible with the PowerPC architecture definition) with 32 32-bit general-purpose registers (GPRs)
  - The core performs branch prediction with conditional prefetch, without conditional execution.
  - 4-Kbyte data cache and 4-Kbyte instruction cache
    - 4-Kbyte instruction cache is two-way, set-associative with 128 sets.
    - 4-Kbyte data cacheis two-way, set-associative with 128 sets.
    - Cache coherency for both instruction and data caches is maintained on 128-bit (4-word) cache blocks.
    - Caches are physically addressed, implement a least recently used (LRU) replacement algorithm, and are lockable on a cache block basis.
  - MMUs with 32-entry TLB, fully associative instruction, and data TLBs
  - MMUs support multiple page sizes of 4, 16, and 512 Kbytes, and 8 Mbytes; 16 virtual address spaces, and 16 protection groups
- Up to 32-bit data bus (dynamic bus sizing for 8, 16, and 32 bits)
- 32 address lines
- Memory controller (eight banks)
  - Contains complete dynamic RAM (DRAM) controller
  - Each bank can be a chip select or $\overline{\text{RAS}}$ to support a DRAM bank
  - Up to 30 wait states programmable per memory bank
  - Glueless interface to DRAM, SIMMS, SRAM, EPROMs, Flash EPROMs, and other memory devices
  - DRAM controller-programmable to support most size and speed memory interfaces
  - Four $\overline{\text{CAS}}$ lines, four $\overline{\text{WE}}$ lines, and one $\overline{\text{OE}}$ line
  - Boot chip-select available at reset (options for 8-, 16-, or 32-bit memory)
  - Variable block sizes (32 Kbytes–256 Mbytes)
  - Selectable write protection
  - On-chip bus arbitration logic
- Fast Ethernet Controller (FEC)
- General-purpose timers
  - Two 16-bit timers or one 32-bit timer
  - Gate mode can enable or disable counting.
  - Interrupt can be masked on reference match and event capture.

  - Supports one independent PCMCIA socket; 8-memory or I/O windows supported
- Debug interface
  - Eight comparators: four operate on instruction address, two operate on data address, and two operate on data
  - Supports conditions: = ≠ < >
  - Each watchpoint can generate a break point internally.
- Normal high and normal low power modes to conserve power
- 1.8 V Core and 3.3 V I/O operation with 5-V TTL compatibility. Refer to Table 5 for a listing of the 5-V Tolerant pins.

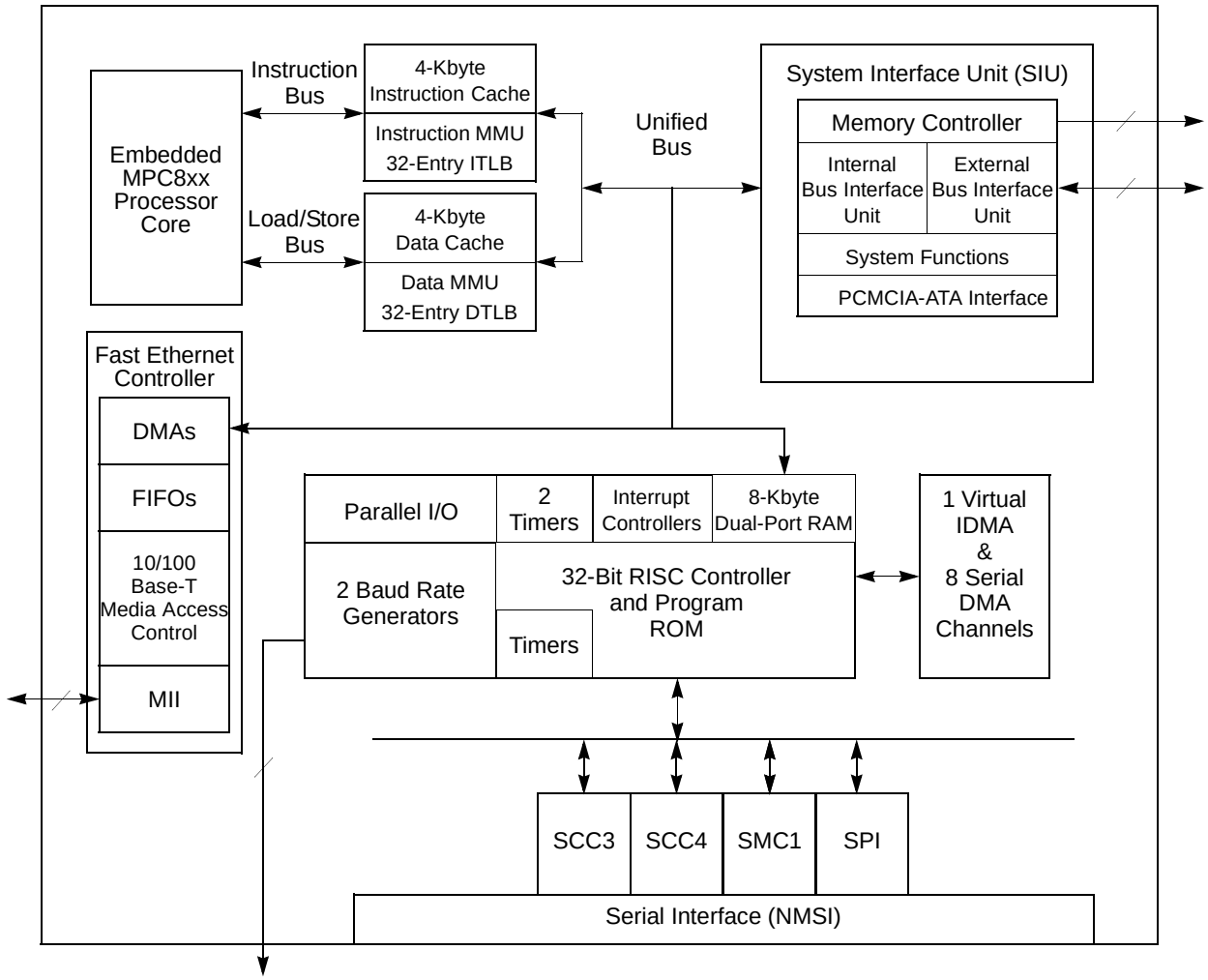

Figure 1. MPC852T Block Diagram

3 Maximum Tolerated Ratings

This section provides the maximum tolerated voltage and temperature ranges for the MPC852T. Table 1 provides the maximum ratings and operating temperatures.

Table 1. Maximum Tolerated Ratings

Rating	Symbol	Value	Unit
Supply voltage [1]	V_{DDL} (core voltage)	– 0.3 to 3.4	V
	V_{DDH} (I/O voltage)	– 0.3 to 4	V
	V_{DDSYN}	– 0.3 to 3.4	V
	Difference between V_{DDL} to V_{DDSYN}	100	mV
Input voltage [2]	V_{in}	GND – 0.3 to V_{DDH}	V
Storage temperature range	T_{stg}	– 55 to +150	°C

1 The power supply of the device must start its ramp from 0.0 V.

2 Functional operating conditions are provided with the DC electrical specifications in Table 5. Absolute maximum ratings are stress ratings only; functional operation at the maxima is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
Caution: All inputs that tolerate 5 V cannot be more than 2.5 V greater than V_{DDH}. This restriction applies to power-up and normal operation (that is, if the MPC852T is unpowered, a voltage greater than 2.5 V must not be applied to its inputs).

Table 2. Operating Temperatures

Rating	Symbol	Value	Unit
Temperature [1] (standard)	$T_{A(min)}$	0	°C
	$T_{j(max)}$	95	°C
Temperature (extended)	$T_{A(min)}$	– 40	°C
	$T_{j(max)}$	100	°C

1 Minimum temperatures are guaranteed as ambient temperature, T_A. Maximum temperatures are guaranteed as junction temperature, T_j.

This device contains circuitry protecting against damage that high-static voltage or electrical fields cause; however, Motorola recommends taking normal precautions to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V_{DD}). -- V_{DDH}.

4 Thermal Characteristics

Table 3 shows the thermal characteristics for the MPC852T.

Table 5. DC Electrical Specifications (continued)

Characteristic	Symbol	Min	Max	Unit
Output high voltage, IOH = -2.0 mA, V_{DDH} = 3.0 V Except XTAL and open drain pins	VOH	2.4	—	V
Output low voltage IOL = 2.0 mA (CLKOUT) IOL = 3.2 mA [3] IOL = 5.3 mA [4] IOL = 7.0 mA (Txd1/pa14, txd2/pa12) IOL = 8.9 mA (TS, TA, TEA, BI, BB, HRESET, SRESET)	VOL	—	0.5	V

1 The PA[0:3], PA[8:11], PB15, PB[24:25]; PB[28:31], PC[4:7], PC[12:13], PC15, PD[3:15], TDI, TDO, TCK, TRST, TMS, MII_TXEN, MII_MDIO are 5 V-tolerant pins.

2 Input capacitance is periodically sampled.

3 A(0:31), TSIZ0/REG, TSIZ1, D(0:31), DP(0:3)/IRQ(3:6), RD/WR, BURST, RSV/IRQ2, IWP(0:1)/VFLS(0:1), RXD3/PA11, TXD3/PA10, RXD4/PA9, TXD4/PA8, TIN3/BRGO3/CLK5/PA3, BRGCLK2/TOUT3/CLK6/PA2, TIN4/BRGO4/CLK7/PA1, TOUT4/CLK8/PA0, SPISEL/PB31, SPICLK/PB30, SPIMOSI/PB29, BRGO4/SPIMISO/PB28, SMTXD1/PB25, SMRXD1/PB24, BRGO3/PB15, RTS1/DREQ0/PC15, RTS3/PC13, RTS4/PC12, CTS3/PC7, CD3/PC6, CTS4/SDACK1/PC5, CD4/PC4, MII-RXD3/PD15, MII-RXD2/PD14, MII-RXD1/PD13, MII-MDC/PD12, MII-TXERR/RXD3/PD11, MII-RX0/TXD3/PD10, MII-TXD0/RXD4/PD9, MII-RXCLK/TXD4/PD8, MII-TXD3/PD5, MII-RXDV/RTS4/PD6, MII-RXERR/RTS3/PD7, MII-TXD2/REJECT3/PD4, MII-TXD1/REJECT4/PD3, MII_CRS, MII_MDIO, MII_TXEN, MII_COL

4 BDIP/GPL_B(5), BR, BG, FRZ/IRQ6, CS(0:5), CS(6), CS(7), WE0/BS_B0/IORD, WE1/BS_B1/IOWR, WE2/BS_B2/PCOE, WE3/ BS_B3/PCWE, BS_A(0:3), GPL_A0/GPL_B0, OE/GPL_A1/GPL_B1, GPL_A(2:3)/GPL_B(2:3)/CS(2:3), UPWAITA/GPL_A4, GPL_A5, ALE_A, CE1_A, CE2_A, DSCK, OP(0:1), OP2/MODCK1/STS, OP3/MODCK2/DSDO, BADDR(28:30)

7 Thermal Calculation and Measurement

For the following discussions, $P_D = (V_{DDL} \times IDDL) + P_{I/O}$, where $P_{I/O}$ is the power dissipation of the I/O drivers.

NOTE

The V_{DDSYN} power dissipation is negligible.

7.1 Estimation with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J, in °C can be obtained from the equation:

$T_J = T_A + (R_{\theta JA} \times P_D)$

where:

T_A = ambient temperature ºC

$R_{\theta JA}$ = package junction-to-ambient thermal resistance (ºC/W)

P_D = power dissipation in package

7.5 Experimental Determination

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$T_J = T_T + (\Psi_{JT} \times P_D)$

where:

Ψ_{JT} = thermal characterization parameter

T_T = thermocouple temperature on top of package

P_D = power dissipation in package

The thermal characterization parameter is measured per JESD51-2 specification published by JEDEC using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors that cooling effects of the thermocouple wire cause.

8 References

Semiconductor Equipment and Materials International(415) 964-5111
805 East Middlefield Rd
Mountain View, CA 94043

MIL-SPEC and EIA/JESD (JEDEC) specifications800-854-7179 or
(Available from Global Engineering documents)303-397-7956

JEDEC Specifications http://www.jedec.org

1. C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47-54.

2. B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212-220.

9 Power Supply and Power Sequencing

This section provides design considerations for the MPC852T power supply. The MPC852T has a core voltage (V_{DDL}) and PLL voltage (V_{DDSYN}) that operates at a lower voltage than the I/O voltage V_{DDH}. The I/O section of the MPC852T is supplied with 3.3 V across V_{DDH} and V_{SS} (GND).

The signal PA[0:3], PA[8:11], PB15, PB[24:25]; PB[28:31], PC[4:7], PC[12:13], PC15] PD[3:15], TDI, TDO, TCK, TRST, TMS, MII_TXEN, MII_MDIO are 5 V-tolerant. All inputs cannot be more than 2.5 V greater than V_{DDH}. In addition, 5 V-tolerant pins can not exceed 5.5 V, and remaining input pins cannot exceed 3.465 V. This restriction applies to power-on reset or power down and normal operation.

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B30c	$\overline{WE}$(0:3)/BS_B[0:3] negated to A(0:31), BADDR(28:30) invalid GPCM write access, TRLX = 0, CSNT = 1. $\overline{CS}$ negated to A(0:31) invalid GPCM write access, TRLX = 0, CSNT = 1 ACS = 10, ACS == 11, EBDF = 1 (MIN = 0.375 x B1 - 3.00)	8.40	—	6.40	—	4.50	—	2.70	—	ns
B30d	$\overline{WE}$(0:3)/BS_B[0:3] negated to A(0:31), BADDR(28:30) invalid GPCM write access TRLX = 1, CSNT =1, $\overline{CS}$ negated to A(0:31) invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10 or 11, EBDF = 1	38.67	—	31.38	—	24.50	—	17.83	—	ns
B31	CLKOUT falling edge to $\overline{CS}$ valid - as requested by control bit CST4 in the corresponding word in the UPM (MAX = 0.00 X B1 + 6.00)	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B31a	CLKOUT falling edge to $\overline{CS}$ valid - as requested by control bit CST1 in the corresponding word in the UPM (MAX = 0.25 x B1 + 6.80)	7.60	14.30	6.30	13.00	5.00	11.80	3.80	10.50	ns
B31b	CLKOUT rising edge to $\overline{CS}$ valid - as requested by control bit CST2 in the corresponding word in the UPM (MAX = 0.00 x B1 + 8.00)	1.50	8.00	1.50	8.00	1.50	8.00	1.50	8.00	ns
B31c	CLKOUT rising edge to $\overline{CS}$ valid- as requested by control bit CST3 in the corresponding word in the UPM (MAX = 0.25 x B1 + 6.30)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
B31d	CLKOUT falling edge to $\overline{CS}$ valid, as requested by control bit CST1 in the corresponding word in the UPM EBDF = 1 (MAX = 0.375 x B1 + 6.6)	13.30	18.00	11.30	16.00	9.40	14.10	7.60	12.30	ns
B32	CLKOUT falling edge to $\overline{BS}$ valid- as requested by control bit BST4 in the corresponding word in the UPM (MAX = 0.00 x B1 + 6.00)	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B32a	CLKOUT falling edge to $\overline{BS}$ valid - as requested by control bit BST1 in the corresponding word in the UPM, EBDF = 0 (MAX = 0.25 x B1 + 6.80)	7.60	14.30	6.30	13.00	5.00	11.80	3.80	10.50	ns
B32b	CLKOUT rising edge to $\overline{BS}$ valid - as requested by control bit BST2 in the corresponding word in the UPM (MAX = 0.00 x B1 + 8.00)	1.50	8.00	1.50	8.00	1.50	8.00	1.50	8.00	ns
B32c	CLKOUT rising edge to $\overline{BS}$ valid - as requested by control bit BST3 in the corresponding word in the UPM (MAX = 0.25 x B1 + 6.80)	7.60	14.30	6.30	13.00	5.00	11.80	3.80	10.50	ns

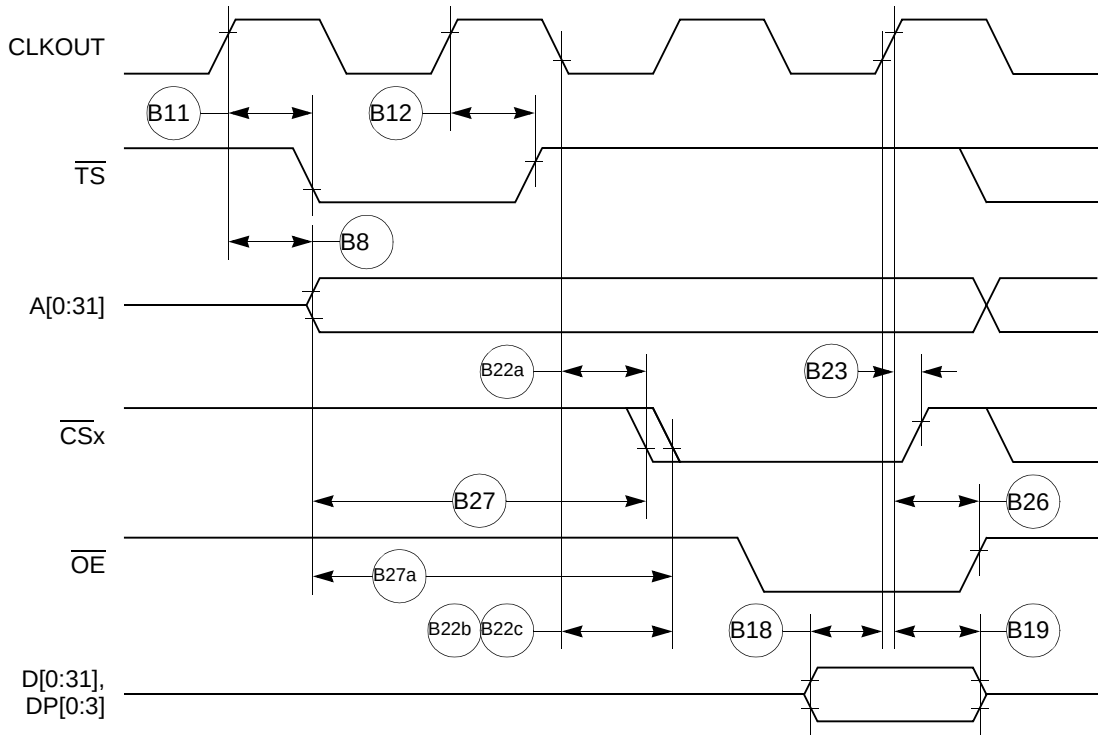

Figure 13. External Bus Read Timing (GPCM Controlled—TRLX = 0 or 1, ACS = 10, ACS = 11)

Figure 14 through Figure 16 provide the timing for the external bus write that various GPCM factors control.

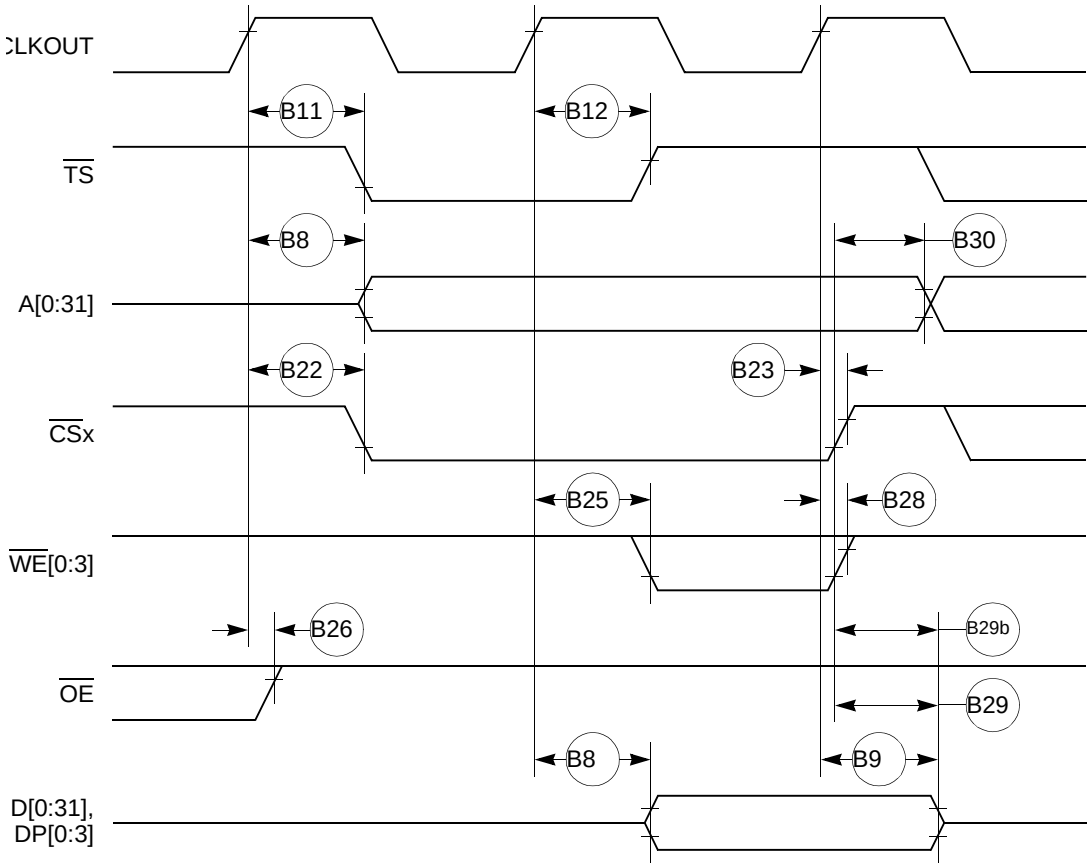

Figure 14. External Bus Write Timing (GPCM Controlled—TRLX = 0 or 1, CSNT = 0)

Figure 26 provides the PCMCIA access cycle timing for the external bus write.

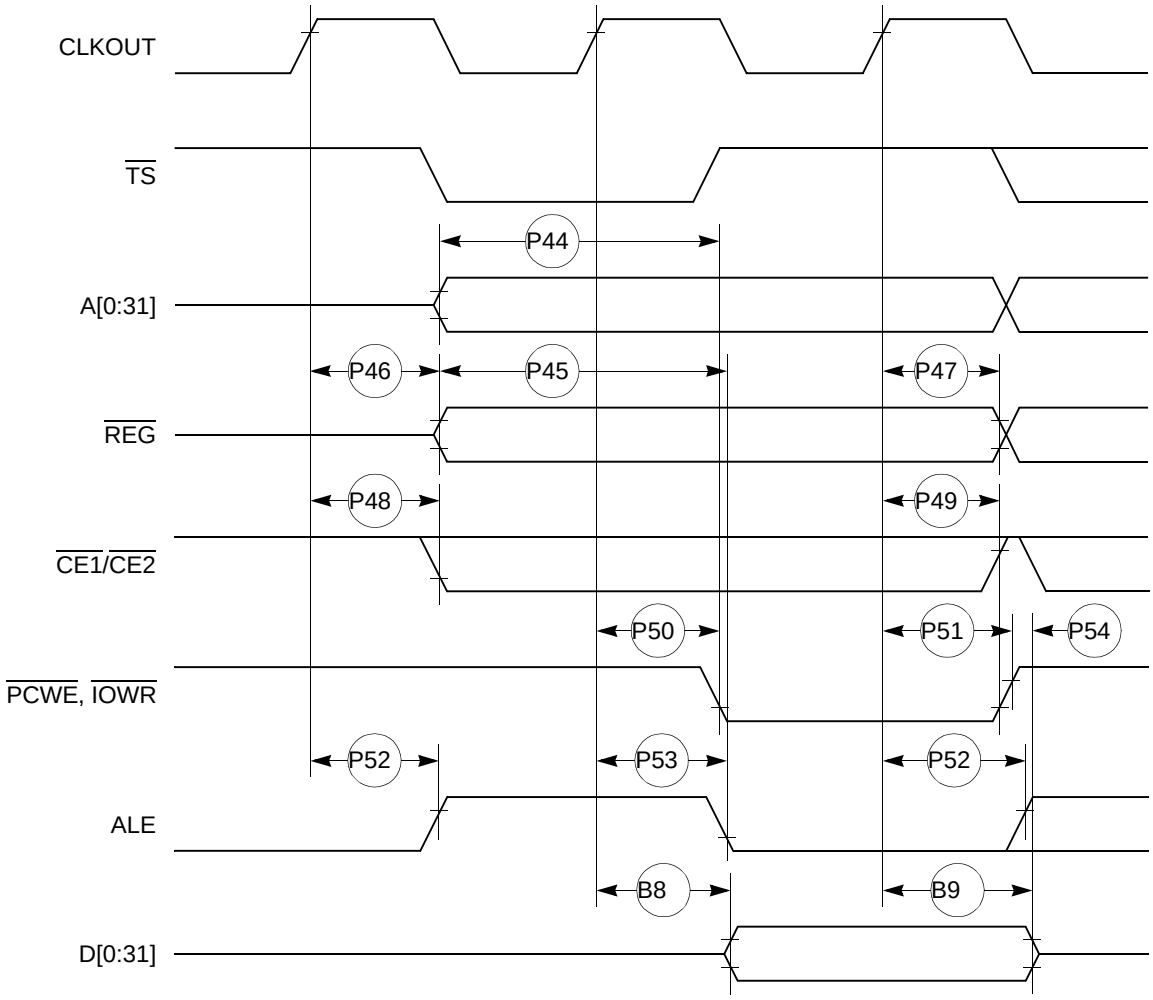

Figure 26. PCMCIA Access Cycles Timing External Bus Write

Figure 27 provides the PCMCIA WAIT signals detection timing.

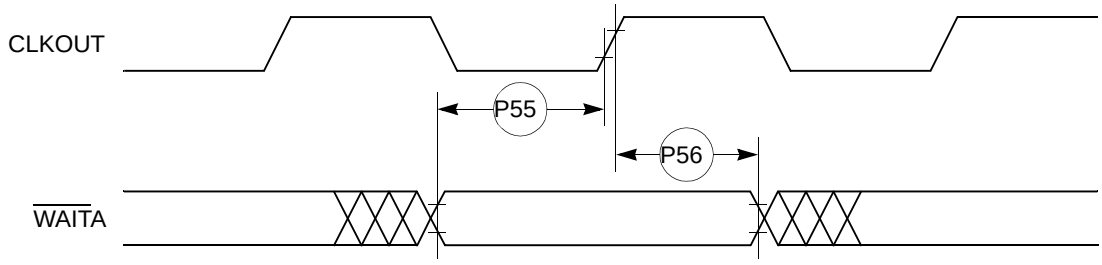

Figure 27. PCMCIA WAIT Signals Detection Timing

Table 13 shows the debug port timing for the MPC852T.

Table 13. Debug Port Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
J82	DSCK cycle time	$3xT_{CLOCKOUT}$	—	—
J83	DSCK clock pulse width	$1.25xT_{CLOCKOUT}$	—	—
J84	DSCK rise and fall times	0.00	3.00	ns
J85	DSDI input data setup time	8.00	—	ns
J86	DSDI data hold time	5.00	—	ns
J87	DSCK low to DSDO data valid	0.00	15.00	ns
J88	DSCK low to DSDO invalid	0.00	2.00	ns

Figure 30 provides the input timing for the debug port clock.

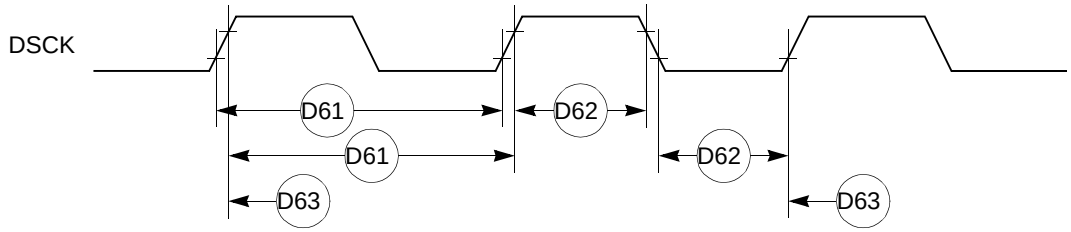

Figure 30. Debug Port Clock Input Timing

Figure 31 provides the timing for the debug port.

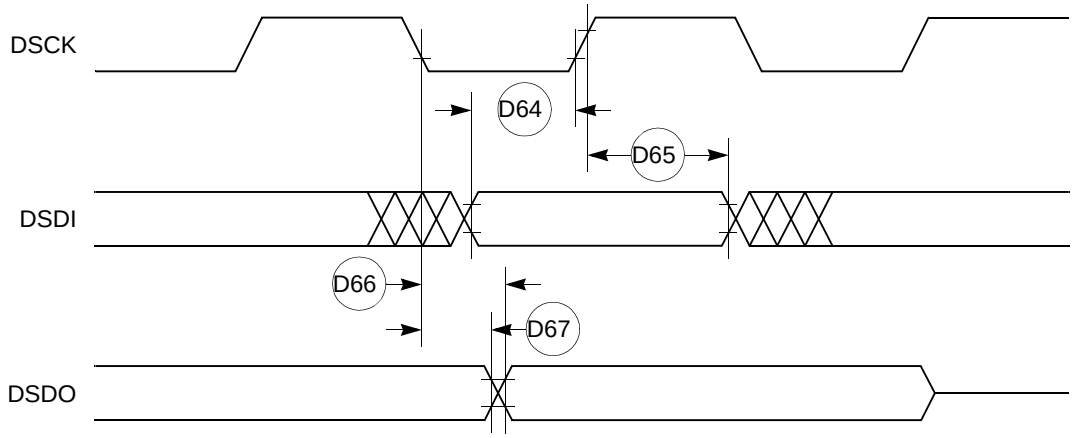

Figure 31. Debug Port Timings

Figure 34 provides the reset timing for the debug port configuration.

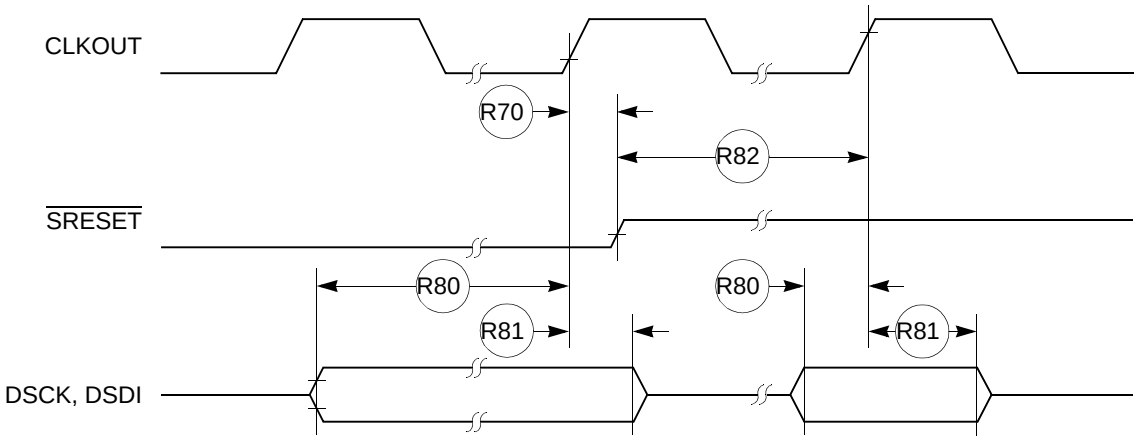

Figure 34. Reset Timing—Debug Port Configuration

13 IEEE 1149.1 Electrical Specifications

Table 15 provides the JTAG timings for the MPC852T shown in Figure 35 through Figure 38.

Table 15. JTAG Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
J82	TCK cycle time	100.00	—	ns
J83	TCK clock pulse width measured at 1.5 V	40.00	—	ns
J84	TCK rise and fall times	0.00	10.00	ns
J85	TMS, TDI data setup time	5.00	—	ns
J86	TMS, TDI data hold time	25.00	—	ns
J87	TCK low to TDO data valid	—	27.00	ns
J88	TCK low to TDO data invalid	0.00	—	ns
J89	TCK low to TDO high impedance	—	20.00	ns
J90	$\overline{\text{TRST}}$ assert time	100.00	—	ns
J91	$\overline{\text{TRST}}$ setup time to TCK low	40.00	—	ns
J92	TCK falling edge to output valid	—	50.00	ns
J93	TCK falling edge to output valid out of high impedance	—	50.00	ns
J94	TCK falling edge to output high impedance	—	50.00	ns
J95	Boundary scan input valid to TCK rising edge	50.00	—	ns
J96	TCK rising edge to boundary scan input invalid	50.00	—	ns

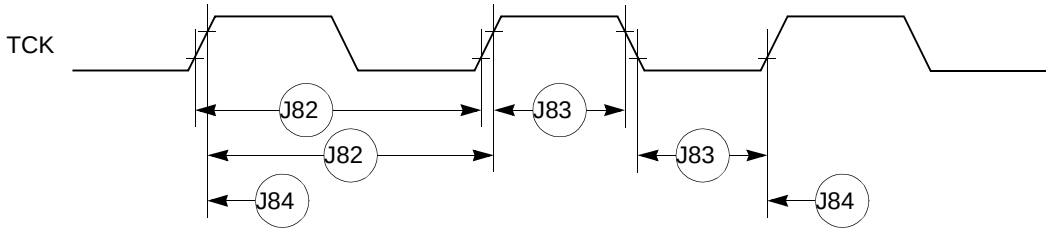

Figure 35. JTAG Test Clock Input Timing

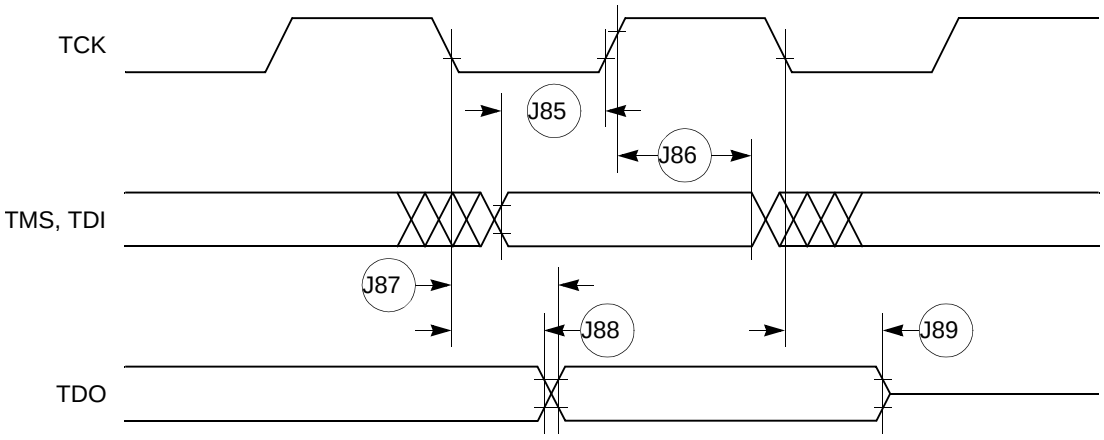

Figure 36. JTAG Test Access Port Timing Diagram

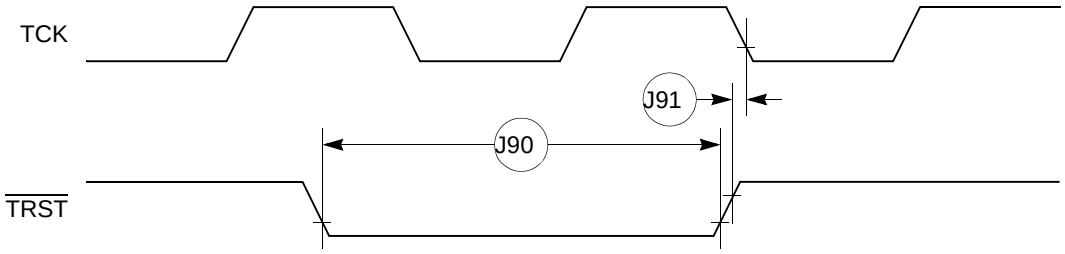

Figure 37. JTAG $\overline{\text{TRST}}$ Timing Diagram

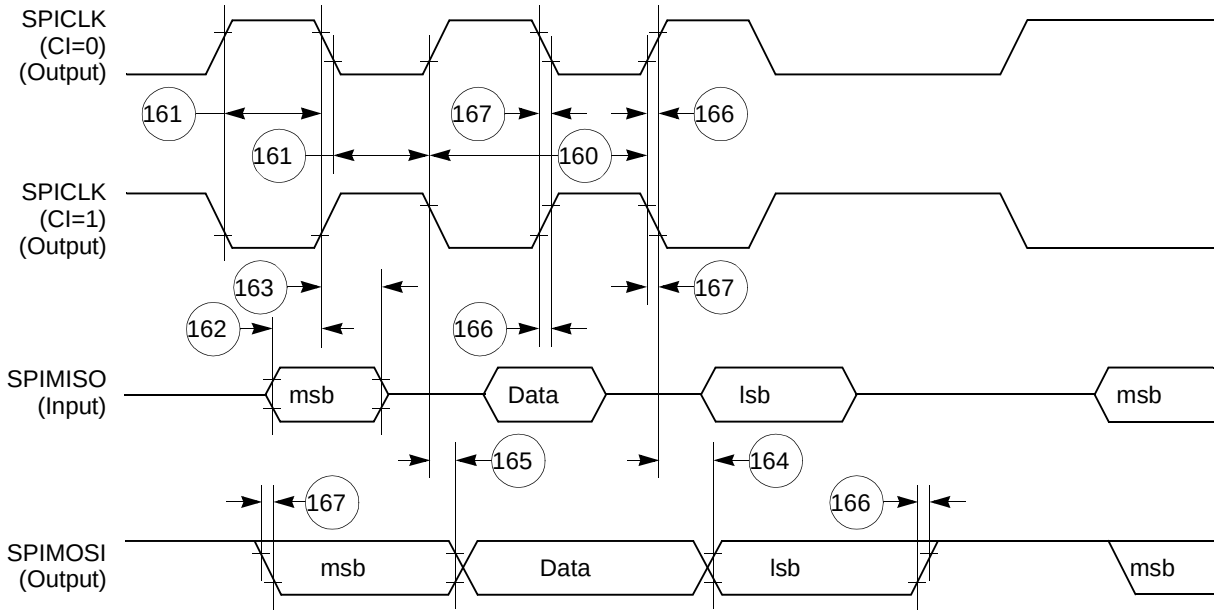

Figure 55. SPI Master (CP = 1) Timing Diagram

14.8 SPI Slave AC Electrical Specifications

Table 24 provides the SPI slave timings as shown in Figure 56 and Figure 57.

Table 24. SPI Slave Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
170	Slave cycle time	2	—	t_{cyc}
171	Slave enable lead time	15	—	ns
172	Slave enable lag time	15	—	ns
173	Slave clock (SPICLK) high or low time	1	—	t_{cyc}
174	Slave sequential transfer delay (does not require deselect)	1	—	t_{cyc}
175	Slave data setup time (inputs)	20	—	ns
176	Slave data hold time (inputs)	20	—	ns
177	Slave access time	—	50	ns

Figure 58 shows MII receive signal timing.

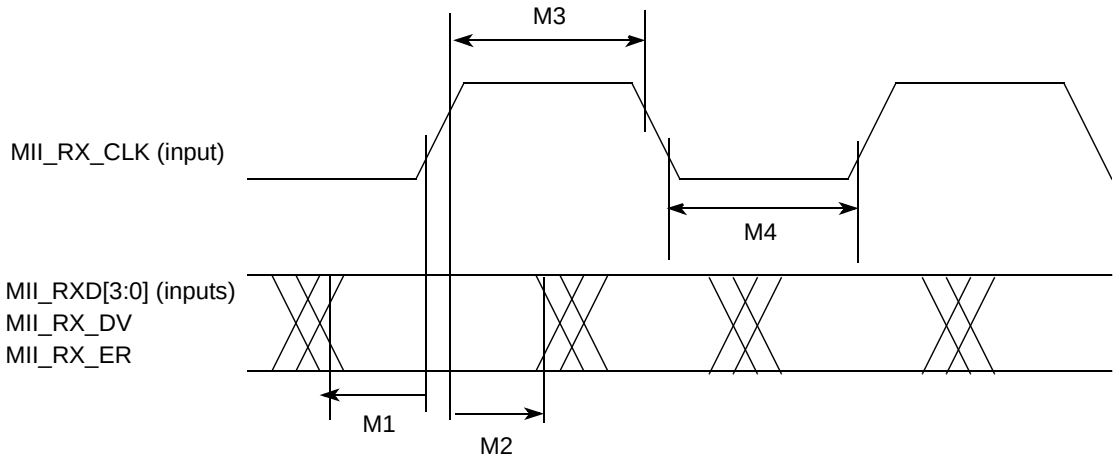

Figure 58. MII Receive Signal Timing Diagram

15.2 MII Transmit Signal Timing (MII_TXD[3:0], MII_TX_EN, MII_TX_ER, MII_TX_CLK)

The transmitter functions correctly up to a MII_TX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII_TX_CLK frequency - 1%.

Table 26 provides information about the MII transmit signal timing,.

Table 26. MII Transmit Signal Timing

Num	Characteristic	Min	Max	Unit
M5	MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER invalid	5	—	ns
M6	MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER valid	—	25	—
M7	MII_TX_CLK pulse width high	35%	65%	MII_TX_CLK period
M8	MII_TX_CLK pulse width low	35%	65%	MII_TX_CLK period

Figure 59 shows the MII transmit signal timing diagram.

16 Mechanical Data and Ordering Information

Table 29 identifies the packages and operating frequencies orderable for the MPC852T.

Table 29. MPC852T Package/Frequency Orderable

Package Type	Temperature (Tj)	Frequency (MHz)	Order Number
Plastic ball grid array (VR and ZT suffix)	0°C to 95°C	50	MPC852TVR50 MPC852TZT50
		66	MPC852TVR66 MPC852TZT66
		80	MPC852TVR80 MPC852TZT80
		100	MPC852TVR100 MPC852TZT100
Plastic ball grid array (CVR suffix)	– 40°C to 100°C	66	TBD

16.1 Pin Assignments

The following sections give the pinout and pin listing for the JEDEC Compliant and the non-JEDEC versions of the 16 x 16 PBGA package.

Table 30 contains a list of the MPC852T input and output signals and shows multiplexing and pin assignments.

Table 30. Pin Assignments - JEDEC Standard

Name	Pin Number	Type
A[0:31]	B15, A15, A14, C14, D13, E11, B14, A13, C13, B13, D12, E10, C12, B12, A12, D11, E9, C11, A9, A11, D10, C10, B8, A10, D9, C9, C8, B11, A8, B10, B9, D8	Bidirectional Three-state (3.3V only)
TSIZ0 $\overline{\text{REG}}$	E8	Bidirectional Three-state (3.3V only)
TSIZ1	E7	Bidirectional Three-state (3.3V only)
RD/$\overline{\text{WR}}$	B1	Bidirectional Three-state (3.3V only)
$\overline{\text{BURST}}$	G3	Bidirectional Three-state (3.3V only)
$\overline{\text{BDIP}}$ $\overline{\text{GPL\_B5}}$	D1	Output
$\overline{\text{TS}}$	E2	Bidirectional Active Pull-up (3.3V only)
$\overline{\text{TA}}$	F4	Bidirectional Active Pull-up (3.3V only)
$\overline{\text{TEA}}$	E3	Open-drain
$\overline{\text{BI}}$	D2	Bidirectional Active Pull-up (3.3V only)
$\overline{\text{IRQ2}}$ $\overline{\text{RSV}}$	G2	Bidirectional Three-state (3.3V only)
$\overline{\text{IRQ4}}$ $\overline{\text{KR}}$ $\overline{\text{RETRY}}$ SPKROUT	J1	Bidirectional Three-state (3.3V only)
$\overline{\text{CR}}$ $\overline{\text{IRQ3}}$	F1	Input (3.3V only)
D[0:31]	R13, T11, R10, T10, T12, R9, R7, T6, T13, M10, N10, P10, P12, R12, M9, N9, P9, N11, T9, R8, P8, N8, T7, P11, P7, N7, M8, R11, R6, P6, T5, R5	Bidirectional Three-state (3.3V only)
DP0 $\overline{\text{IRQ3}}$	P4	Bidirectional Three-state (3.3V only)
DP1 $\overline{\text{IRQ4}}$	P5	Bidirectional Three-state (3.3V only)
DP2 $\overline{\text{IRQ5}}$	T4	Bidirectional Three-state (3.3V only)
DP3 $\overline{\text{IRQ6}}$	R4	Bidirectional Three-state (3.3V only)
$\overline{\text{BR}}$	E1	Bidirectional (3.3V only)

Table 30. Pin Assignments - JEDEC Standard (continued)

Name	Pin Number	Type
PA10 TXD3	H15	Bidirectional (5V tolerant)
PA9 RXD4	J16	Bidirectional (Optional: Open-drain) (5V tolerant)
PA8 TXD4	J15	Bidirectional (5V tolerant)
PA3 CLK5 BRGO3 TIN3	K16	Bidirectional (5V tolerant)
PA2 CLK6 $\overline{\text{TOUT3}}$	K14	Bidirectional (5V tolerant)
PA1 CLK7 BRGO4 TIN4	L15	Bidirectional (5V tolerant)
PA0 CLK8 $\overline{\text{TOUT4}}$	M16	Bidirectional (5V tolerant)
PB31 $\overline{\text{SPISEL}}$	E13	Bidirectional (Optional: Open-drain) (5V tolerant)
PB30 SPICLK	F13	Bidirectional (Optional: Open-drain) (5V tolerant)
PB29 SPIMOSI	D15	Bidirectional (Optional: Open-drain) (5V tolerant)
PB28 SPIMISO BRGO4	G13	Bidirectional (Optional: Open-drain) (5V tolerant)
PB25 SMTXD1	H14	Bidirectional (Optional: Open-drain) (5V tolerant)
PB24 SMRXD1	H16	Bidirectional (Optional: Open-drain) (5V tolerant)
PB15 BRGO3	L16	Bidirectional (5V tolerant)

Table 31. Pin Assignments - non-JEDEC (continued)

Name	Pin Number	Type
$\overline{BR}$	F2	Bidirectional (3.3 V only)
$\overline{BG}$	H5	Bidirectional (3.3 V only)
$\overline{BB}$	G4	Bidirectional Active Pull-up (3.3 V only)
FRZ $\overline{IRQ6}$	J5	Bidirectional (3.3 V only)
$\overline{IRQ0}$	R14	Input (3.3 V only)
$\overline{IRQ1}$	N12	Input (3.3 V only)
$\overline{IRQ7}$ M_TX_CLK	P13	Input (3.3 V only)
$\overline{CS}$[0:5]	C3, B3, E4, D4, F7, D5	Output
$\overline{CS6}$	E5	Output
$\overline{CS7}$	B4	Output
$\overline{WE0}$ BS_B0 $\overline{IORD}$	E7	Output
$\overline{WE1}$ BS_B1 $\overline{IOWR}$	D7	Output
$\overline{WE2}$ BS_B2 $\overline{PCOE}$	B6	Output
$\overline{WE3}$ BS_B3 $\overline{PCWE}$	C6	Output
$\overline{BS\_A}$[0:3]	B7, E8, D8, C8	Output
$\overline{GPL\_A0}$ $\overline{GPL\_B0}$	D6	Output
$\overline{OE}$ $\overline{GPL\_A1}$ $\overline{GPL\_B1}$	E6	Output
$\overline{GPL\_A}$[2:3] $\overline{GPL\_B}$[2:3] $\overline{CS}$[2–3]	B5, C5	Output
UPWAITA $\overline{GPL\_A4}$	D3	Bidirectional (3.3 V only)
$\overline{GPL\_A5}$	F5	Output
$\overline{PORESET}$	R2	Input (3.3 V only)

Table 31. Pin Assignments - non-JEDEC (continued)

Name	Pin Number	Type
PB25 SMTXD1	J15	Bidirectional (Optional: Open-drain) (5 V-tolerant)
PB24 SMRXD1	J17	Bidirectional (Optional: Open-drain) (5 V-tolerant)
PB15 BRGO3	M17	Bidirectional (5 V-tolerant)
PC15 $\overline{\text{DREQ0}}$	D17	Bidirectional (5 V-tolerant)
PC13 $\overline{\text{RTS3}}$	F15	Bidirectional (5 V-tolerant)
PC12 $\overline{\text{RTS4}}$	F16	Bidirectional (5 V-tolerant)
PC7 $\overline{\text{CTS3}}$	K15	Bidirectional (5 V-tolerant)
PC6 $\overline{\text{CD3}}$	L16	Bidirectional (5 V-tolerant)
PC5 $\overline{\text{CTS4}}$ SDACK1	K14	Bidirectional (5 V-tolerant)
PC4 $\overline{\text{CD4}}$	M15	Bidirectional (5 V-tolerant)
PD15 MII_RXD3	N15	Bidirectional (5 V-tolerant)
PD14 MII_RXD2	P17	Bidirectional (5 V-tolerant)
PD13 MII_RXD1	L14	Bidirectional (5 V-tolerant)
PD12 MII_MDC	P16	Bidirectional (5 V-tolerant)
PD11 RXD3 MII_TX_ER	R17	Bidirectional (5 V-tolerant)
PD10 TXD3 MII_RXD0	T16	Bidirectional (5 V-tolerant)

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