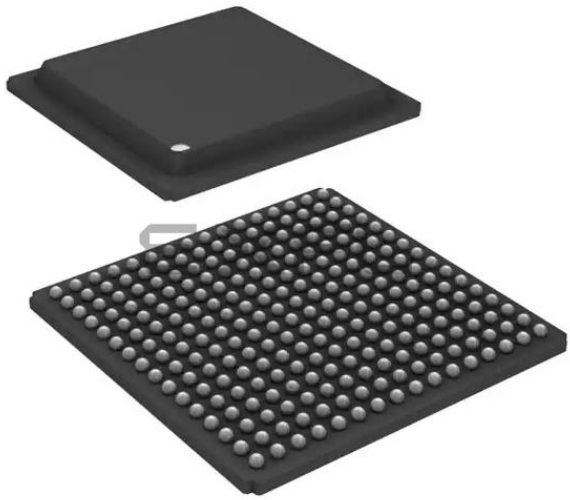

**Welcome to E-XFL.COM**

## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | MPC8xx |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 66MHz |
| Co-Processors/DSP | Communications; CPM |
| RAM Controllers | DRAM |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10Mbps (1) |
| SATA | - |
| USB | - |
| Voltage - I/O | 3.3V |
| Operating Temperature | 0°C ~ 95°C (TA) |
| Security Features | - |
| Package / Case | 256-BBGA |
| Supplier Device Package | 256-PBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc852tvr66 |

- System integration unit (SIU)
  - Bus monitor
  - Software watchdog
  - Periodic interrupt timer (PIT)
  - Clock synthesizer
  - Decrementer and time base
  - Reset controller
  - IEEE 1149.1 test access port (JTAG)
- Interrupts
  - Seven external interrupt request (IRQ) lines
  - Seven port pins with interrupt capability
  - Eighteen internal interrupt sources
  - Programmable priority between SCCs
  - Programmable highest-priority request
- Communications processor module (CPM)
  - RISC controller
  - Communication-specific commands (for example, GRACEFUL STOP TRANSMIT, ENTER HUNT MODE, and RESTART TRANSMIT)
  - Supports continuous mode transmission and reception on all serial channels
  - 8-Kbytes of dual-port RAM
  - 8 serial DMA (SDMA) channels
  - Three parallel I/O registers with open-drain capability
- Two baud rate generators
  - Independent (can be connected toany SCC3/4 or SMC1)
  - Allows changes during operation
  - Autobaud support option
- Two SCCs (serial communication controllers)
  - Ethernet/IEEE 802.3 optional on SCC3 & SCC4, supporting full 10-Mbps operation
  - HDLC/SDLC
  - HDLC bus (implements an HDLC-based local area network (LAN))
  - Universal asynchronous receiver transmitter (UART)
  - Totally transparent (bit streams)
  - Totally transparent (frame-based with optional cyclic redundancy check (CRC))
- One SMC (serial management channels)
  - UART
- One SPI (serial peripheral interface)
  - Supports master and slave modes
  - Supports multimaster operation on the same bus
- PCMCIA interface
  - Master (socket) interface, release 2.1 compliant

  - Supports one independent PCMCIA socket; 8-memory or I/O windows supported
- Debug interface
  - Eight comparators: four operate on instruction address, two operate on data address, and two operate on data
  - Supports conditions: = ≠ < >
  - Each watchpoint can generate a break point internally.
- Normal high and normal low power modes to conserve power
- 1.8 V Core and 3.3 V I/O operation with 5-V TTL compatibility. Refer to Table 5 for a listing of the 5-V Tolerant pins.

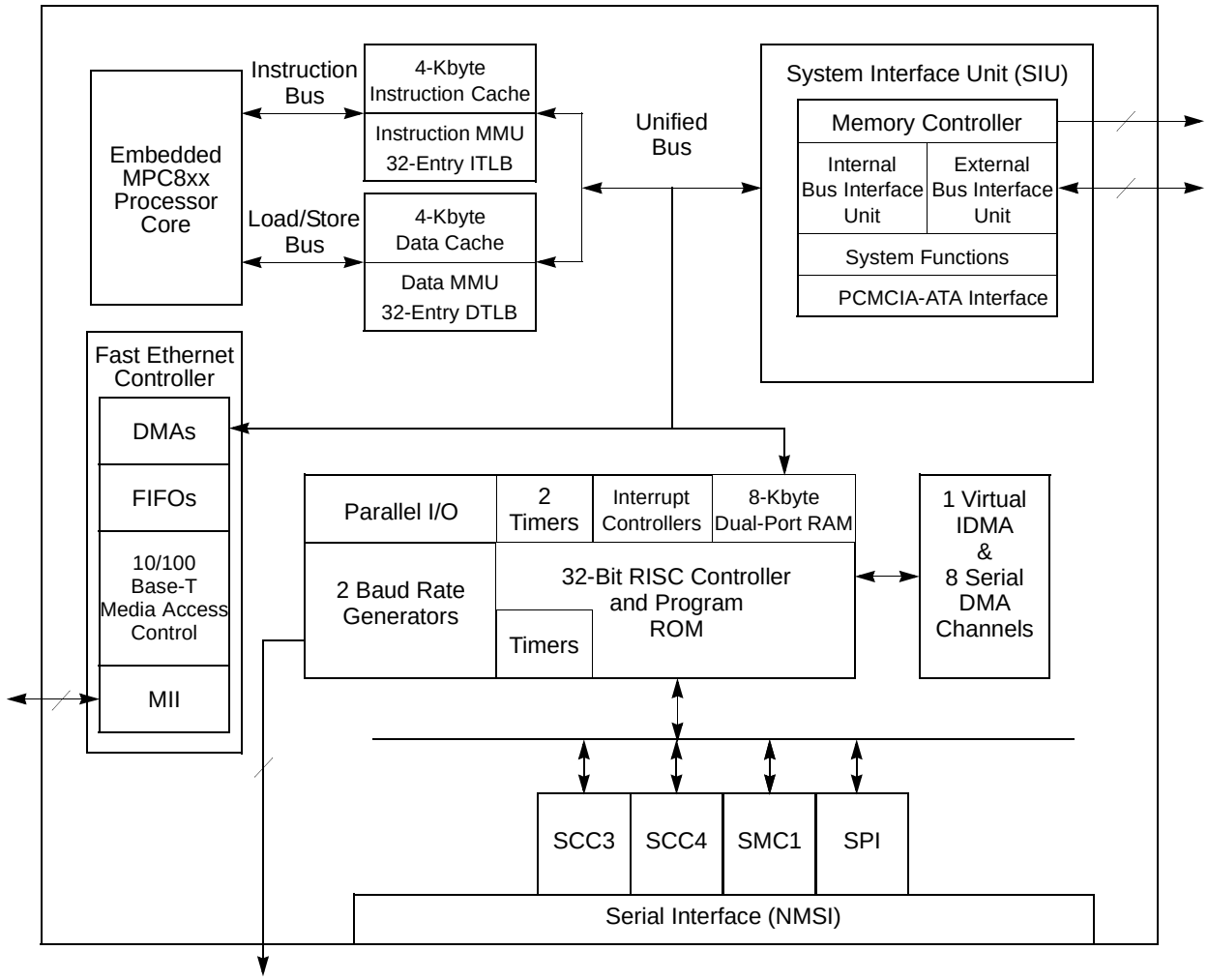


**Figure 1. MPC852T Block Diagram**

**Table 3. MPC852T Thermal Resistance Data**

| Rating | Environment | | Symbol | Value | Unit |
|---|---|---|---|---|---|
| Junction to ambient [1] | Natural convection | Single layer board (1s) | $R_{\theta JA}$ [2] | 49 | °C/W |
| | | Four layer board (2s2p) | $R_{\theta JMA}$ [3] | 32 | |
| | Air flow (200 ft/min) | Single layer board (1s) | $R_{\theta JMA}$ [3] | 41 | |
| | | Four layer board (2s2p) | $R_{\theta JMA}$ [3] | 29 | |
| Junction to board [4] | | | $R_{\theta JB}$ | 24 | |
| Junction to case [5] | | | $R_{\theta JC}$ | 13 | |
| Junction to package top [6] | Natural convection | | $\Psi_{JT}$ | 3 | |
| | Air flow (200 ft/min) | | $\Psi_{JT}$ | 2 | |

1 Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal

3 Per JEDEC JESD51-6 with the board horizontal

4 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature. For exposed pad packages where the pad would be expected to be soldered, junction to case thermal resistance is a simulated value from the junction to the exposed pad without contact resistance.

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2

# 5 Power Dissipation

Table 4 provides power dissipation information. The modes are 1:1, where CPU and bus speeds are equal, and 2:1 mode, where CPU frequency is twice bus speed.

**Table 4. Power Dissipation ($P_D$)**

| Die Revision | Bus Mode | Frequency (MHz) | Typical [1] | Maximum [2] | Unit |
|---|---|---|---|---|---|
| 0 | 1:1 | 50 | 110 | 140 | mW |
| | | 66 | 150 | 180 | mW |
| | 2:1 | 66 | 140 | 160 | mW |
| | | 80 | 170 | 200 | mW |
| | | 100 | 210 | 250 | mW |

1 Typical power dissipation is measured at 1.9 V.

**Table 5. DC Electrical Specifications (continued)**

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Output high voltage, IOH = -2.0 mA, $V_{DDH}$ = 3.0 V<br>Except XTAL and open drain pins | VOH | 2.4 | — | V |
| Output low voltage<br>IOL = 2.0 mA (CLKOUT)<br>IOL = 3.2 mA [3]<br>IOL = 5.3 mA [4]<br>IOL = 7.0 mA (Txd1/pa14, txd2/pa12)<br>IOL = 8.9 mA (TS, TA, TEA, BI, BB, HRESET, SRESET) | VOL | — | 0.5 | V |

1 The PA[0:3], PA[8:11], PB15, PB[24:25]; PB[28:31], PC[4:7], PC[12:13], PC15, PD[3:15], TDI, TDO, TCK, TRST, TMS, MII_TXEN, MII_MDIO are 5 V-tolerant pins.

2 Input capacitance is periodically sampled.

3 A(0:31), TSIZ0/REG, TSIZ1, D(0:31), DP(0:3)/IRQ(3:6), RD/WR, BURST, RSV/IRQ2, IWP(0:1)/VFLS(0:1), RXD3/PA11, TXD3/PA10, RXD4/PA9, TXD4/PA8, TIN3/BRGO3/CLK5/PA3, BRGCLK2/TOUT3/CLK6/PA2, TIN4/BRGO4/CLK7/PA1, TOUT4/CLK8/PA0, SPISEL/PB31, SPICLK/PB30, SPIMOSI/PB29, BRGO4/SPIMISO/PB28, SMTXD1/PB25, SMRXD1/PB24, BRGO3/PB15, RTS1/DREQ0/PC15, RTS3/PC13, RTS4/PC12, CTS3/PC7, CD3/PC6, CTS4/SDACK1/PC5, CD4/PC4, MII-RXD3/PD15, MII-RXD2/PD14, MII-RXD1/PD13, MII-MDC/PD12, MII-TXERR/RXD3/PD11, MII-RX0/TXD3/PD10, MII-TXD0/RXD4/PD9, MII-RXCLK/TXD4/PD8, MII-TXD3/PD5, MII-RXDV/RTS4/PD6, MII-RXERR/RTS3/PD7, MII-TXD2/REJECT3/PD4, MII-TXD1/REJECT4/PD3, MII_CRS, MII_MDIO, MII_TXEN, MII_COL

4 BDIP/GPL_B(5), BR, BG, FRZ/IRQ6, CS(0:5), CS(6), CS(7), WE0/BS_B0/IORD, WE1/BS_B1/IOWR, WE2/BS_B2/PCOE, WE3/ BS_B3/PCWE, BS_A(0:3), GPL_A0/GPL_B0, OE/GPL_A1/GPL_B1, GPL_A(2:3)/GPL_B(2:3)/CS(2:3), UPWAITA/GPL_A4, GPL_A5, ALE_A, CE1_A, CE2_A, DSCK, OP(0:1), OP2/MODCK1/STS, OP3/MODCK2/DSDO, BADDR(28:30)

# 7 Thermal Calculation and Measurement

For the following discussions, $P_D = (V_{DDL} \times IDDL) + P_{I/O}$, where $P_{I/O}$ is the power dissipation of the I/O drivers.

**NOTE**

The $V_{DDSYN}$ power dissipation is negligible.

## 7.1 Estimation with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, $T_J$, in °C can be obtained from the equation:

$T_J = T_A + (R_{\theta JA} \times P_D)$

where:

$T_A$ = ambient temperature ºC

$R_{\theta JA}$ = package junction-to-ambient thermal resistance (ºC/W)

$P_D$ = power dissipation in package

The MBMR[GPLB4DIS], PAPAR, PADIR, PBPAR, PBDIR, PCPAR, and PCDIR should be configured with the mandatory value in Table 6 in the boot code after the reset deasserts.

**Table 6. Mandatory Reset Configuration of MPC852T**

| Register/Configuration | Field | Value (binary) |
|---|---|---|
| HRCW<br>(Hardware reset configuration word) | HRCW[DBGC] | X1 |
| SIUMCR<br>(SIU module configuration register) | SIUMCR[DBGC] | X1 |
| MBMR<br>(Machine B mode register) | MBMR[GPLB4DIS} | 0 |
| PAPAR<br>(Port A pin assignment register) | PAPAR[4-7]<br>PAPAR[12-15] | 0 |
| PADIR<br>(Port A Data Direction Register) | PADIR[4-7]<br>PADIR[12-15] | 1 |
| PBPAR<br>(Port B Pin Assignment Register) | PBPAR[14]<br>PBPAR[16-23]<br>PBPAR[26-27] | 0 |
| PBDIR<br>(Port B Data Direction Register) | PBDIR[14]<br>PBDIR[16-23]<br>PBDIR[26-27] | 1 |
| PCPAR<br>(Port C Pin Assignment Register) | PCPAR[8-11]<br>PCDIR[14] | 0 |
| PCDIR<br>(Port C Data Direction Register) | PCDIR[8-11]<br>PCDIR[14] | 1 |

# 11 Layout Practices

Each $V_{DD}$ pin on the MPC852T should be provided with a low-impedance path to the board's supply. Each GND pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The $V_{DD}$ power supply should be bypassed to ground using at least four 0.1 µF by-pass capacitors located as close as possible to the four sides of the package. Each board designed should be characterized and additional appropriate decoupling capacitors should be used if required. The capacitor leads and associated printed circuit traces connecting to chip $V_{DD}$ and GND should be kept to less than half an inch per capacitor lead. At a minimum, a four-layer board employing two inner layers as $V_{DD}$ and GND planes should be used.

All output pins on the MPC852T have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized to minimize undershoot and reflections that these fast output switching times cause. This recommendation particularly applies to the address and data buses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances that the PC traces cause. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads, because these loads create higher transient currents in the $V_{DD}$ and GND circuits. Pull up all unused inputs or signals that are inputs during reset. Special care should be taken to minimize the noise levels on the PLL

**Table 9. Bus Operation Timings (continued)**

| Num | Characteristic | 33 MHz | | 40 MHz | | 50 MHz | | 66 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| B1d | CLKOUT phase jitter peak-to-peak for OSCLK ≥ 15 MHz | — | 4 | — | 4 | — | 4 | — | 4 | ns |
| | CLKOUT phase jitter peak-to-peak for OSCLK < 15 MHz | — | 5 | — | 5 | — | 5 | — | 5 | ns |
| B2 | CLKOUT pulse width low (MIN = 0.4 x B1, MAX = 0.6 x B1) | 12.1 | 18.2 | 10.0 | 15.0 | 8.0 | 12.0 | 6.1 | 9.1 | ns |
| B3 | CLKOUT pulse width high (MIN = 0.4 x B1, MAX = 0.6 x B1) | 12.1 | 18.2 | 10.0 | 15.0 | 8.0 | 12.0 | 6.1 | 9.1 | ns |
| B4 | CLKOUT rise time | — | 4.00 | — | 4.00 | — | 4.00 | — | 4.00 | ns |
| B5 | CLKOUT fall time | — | 4.00 | — | 4.00 | — | 4.00 | — | 4.00 | ns |
| B7 | CLKOUT to A(0:31), BADDR(28:30), RD/$\overline{WR}$, $\overline{BURST}$, D(0:31), DP(0:3) output hold (MIN = 0.25 x B1) | 7.60 | — | 6.30 | — | 5.00 | — | 3.80 | — | ns |
| B7a | CLKOUT to TSIZ(0:1), $\overline{REG}$, $\overline{RSV}$, $\overline{BDIP}$, PTR output hold (MIN = 0.25 x B1) | 7.60 | — | 6.30 | — | 5.00 | — | 3.80 | — | ns |
| B7b | CLKOUT to $\overline{BR}$, $\overline{BG}$, FRZ, VFLS(0:1), VF(0:2) IWP(0:2), LWP(0:1), $\overline{STS}$ output hold (MIN = 0.25 x B1) | 7.60 | — | 6.30 | — | 5.00 | — | 3.80 | — | ns |
| B8 | CLKOUT to A(0:31), BADDR(28:30) RD/$\overline{WR}$, $\overline{BURST}$, D(0:31), DP(0:3) valid (MAX = 0.25 x B1 + 6.3) | — | 13.80 | — | 12.50 | — | 11.30 | — | 10.00 | ns |
| B8a | CLKOUT to TSIZ(0:1), $\overline{REG}$, $\overline{RSV}$, $\overline{BDIP}$, PTR valid (MAX = 0.25 x B1 + 6.3) | — | 13.80 | — | 12.50 | — | 11.30 | — | 10.00 | ns |
| B8b | CLKOUT to $\overline{BR}$, $\overline{BG}$, VFLS(0:1), VF(0:2), IWP(0:2), FRZ, LWP(0:1), $\overline{STS}$ Valid [3] (MAX = 0.25 x B1 + 6.3) | — | 13.80 | — | 12.50 | — | 11.30 | — | 10.00 | ns |
| B9 | CLKOUT to A(0:31), BADDR(28:30), RD/$\overline{WR}$, $\overline{BURST}$, D(0:31), DP(0:3), TSIZ(0:1), $\overline{REG}$, $\overline{RSV}$, PTR High-Z (MAX = 0.25 x B1 + 6.3) | 7.60 | 13.80 | 6.30 | 12.50 | 5.00 | 11.30 | 3.80 | 10.00 | ns |
| B11 | CLKOUT to $\overline{TS}$, $\overline{BB}$ assertion (MAX = 0.25 x B1 + 6.0) | 7.60 | 13.60 | 6.30 | 12.30 | 5.00 | 11.00 | 3.80 | 9.80 | ns |
| B11a | CLKOUT to $\overline{TA}$, $\overline{BI}$ assertion (when driven by the memory controller or PCMCIA interface) (MAX = 0.00 x B1 + 9.30 [2]) | 2.50 | 9.30 | 2.50 | 9.30 | 2.50 | 9.30 | 2.50 | 9.80 | ns |
| B12 | CLKOUT to $\overline{TS}$, $\overline{BB}$ negation (MAX = 0.25 x B1 + 4.8) | 7.60 | 12.30 | 6.30 | 11.00 | 5.00 | 9.80 | 3.80 | 8.50 | ns |
| B12a | CLKOUT to $\overline{TA}$, $\overline{BI}$ negation (when driven by the memory controller or PCMCIA interface) (MAX = 0.00 x B1 + 9.00) | 2.50 | 9.00 | 2.50 | 9.00 | 2.50 | 9.00 | 2.50 | 9.00 | ns |
| B13 | CLKOUT to $\overline{TS}$, $\overline{BB}$ High-Z (MIN = 0.25 x B1) | 7.60 | 21.60 | 6.30 | 20.30 | 5.00 | 19.00 | 3.80 | 14.00 | ns |

Figure 9 provides the timing for the input data controlled by the UPM for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

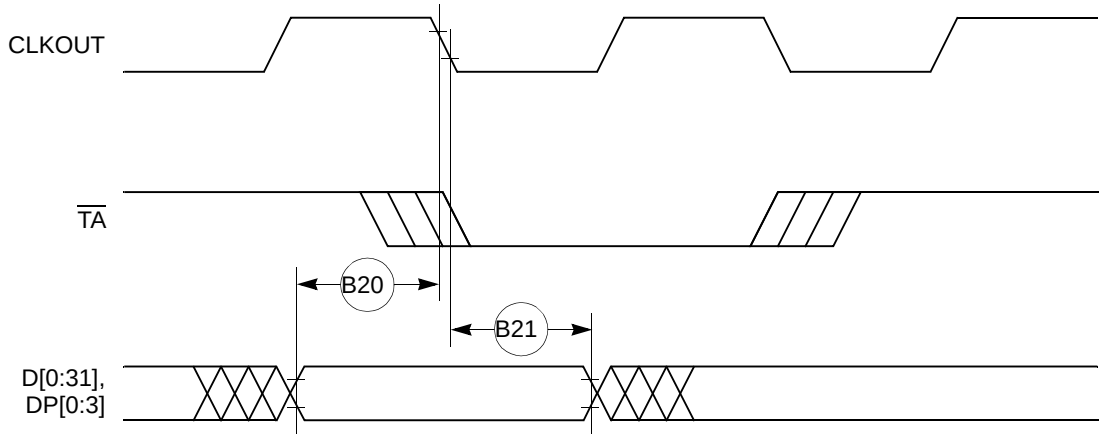


**Figure 9. Input Data Timing When Controlled by UPM in the Memory Controller and DLT3 = 1**

Figure 10 through Figure 13 provide the timing for the external bus read that various GPCM factors control.

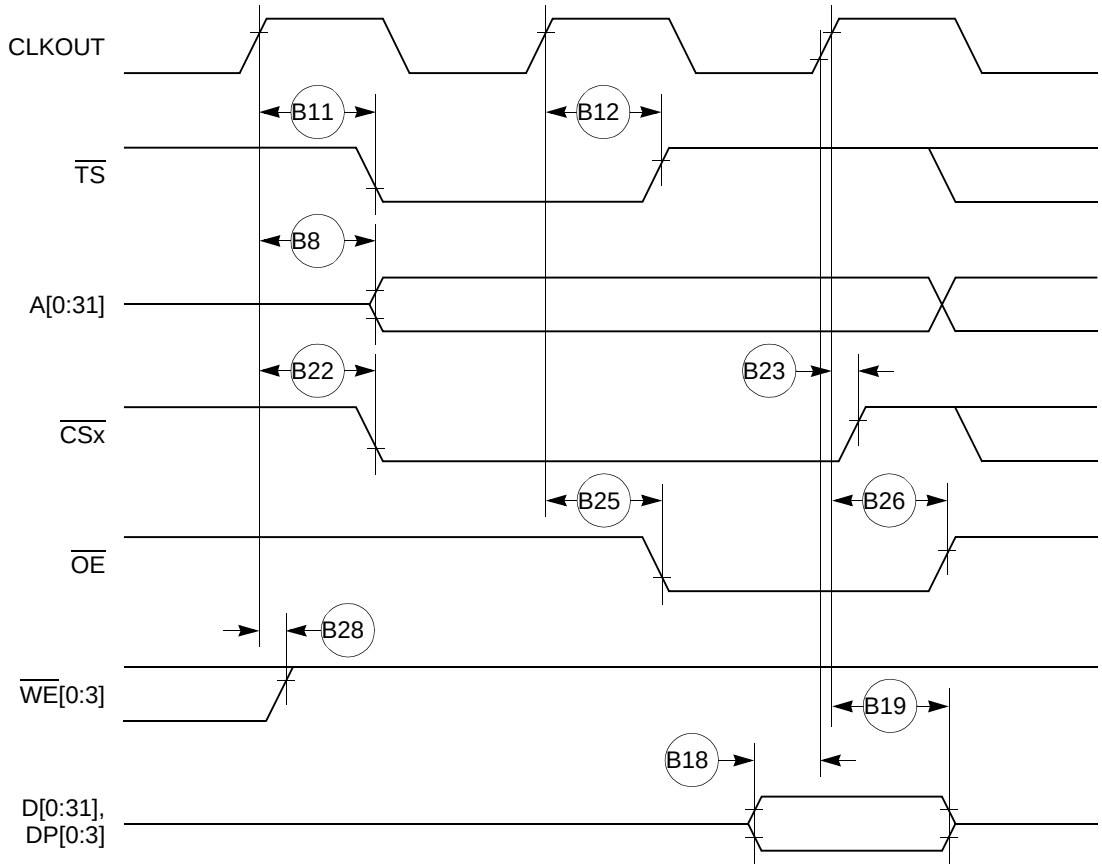


**Figure 10. External Bus Read Timing (GPCM Controlled—ACS = 00)**

Figure 14 through Figure 16 provide the timing for the external bus write that various GPCM factors control.

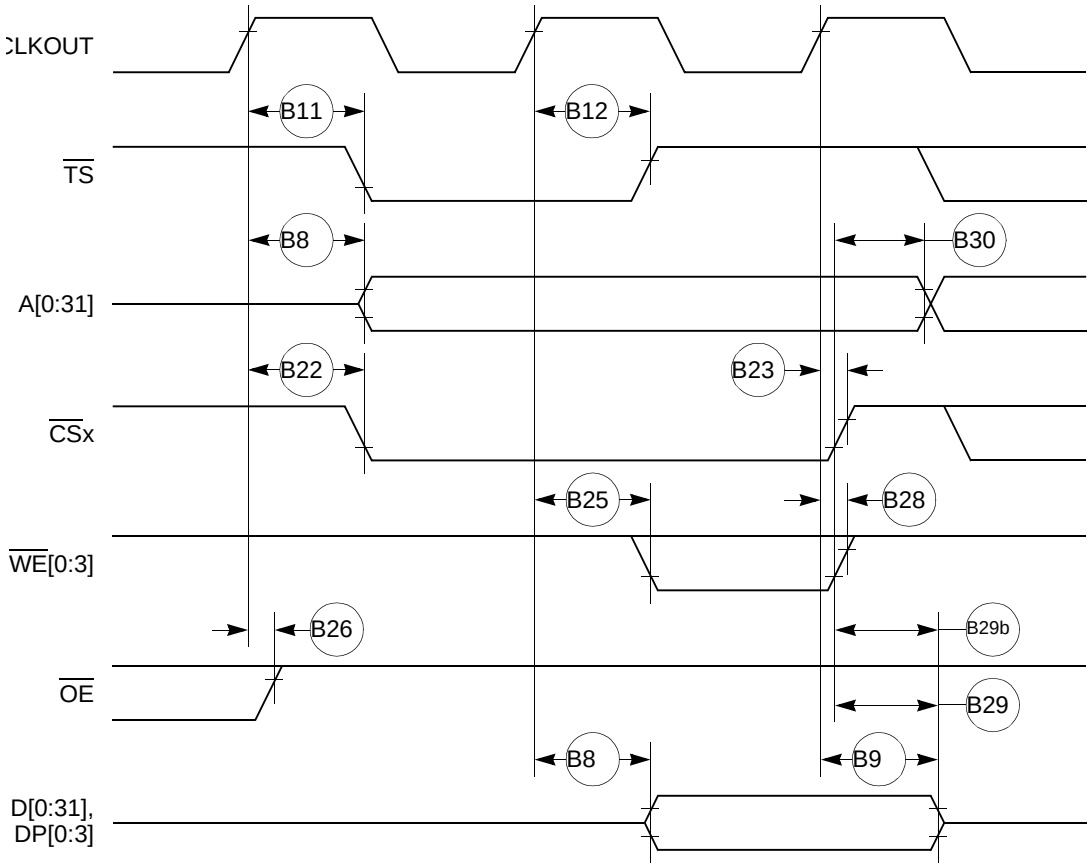


**Figure 14. External Bus Write Timing (GPCM Controlled—TRLX = 0 or 1, CSNT = 0)**

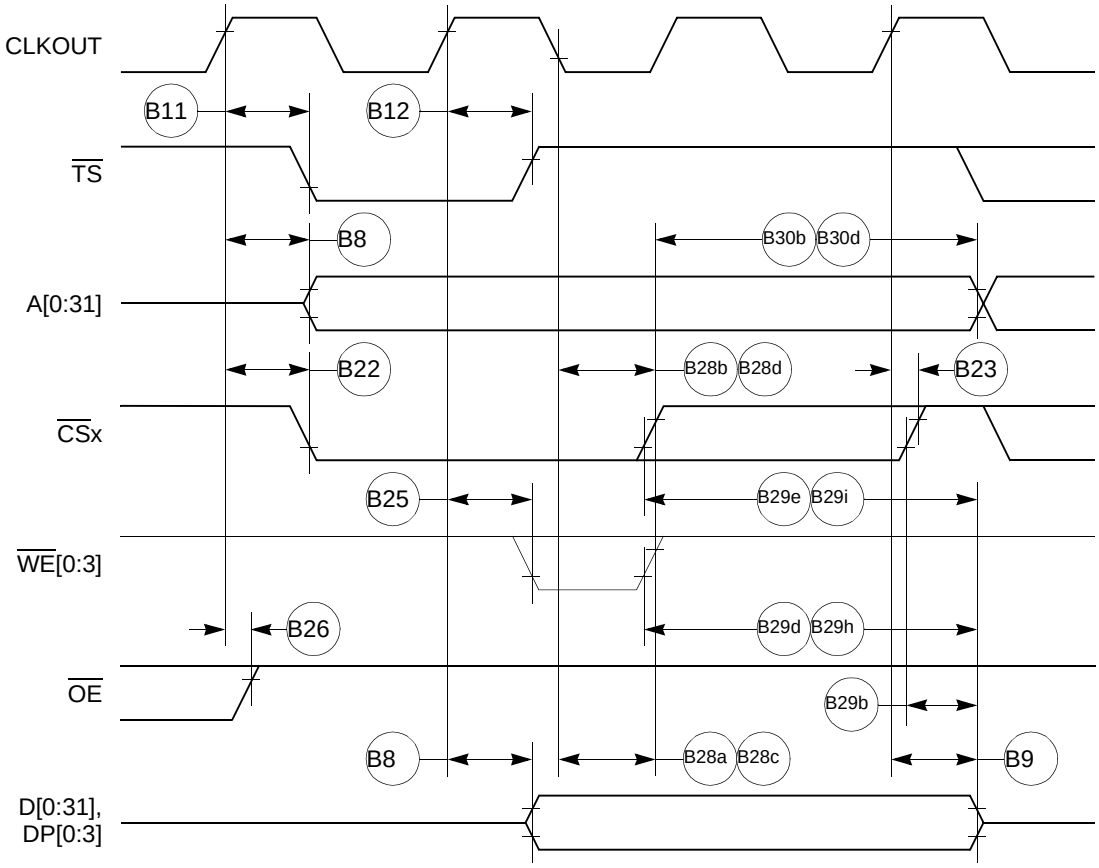


**Figure 16. External Bus Write Timing (GPCM Controlled—TRLX = 0 or 1, CSNT = 1)**

Figure 17 provides the timing for the external bus that the UPM controls.

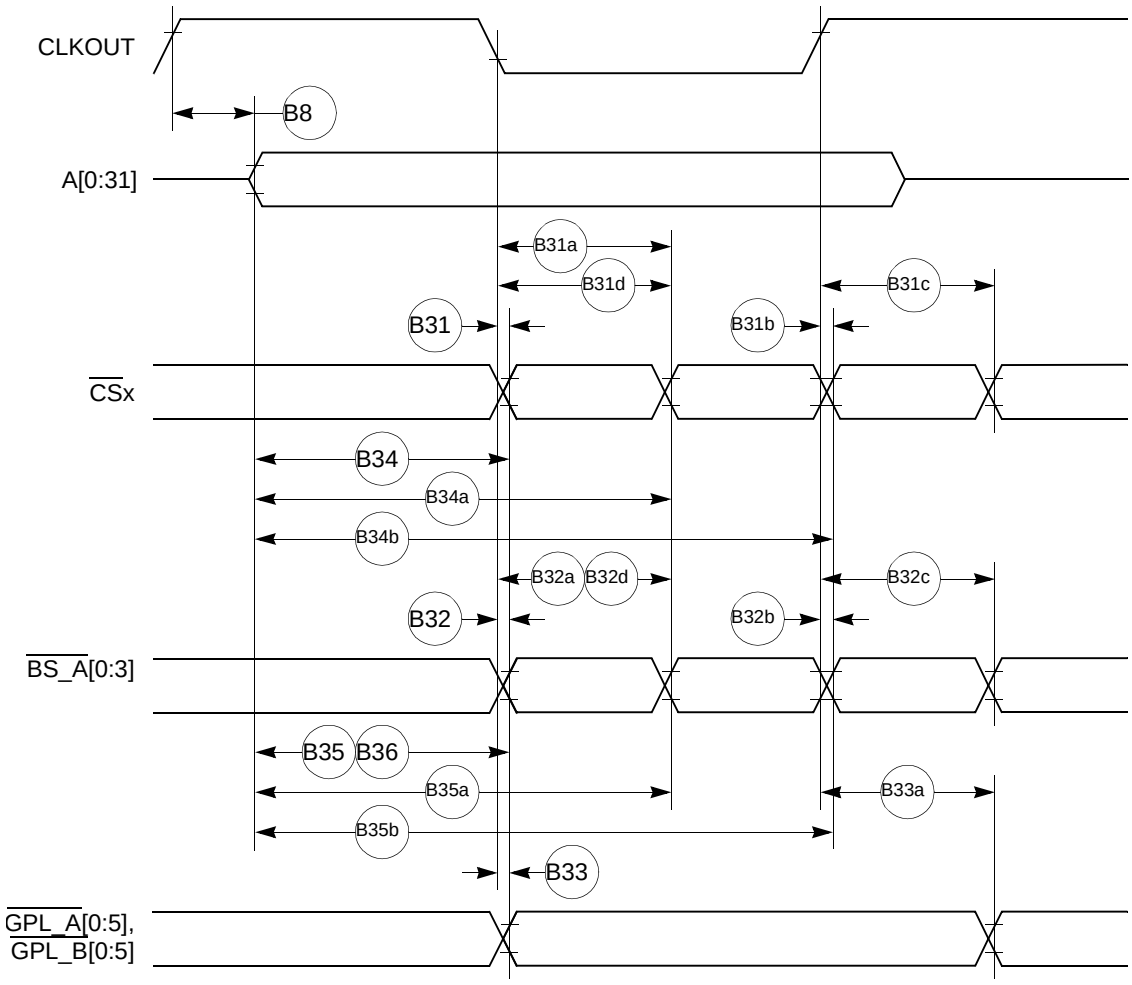


**Figure 17. External Bus Timing (UPM Controlled Signals)**

Figure 20 provides the timing for the synchronous external master access that the GPCM controls.

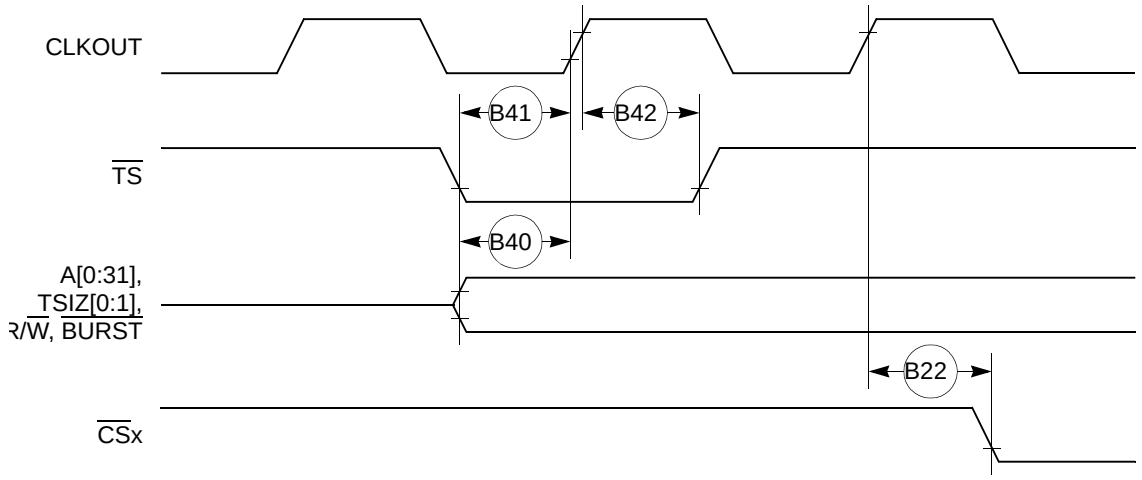


**Figure 20. Synchronous External Master Access Timing (GPCM Handled ACS = 00)**

Figure 21 provides the timing for the asynchronous external master memory access that the GPCM controls.

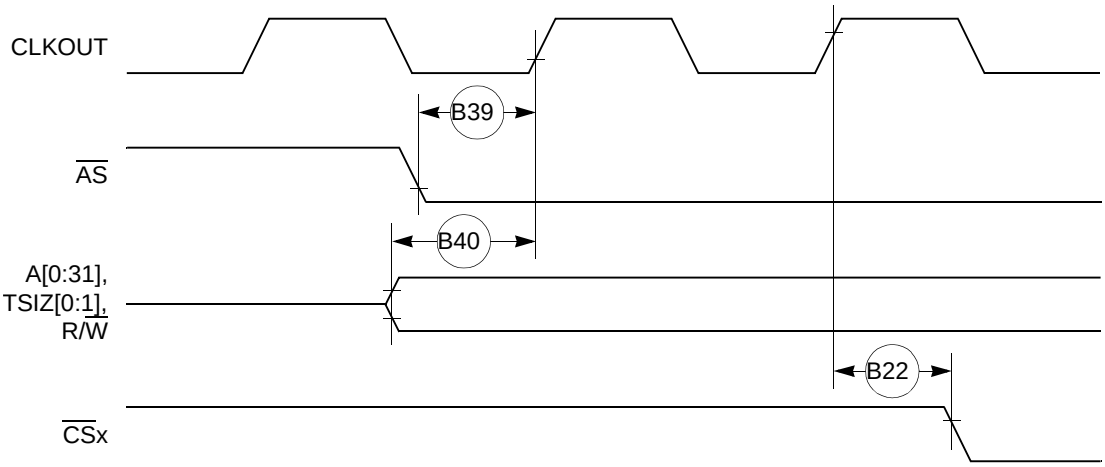


**Figure 21. Asynchronous External Master Memory Access Timing (GPCM Controlled—ACS = 00)**

Figure 22 provides the timing for the asynchronous external master control signals negation.

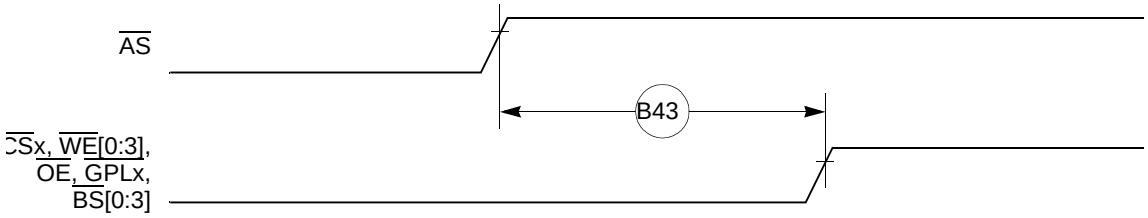


**Figure 22. Asynchronous External Master—Control Signals Negation Timing**

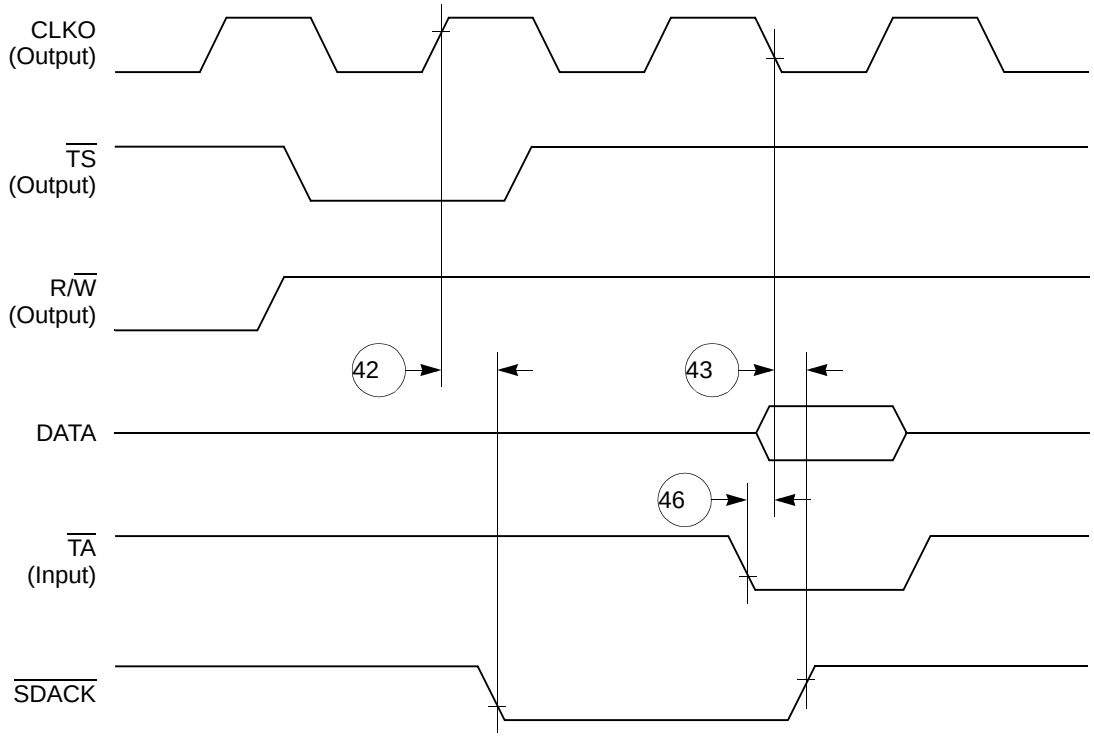


**Figure 41. SDACK Timing Diagram—Peripheral Write, Externally-Generated TA**

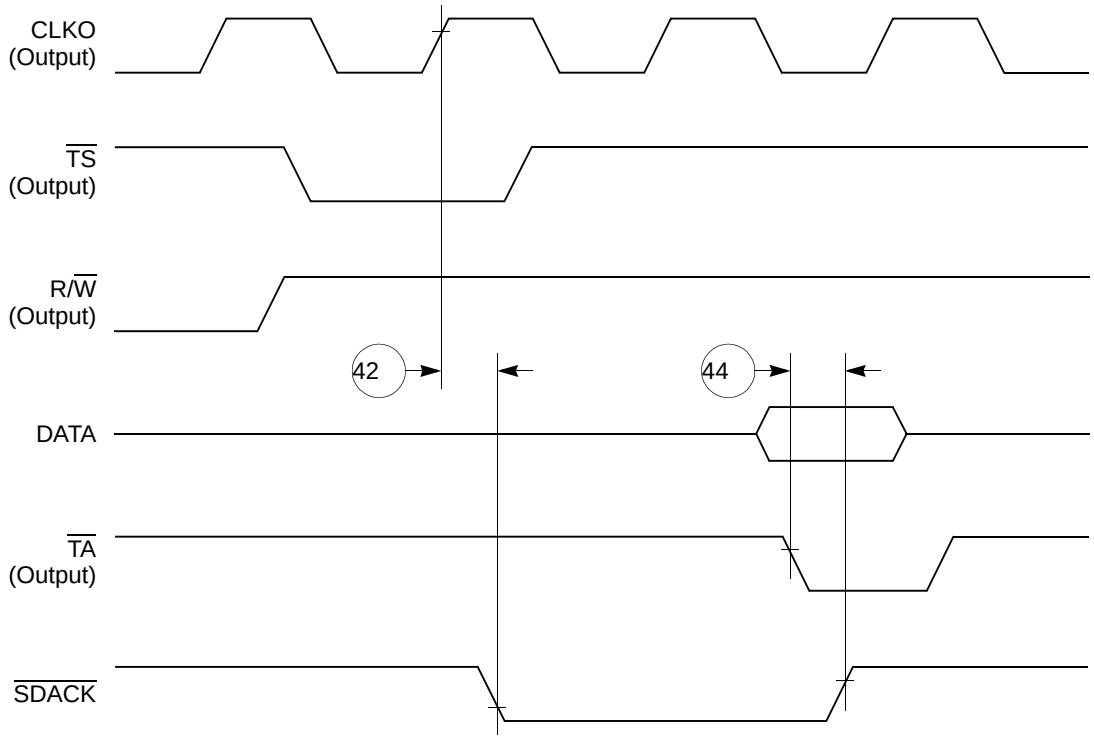


**Figure 42. SDACK Timing Diagram—Peripheral Write, Internally-Generated TA**

Figure 46 through Figure 48 show the NMSI timings.

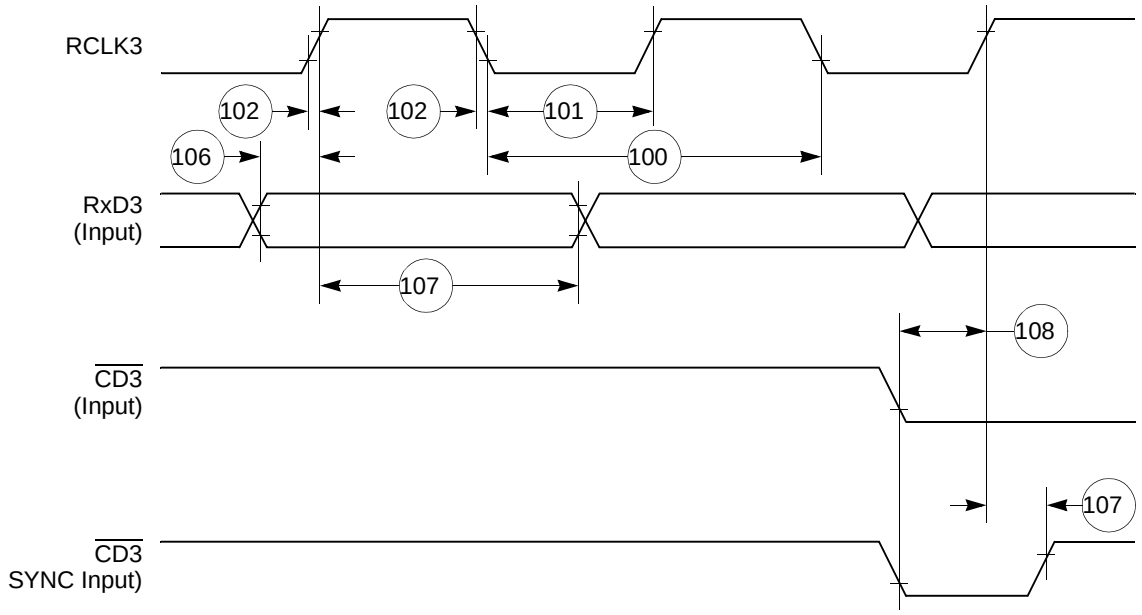


**Figure 46. SCC NMSI Receive Timing Diagram**

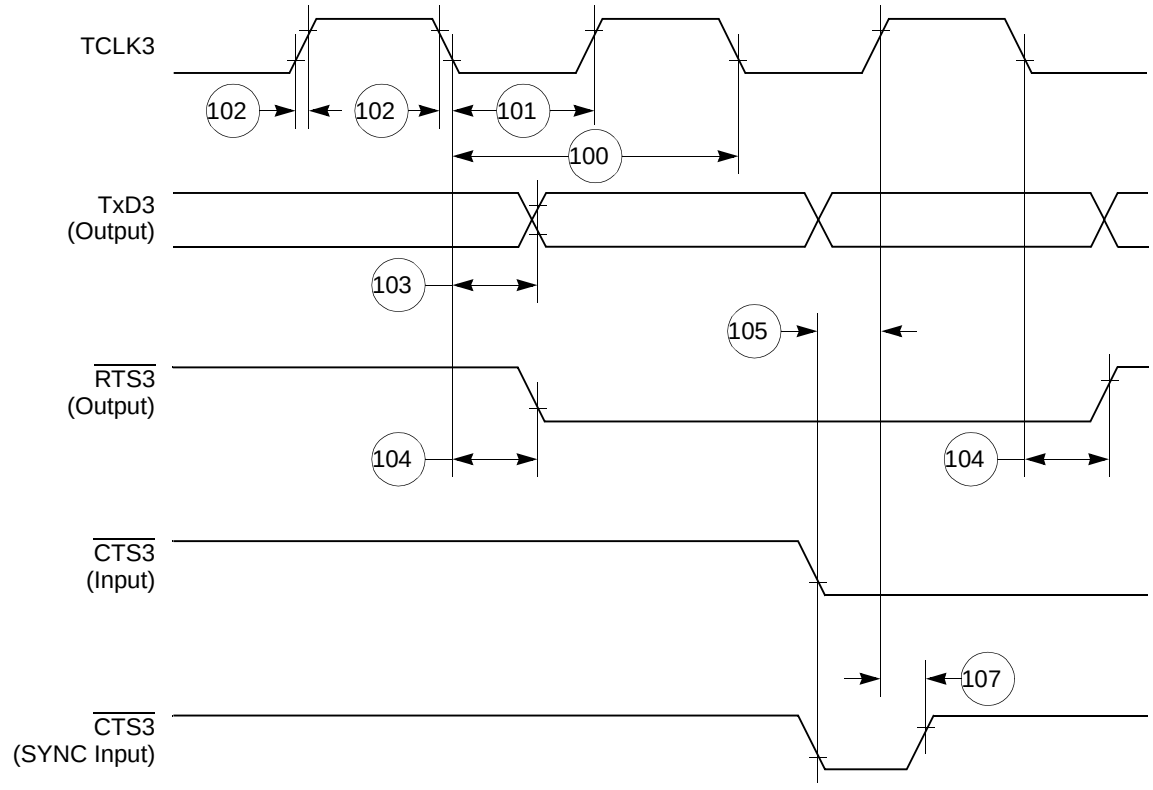


**Figure 47. SCC NMSI Transmit Timing Diagram**

# 14.7 SPI Master AC Electrical Specifications

Table 23 provides the SPI master timings as shown in Figure 54 and Figure 55.

**Table 23. SPI Master Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 160 | MASTER cycle time | 4 | 1024 | $t_{cyc}$ |
| 161 | MASTER clock (SCK) high or low time | 2 | 512 | $t_{cyc}$ |
| 162 | MASTER data setup time (inputs) | 15 | — | ns |
| 163 | Master data hold time (inputs) | 0 | — | ns |
| 164 | Master data valid (after SCK edge) | — | 10 | ns |
| 165 | Master data hold time (outputs) | 0 | — | ns |
| 166 | Rise time output | — | 15 | ns |
| 167 | Fall time output | — | 15 | ns |

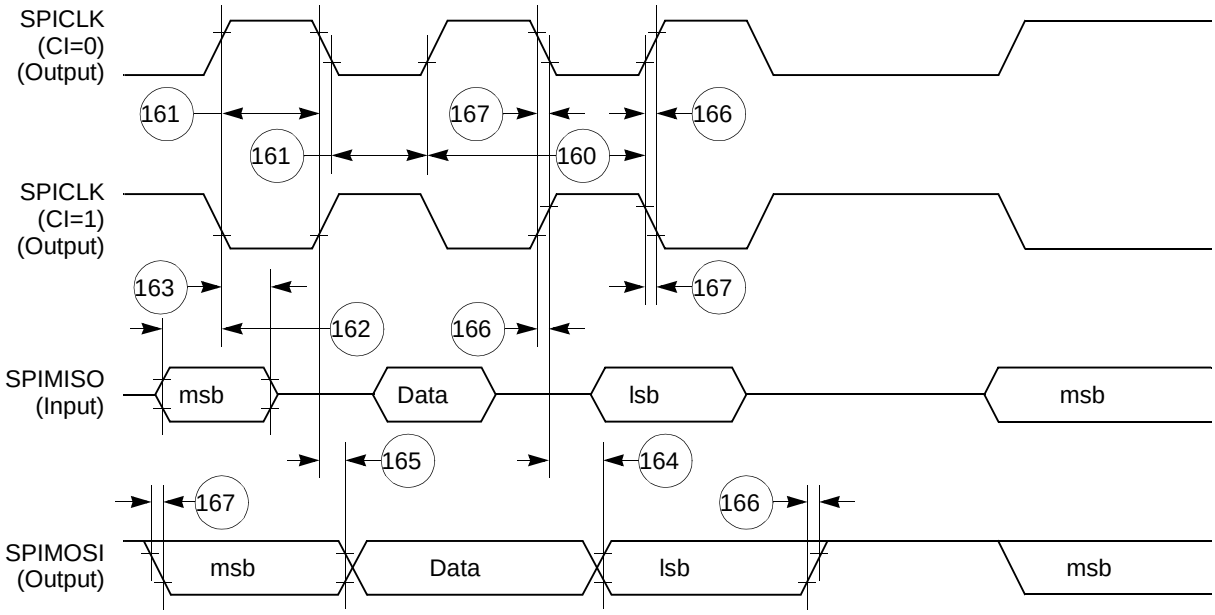


**Figure 54. SPI Master (CP = 0) Timing Diagram**

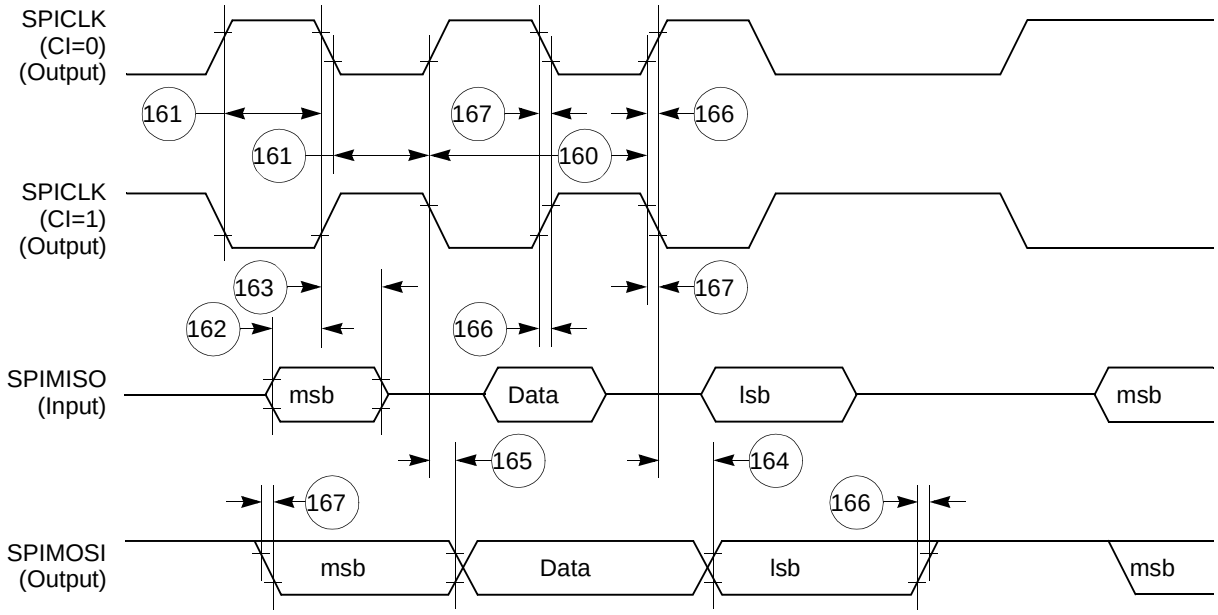


**Figure 55. SPI Master (CP = 1) Timing Diagram**

# 14.8 SPI Slave AC Electrical Specifications

Table 24 provides the SPI slave timings as shown in Figure 56 and Figure 57.

**Table 24. SPI Slave Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 170 | Slave cycle time | 2 | — | $t_{cyc}$ |
| 171 | Slave enable lead time | 15 | — | ns |
| 172 | Slave enable lag time | 15 | — | ns |
| 173 | Slave clock (SPICLK) high or low time | 1 | — | $t_{cyc}$ |
| 174 | Slave sequential transfer delay (does not require deselect) | 1 | — | $t_{cyc}$ |
| 175 | Slave data setup time (inputs) | 20 | — | ns |
| 176 | Slave data hold time (inputs) | 20 | — | ns |
| 177 | Slave access time | — | 50 | ns |

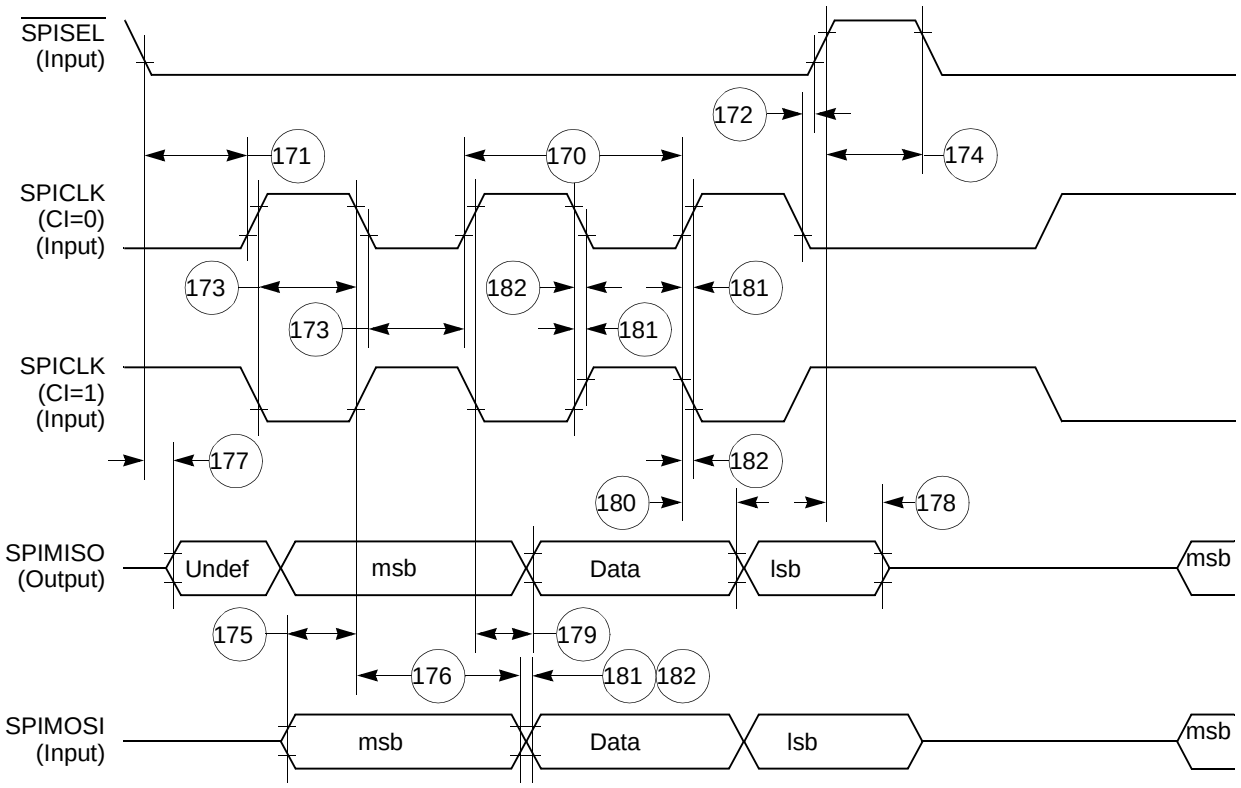


**Figure 57. SPI Slave (CP = 1) Timing Diagram**

# 15 FEC Electrical Characteristics

This section provides the AC electrical specifications for the fast Ethernet controller (FEC). Note that the timing specifications for the MII signals are independent of system clock frequency (part speed designation). Also, MII signals use TTL signal levels compatible with devices operating at either 5.0 V or 3.3 V.

## 15.1 MII Receive Signal Timing (MII_RXD[3:0], MII_RX_DV, MII_RX_ER, MII_RX_CLK)

The receiver functions correctly up to a MII_RX_CLK maximum frequency of 25MHz +1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII_RX_CLK frequency - 1%.

Table 25 provides information on the MII receive signal timing.

**Table 25. MII Receive Signal Timing**

| Num | Characteristic | Min | Max | Unit |
|---|---|---|---|---|
| M1 | MII_RXD[3:0], MII_RX_DV, MII_RX_ER to MII_RX_CLK setup | 5 | — | ns |
| M2 | MII_RX_CLK to MII_RXD[3:0], MII_RX_DV, MII_RX_ER hold | 5 | — | ns |
| M3 | MII_RX_CLK pulse width high | 35% | 65% | MII_RX_CLK period |
| M4 | MII_RX_CLK pulse width low | 35% | 65% | MII_RX_CLK period |

## 16.1.2 The non-JEDEC Pinout

Figure 63 shows the non-JEDEC pinout of the PBGA package as viewed from the top surface. For additional information, see the *MPC866 PowerQUICC Family User's Manual*.

**NOTE: This figure shows the top view of the device.**

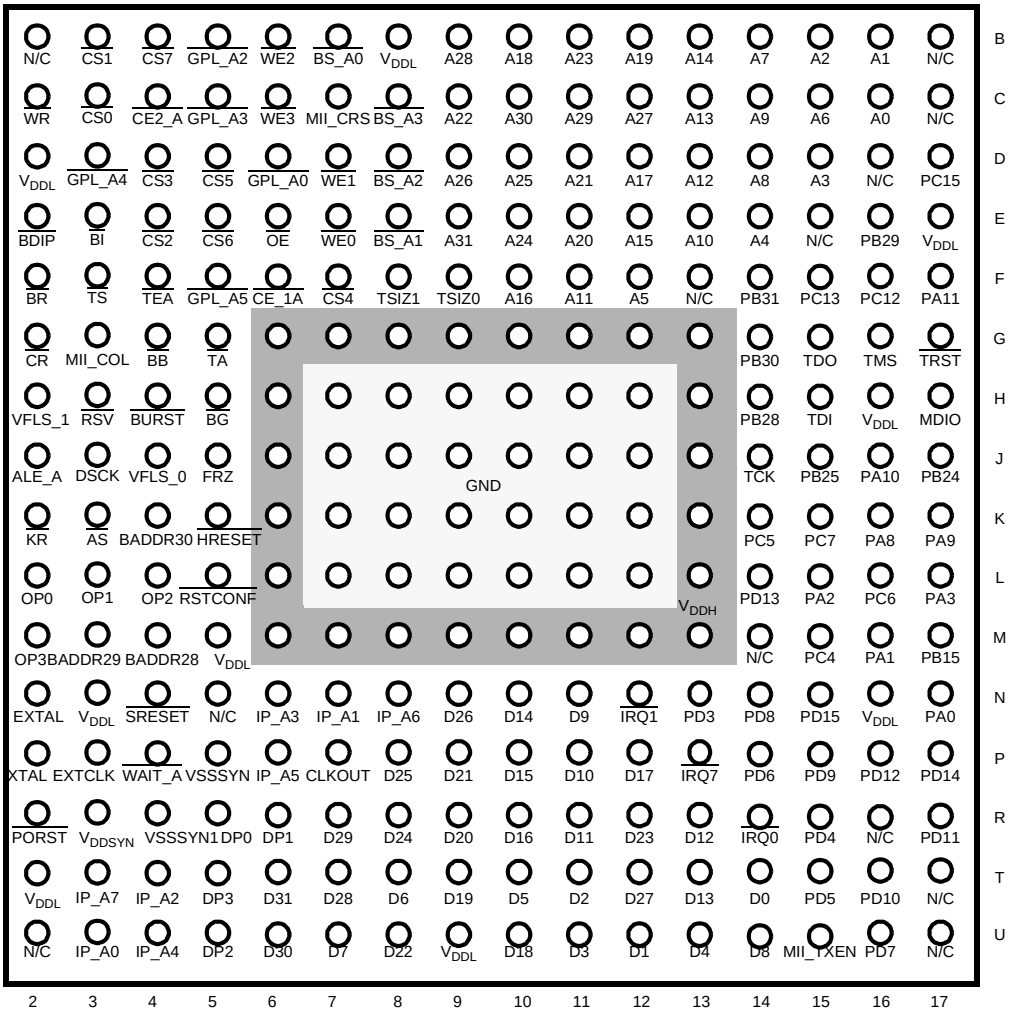


**Figure 63. Pinout of the PBGA Package - non-JEDEC**

**Table 31. Pin Assignments - non-JEDEC (continued)**

| Name | Pin Number | Type |
|---|---|---|
| $\overline{\text{RSTCONF}}$ | L5 | Input (3.3 V only) |
| $\overline{\text{HRESET}}$ | K5 | Open-drain |
| $\overline{\text{SRESET}}$ | N4 | Open-drain |
| XTAL | P2 | Analog Output |
| EXTAL | N2 | Analog Input (3.3 V only) |
| CLKOUT | P7 | Output |
| EXTCLK | P3 | Input (3.3 V only) |
| ALE_A | J2 | Output |
| $\overline{\text{CE1\_A}}$ | F6 | Output |
| $\overline{\text{CE2\_A}}$ | C4 | Output |
| $\overline{\text{WAIT\_A}}$ | P4 | Input (3.3 V only) |
| IP_A0 | U3 | Input (3.3 V only) |
| IP_A1 | N7 | Input (3.3 V only) |
| IP_A2<br>$\overline{\text{IOIS16\_A}}$ | T4 | Input (3.3 V only) |
| IP_A3 | N6 | Input (3.3 V only) |
| IP_A4 | U4 | Input (3.3 V only) |
| IP_A5 | P6 | Input (3.3 V only) |
| IP_A6 | N8 | Input (3.3 V only) |
| IP_A7 | T3 | Input (3.3 V only) |
| DSCK | J3 | Bidirectional<br>Three-state (3.3 V only) |
| IWP[0:1]<br>VFLS[0:1] | J4, H2 | Bidirectional (3.3 V only) |
| OP0 | L2 | Bidirectional (3.3 V only) |
| OP1 | L3 | Output |
| OP2<br>MODCK1<br>$\overline{\text{STS}}$ | L4 | Bidirectional (3.3 V only) |
| OP3<br>MODCK2<br>DSDO | M2 | Bidirectional (3.3 V only) |
| BADDR[28:29] | M4, M3 | Output |
| BADDR30<br>$\overline{\text{REG}}$ | K4 | Output |

**Table 31. Pin Assignments - non-JEDEC (continued)**

| Name | Pin Number | Type |
|---|---|---|
| PD9<br>RXD4<br>MII_TXD0 | P15 | Bidirectional<br>(5 V-tolerant) |
| PD8<br>TXD4<br>MII_RX_CLK | N14 | Bidirectional<br>(5 V-tolerant) |
| PD7<br>$\overline{\text{RTS3}}$<br>MII_RX_ER | U16 | Bidirectional<br>(5 V-tolerant) |
| PD6<br>$\overline{\text{RTS4}}$<br>MII_RX_DV | P14 | Bidirectional<br>(5 V-tolerant) |
| PD5<br>MII_TXD3 | T15 | Bidirectional<br>(5 V-tolerant) |
| PD4<br>MII_TXD2 | R15 | Bidirectional<br>(5 V-tolerant) |
| PD3<br>MII_TXD1 | N13 | Bidirectional<br>(5 V-tolerant) |
| TMS | G16 | Input<br>(5 V-tolerant) |
| TDI<br>DSDI | H15 | Input<br>(5 V-tolerant) |
| TCK<br>DSCK | J14 | Input<br>(5 V-tolerant) |
| $\overline{\text{TRST}}$ | G17 | Input<br>(5 V-tolerant) |
| TDO<br>DSDO | G15 | Output<br>(5 V-tolerant) |
| MII_CRS | C7 | Input |
| MII_MDIO | H17 | Bidirectional<br>(5 V-tolerant) |
| MII_TX_EN | U15 | Output<br>(5 V-tolerant) |
| MII_COL | G3 | Input |
| $V_{SSSYN}$ | P5 | PLL analog GND |
| $V_{SSSYN1}$ | R4 | PLL analog GND |
| $V_{DDSYN}$ | R3 | PLL analog $V_{DD}$ |

## 16.2 Mechanical Dimensions of the PBGA Package

For more information on the printed circuit board layout of the PBGA package, including thermal via design and suggested pad layout, refer to Plastic Ball Grid Array Application Note (order number: AN1231/D) that is available from your local Motorola sales office. Figure 64 shows the mechanical dimensions of the PBGA package.