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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM7®
Core Size	32-Bit Single-Core
Speed	77.4MHz
Connectivity	EBI/EMI, Ethernet, I²C, SSP, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	88
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LFBGA
Supplier Device Package	208-CABGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/socle/lh79524n0f100a0

SIGNAL DESCRIPTIONS

Table 1. LH79524 Pin Descriptions

CABGA PIN	SIGNAL NAME	TYPE	DESCRIPTION
T12	A0	O	External Address Bus
R11	A1		
T11	A2		
P10	A3		
R10	A4		
T10	A5		
P9	A6		
R9	A7		
T9	A8		
T8	A9		
R8	A10		
P8	A11		
T7	A12		
R7	A13		
P7	A14		
T6	A15		
M15	D0	I/O	External Data Bus
N16	D1		
L13	D2		
M14	D3		
N15	D4		
P16	D5		
M13	D6		
N14	D7		
F14	SDCLK	O	SDRAM Clock
G15	SDCKE	O	SDRAM Clock Enable
D13	DQM0	O	Data Mask Output to SDRAMs
E13	DQM1		
E14	DQM2		
G14	DQM3		
G16	nDCS0	O	SDRAM Chip Select
H14	nDCS1	O	SDRAM Chip Select
H15	nRAS	O	Row Address Strobe
H16	nCAS	O	Column Address Strobe
L16	nCS0/PM0	O	Static Memory Chip Select; multiplexed with GPIO Port M[3:0] (output only)
L15	nCS1/PM1		
M16	nCS2/PM2		
L14	nCS3/PM3		
J15	nBLE0/PM4	O	Static Memory Byte Lane Enable / Byte Write Enable; multiplexed with GPIO Port M[7:4] (output only)
J14	nBLE1/PM5		
K16	nBLE2/PM6		
K15	nBLE3/PM7		

Table 1. LH79524 Pin Descriptions (Cont'd)

CABGA PIN	SIGNAL NAME	TYPE	DESCRIPTION
M3	PB7/INT1/UARTTX0/ UARTIRTX0	I/O	General Purpose I/O Signal — Port B7; multiplexed with UART0 Infrared Transmitted Serial Data Output, UART0 Serial Transmit Data Out, and External Interrupt 1.
N7	PC0/A16	I/O	General Purpose I/O Signal — Port C0; multiplexed with Address A16
R6	PC1/A17	I/O	General Purpose I/O Signal — Port C1; multiplexed with Address A17
T5	PC2/A18	I/O	General Purpose I/O Signal — Port C2; multiplexed with Address A18
P6	PC3/A19	I/O	General Purpose I/O Signal — Port C3; multiplexed with Address A19
R5	PC4/A20	I/O	General Purpose I/O Signal — Port C4; multiplexed with Address A20
T4	PC5/A21	I/O	General Purpose I/O Signal — Port C5; multiplexed with Address A21
P5	PC6/A22/nFWE	I/O	General Purpose I/O Signal — Port C6; multiplexed with Address A22 and NAND Flash Write Enable
R4	PC7/A23/nFRE	I/O	General Purpose I/O Signal — Port C7; multiplexed with Address A23 and NAND Flash Read Enable
P15	PD0/D8	I/O	General Purpose I/O Signal — Port D0; multiplexed with Data D8
P14	PD1/D9	I/O	General Purpose I/O Signal — Port D1; multiplexed with Data D9
N13	PD2/D10	I/O	General Purpose I/O Signal — Port D2; multiplexed with Data D10
T15	PD3/D11	I/O	General Purpose I/O Signal — Port D3; multiplexed with Data D11
N12	PD4/D12	I/O	General Purpose I/O Signal — Port D4; multiplexed with Data D12
T14	PD5/D13	I/O	General Purpose I/O Signal — Port D5; multiplexed with Data D13
P12	PD6/D14	I/O	General Purpose I/O Signal — Port D6; multiplexed with Data D14
T13	PD7/D15	I/O	General Purpose I/O Signal — Port D7; multiplexed with Data D15
B12	PE0/LCDLP/ LCDHRLP	I/O	General Purpose I/O Signals — Port E0; multiplexed with LCD Line Pulse and AD-TFT/HR-TFT Line Pulse
D11	PE1/LCDDCLK	I/O	General Purpose I/O Signals — Port E1; multiplexed with LCD Data Clock
B13	PE2/LCDPS	I/O	General Purpose I/O Signals — Port E2; multiplexed with LCD Power Save
C13	PE3/LCDCLS	I/O	General Purpose I/O Signals — Port E3; multiplexed with LCD Row Driver Clock
D12	PE4/LCDDSPLEN/ LCDREV	I/O	General Purpose I/O Signals — Port E4; multiplexed with LCD Panel Power Enable and LCD Reverse
B16	PE5/LCDVDDEN	I/O	General Purpose I/O Signals — Port E5; multiplexed with LCD VDD Enable
B15	PE6/LCDVEEN/ LCDMOD	I/O	General Purpose I/O Signals — Port E6; multiplexed with LCD Analog Power Enable and MOD
D14	PE7/nWAIT/nDEOT	I/O	General Purpose I/O Signals — Port E7; multiplexed with nWAIT and DMA End of Transfer
A8	PF0/LCDVD6	I/O	General Purpose I/O Signals — Port F0; multiplexed with LCD Video Data bit 6
A9	PF1/LCDVD7	I/O	General Purpose I/O Signals — Port F1; multiplexed with LCD Video Data bit 7
B9	PF2/LCDVD8	I/O	General Purpose I/O Signals — Port F2; multiplexed with LCD Video Data bit 8
C9	PF3/LCDVD9	I/O	General Purpose I/O Signals — Port F3; multiplexed with LCD Video Data bit 9
B10	PF4/LCDVD10	I/O	General Purpose I/O Signals — Port F4; multiplexed with LCD Video Data bit 10
A11	PF5/LCDVD11	I/O	General Purpose I/O Signals — Port F5; multiplexed with LCD Video Data bit 11
B11	PF6/LCDEN/LCDSPL	I/O	General Purpose I/O Signals — Port F6; multiplexed with LCD Start Pulse Left
A12	PF7/LCDFP/LCDSPS	I/O	General Purpose I/O Signals — Port F7; multiplexed with LCD Row Driver Counter reset
A5	PG0/ETHERTXEN	I/O	General Purpose I/O Signals — Port G0; multiplexed with Ethernet TX Enable
B6	PG1/ETHERTXCLK	I/O	General Purpose I/O Signals — Port G1; multiplexed with Ethernet TX Clock
A6	PG2/LCDVD0	I/O	General Purpose I/O Signals — Port G2; multiplexed with LCD Video Data bit 0
C7	PG3/LCDVD1	I/O	General Purpose I/O Signals — Port G3; multiplexed with LCD Video Data bit 1
B7	PG4/LCDVD2	I/O	General Purpose I/O Signals — Port G4; multiplexed with LCD Video Data bit 2

Table 4. LH79525 Pin Descriptions (Cont'd)

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION
20	AN3/LR/Y–/PJ0	I	ADC Input 3, 4 wire touch screen Upper Right, 5 wire touch screen Y–; multiplexed with GPIO Port J0 (input only)
19	AN4/WIPER/PJ1	I	ADC Input 4, 5 wire touch screen Wiper input; multiplexed with Port J1 (input only)
15	AN5/PJ5/INT5	I	ADC Input 5; multiplexed with GPIO Port J5 (input only) and External Interrupt 5
12	AN6/PJ7/INT7	I	ADC Input 6; multiplexed with GPIO Port J7 (input only) and External Interrupt 7
13	AN7/PJ6/INT6	I	ADC Input 7; multiplexed with GPIO Port J6 (input only) and External Interrupt 6
16	AN8/PJ4	I	ADC Input 8; multiplexed with GPIO Port J4 (input only)
18	AN9/PJ2	I	ADC Input 9; multiplexed with GPIO Port J2 (input only)
25	CTCLK/INT4/ BATCNTL	I/O	Timer[2:0] External Clock input; multiplexed with Battery Control and Interrupt 4
36	PA0/UARTRX2/ UARTIRRX2/INT2	I/O	General Purpose I/O Signal — Port A0; multiplexed with UART2 Received Serial Data Input, UART2 Infrared Received Serial Data In, and External Interrupt 2
35	PA1/UARTTX2/ UARTIRRX2/INT3	I/O	General Purpose I/O Signal — Port A1; multiplexed with UART2 Transmitted Serial Data Output, UART2 Serial Transmit Data Out, and External Interrupt 3
34	PA2/CTCAP0A/ CTCMP0A	I/O	General Purpose I/O Signal — Port A2; multiplexed with Counter/Timer 0 Capture A input and Counter/Timer 0 Compare A output
32	PA3/CTCAP0B/ CTCMP0B	I/O	General Purpose I/O Signal — Port A3; multiplexed with Counter/Timer 0 Capture B input and Counter/Timer 0 Compare B output
31	PA4/CTCAP1A/ CTCMP1A	I/O	General Purpose I/O Signal — Port A4; multiplexed with Counter/Timer 1 Capture A input and Counter/Timer 1 Compare A output
30	PA5/CTCAP1B/ CTCMP1B	I/O	General Purpose I/O Signal — Port A5; multiplexed with Counter/Timer 1 Capture B input and Counter/Timer 1 Compare B output
29	PA6/CTCAP2A/ CTCMP2A/SDA	I/O	General Purpose I/O Signal — Port A6; multiplexed with Counter/Timer 2 Capture A input, Counter/Timer 2 Compare A output, and I^2C Bus Data (open drain)
28	PA7/CTCAP2B/ CTCMP2B/SLC	I/O	General Purpose I/O Signal — Port A7; multiplexed with Counter/Timer 2 Capture B input, Counter/Timer 2 Compare B output, and I^2C Bus Clock (open drain)
44	PB0/nDACK/ nUARTCTS0	I/O	General Purpose I/O Signal — Port B0; multiplexed with DMA Acknowledge and UART0 CTS
43	PB1/DREQ/ nUARTRTS0	I/O	General Purpose I/O Signal — Port B1; multiplexed with DMA Request and UART0 RTS
42	PB2/SSPFRM/ I2SWS	I/O	General Purpose I/O Signal — Port B2; multiplexed with SSP Serial Frame Output and I^2S Frame Output
41	PB3/SSPCLK/ I2SCLK	I/O	General Purpose I/O Signal — Port B3; multiplexed with SSP Clock and I^2S Clock
40	PB4/SSPRX/ I2SRXD/UARTRX1/ UARTIRRX1	I/O	General Purpose I/O Signal — Port B4; multiplexed with SSP Data In, I^2S Data In, UART1 Serial Data In, and UART1 Infrared Data In
39	PB5/SSPTX/ I2STXD/UARTTX1/ UARTIRTX1	I/O	General Purpose I/O Signal — Port B5; multiplexed with SSP Data Out, I^2S Data Out, UART1 Data Out, and UART1 IR Data Out
38	PB6/INT0/ UARTRX0/ UARTIRRX0	I/O	General Purpose I/O Signal — Port B6; multiplexed with UART0 Infrared Received Serial Data Input, UART0 Received Serial Data In, and External Interrupt 0
37	PB7/INT1/ UARTTX0/ UARTIRTX0	I/O	General Purpose I/O Signal — Port B7; multiplexed with UART0 Infrared Transmitted Serial Data Output, UART0 Serial Transmit Data Out, and External Interrupt 1
60	PC0/A16	I/O	General Purpose I/O Signal — Port C0; multiplexed with Address A16
59	PC1/A17	I/O	General Purpose I/O Signal — Port C1; multiplexed with Address A17
58	PC2/A18	I/O	General Purpose I/O Signal — Port C2; multiplexed with Address A18
56	PC3/A19	I/O	General Purpose I/O Signal — Port C3; multiplexed with Address A19
55	PC4/A20	I/O	General Purpose I/O Signal — Port C4; multiplexed with Address A20
54	PC5/A21	I/O	General Purpose I/O Signal — Port C5; multiplexed with Address A21

Table 5. LH79525 Numerical Pin List (Cont'd)

PIN NO.	FUNCTION AT RESET	MULTIPLEXED FUNCTION(S)	OUTPUT DRIVE	NOTES
97	D2		8 mA	1
98	D1		8 mA	1
99	D0		8 mA	1
100	nCS3	PM3	8 mA	
101	VDD			
102	nCS2	PM2	8 mA	
103	nCS1	PM1	8 mA	
104	nCS0	PM0	8 mA	
105	VSSC			
106	nOE		8 mA	
107	VDDC			
108	VSS			
109	nBLE1	PM5	8 mA	
110	nBLE0	PM4	8 mA	
111	nWE		8 mA	
112	nCAS		8 mA	
113	nRAS		8 mA	
114	nDCS1		8 mA	
115	nDCS0		8 mA	
116	SDCKE		8 mA	
117	SDCLK		12 mA	
118	DQM1		8 mA	
119	DQM0		8 mA	
120	PE7	nWAIT/nDEOT	8 mA	2, 3
121	VSSA1			
122	VDDA1			
123	VDDA2			
124	VSSA2			
125	XTAL32IN			5
126	XTAL32OUT			6
127	XTALIN			5
128	XTALOUT			6
129	VDD			
130	USBDN			7
131	USBDP			7
132	VSS			
133	PE6	LCDVEEN/ LCDMOD	8 mA	1
134	PE5	LCDVDDEN	8 mA	1
135	VDD			
136	PE4	LCDDSPLEN/LCDREV	8 mA	1
137	PE3	LCDCLS	8 mA	1
138	PE2	LCDPS	8 mA	1
139	PE1	LCDDCLK	8 mA	1
140	VSS			
141	PE0	LCDLP/LCDHRLP	8 mA	1
142	PF7	LCDFP/LCDSPS	8 mA	1
143	PF6	LCDEN/LCDSPL	8 mA	1
144	VDD			
145	PF5	LCDVD11	8 mA	2
146	PF4	LCDVD10	8 mA	2

Table 5. LH79525 Numerical Pin List (Cont'd)

PIN NO.	FUNCTION AT RESET	MULTIPLEXED FUNCTION(S)	OUTPUT DRIVE	NOTES
147	PF3	LCDVD9	8 mA	2
148	VSSC			
149	PF2	LCDVD8	8 mA	2
150	VDDC			
151	PF1	LCDVD7	8 mA	1
152	VSS			
153	PF0	LCDVD6	8 mA	1
154	PG7	LCDVD5	8 mA	1
155	PG6	LCDVD4	8 mA	1
156	PG5	LCDVD3	8 mA	1
157	PG4	LCDVD2	8 mA	1
158	PG3	LCDVD1	8 mA	1
159	PG2	LCDVD0	8 mA	1
160	VDD			
161	PG1	ETHERTXCLK	8 mA	1
162	PG0	ETHERTXEN	8 mA	1
163	PH7	ETHERTX3	8 mA	1
164	PH6	ETHERTX2	8 mA	1
165	PH5	ETHERTX1	8 mA	1
166	PH4	ETHERTX0	8 mA	1
167	PH3	ETHERTXER	8 mA	1
168	VSS			
169	PH2	ETHERRXCLK	8 mA	1
170	PH1	ETHERRXDV	8 mA	1
171	PH0	ETHERRX3	8 mA	1
172	PI7	ETHERRX2	8 mA	1
173	PI6	ETHERRX1	8 mA	1
174	PI5	ETHERRX0	8 mA	1
175	PI4	ETHERRXER	8 mA	1
176	PI3	ETHERCRS	8 mA	1

NOTES:

1. Internal pull-down. The internal pullup and pulldown resistance on all digital I/O pins is 50KΩ
2. Internal pull-up. The internal pullup and pulldown resistance on all digital I/O pins is 50KΩ
3. Input with Schmitt Trigger.
4. Crystal Inputs should be driven to a maximum of 1.8 V ± 10%.
5. Output is for crystal oscillator only, no drive capability.
6. USB Inputs/outputs are tristated.
7. Output Drive Values shown are MAX. See 'DC Specifications'.
8. All unused analog pins, and XTAL32IN (if unused) should be tied to ground through a 33KΩ resistor.

Table 6. TESTx PIN FUNCTION

MODE	TEST1	TEST2	nBLE0
Embedded ICE	0	1	1
Normal	1	1	x

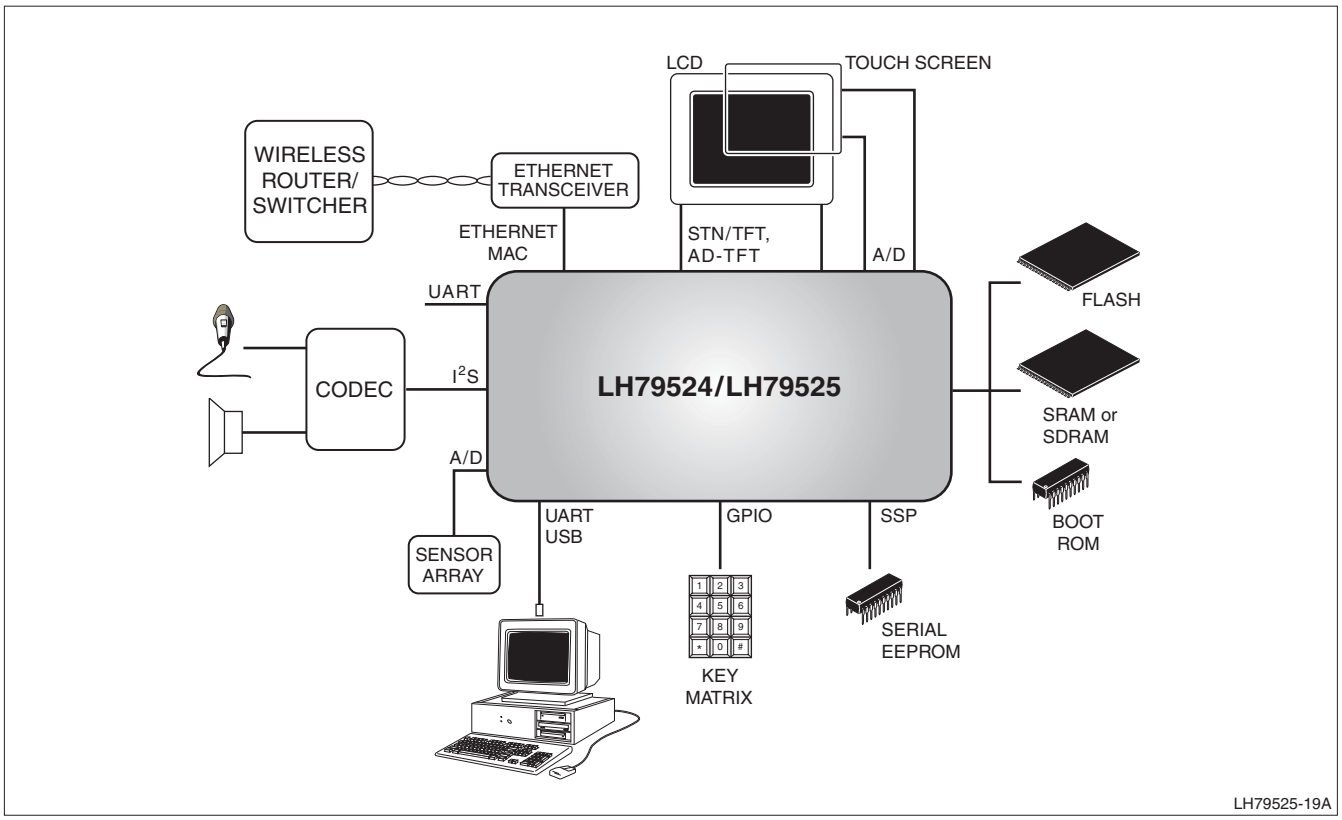


Figure 2. LH79524/LH79525 Application Diagram Example

SYSTEM DESCRIPTIONS

ARM720T Processor

The LH79524/LH79525 microcontrollers feature the ARM720T cached core with an Advanced High-Performance Bus (AHB) interface. The ARM720T features:

- 32-bit ARM720T RISC Core
- 8KB Cache
- MMU (Windows CE enabled)

The core processor for both is a member of the ARM7T family of processors. For more information, see the ARM document, 'ARM720T (Rev 3) Technical Reference Manual', available on ARM's website at www.ARM.com.

The LH79524/LH79525 MMU allows mapping Physical Memory (PA) addresses to virtual memory addresses. This allows physical memory, which is constrained by hardware to specific addresses, to be reorganized at addresses identified by the user. These user identified locations are called Virtual Addresses (VA). When the MMU is enabled, Code and Data must be built, loaded, and executed using Virtual Addresses which the MMU translates to Physical Addresses. In addition, the user may implement a memory protection scheme by using the features of the MMU. Address translation and memory protection services provided by the MMU are controlled by the user. The MMU is directly controlled through the System Control Coprocessor, Coprocessor 15 (CP15). The MMU is indirectly controlled by a Translation Table (TT) and Page Tables (PT) prepared by the user and established using a portion of physical memory dedicated by the user to storing the TT and PT's.

External Memory Controller

An integrated External Memory Controller (EMC) provides a glueless interface to external SDRAM, Low Power SDRAM, Flash, SRAM, ROM, and burst ROM. Three remap options for the physical memory are selectable by software, as shown in Figure 3 through Figure 6.

The EMC supports six banks of external memory. Two chip selects for synchronous memory, and either two (LH79525) or four (LH79524) static memory chip selects are available. The static interface also includes two (LH79525) or four (LH79524) byte lane enable signals.

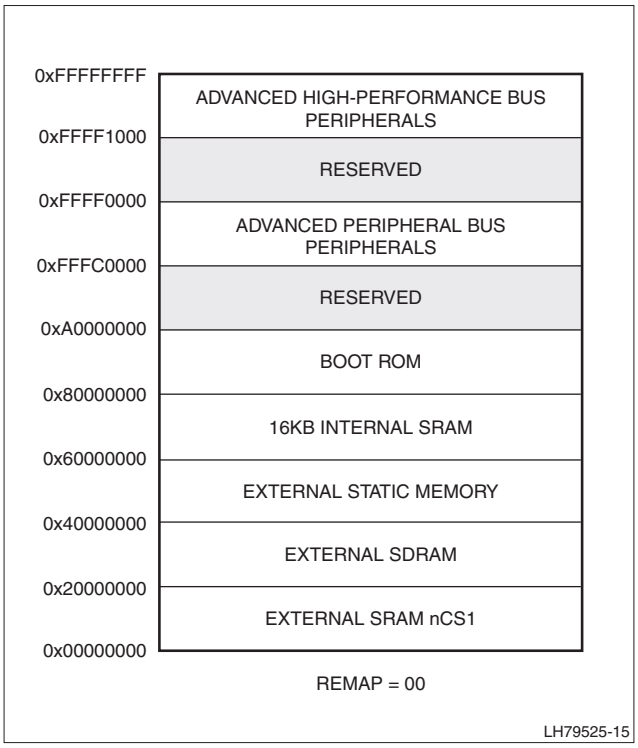


Figure 3. Memory Remap '00'

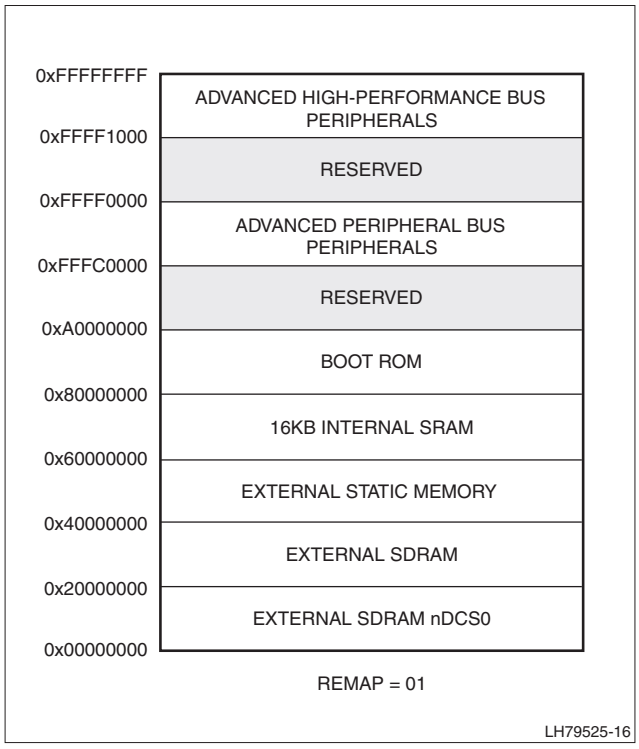


Figure 4. Memory Remap '01'

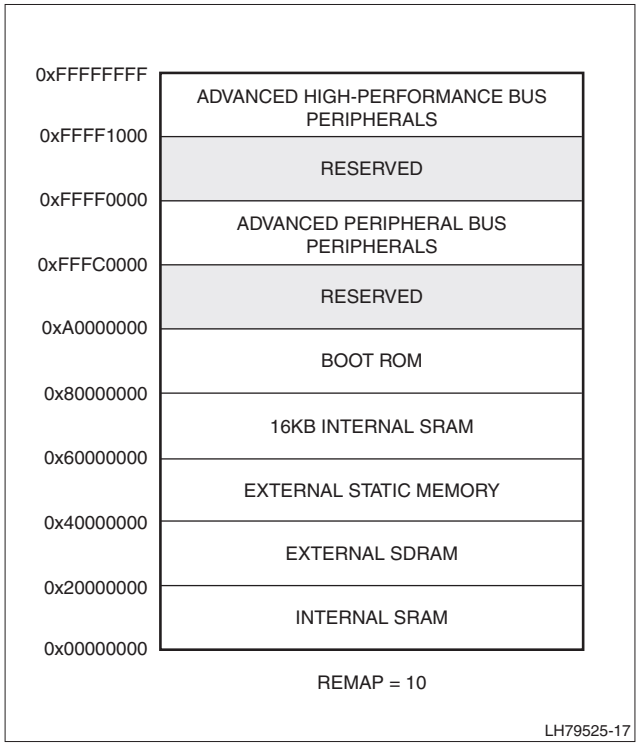


Figure 5. Memory Remap '10'

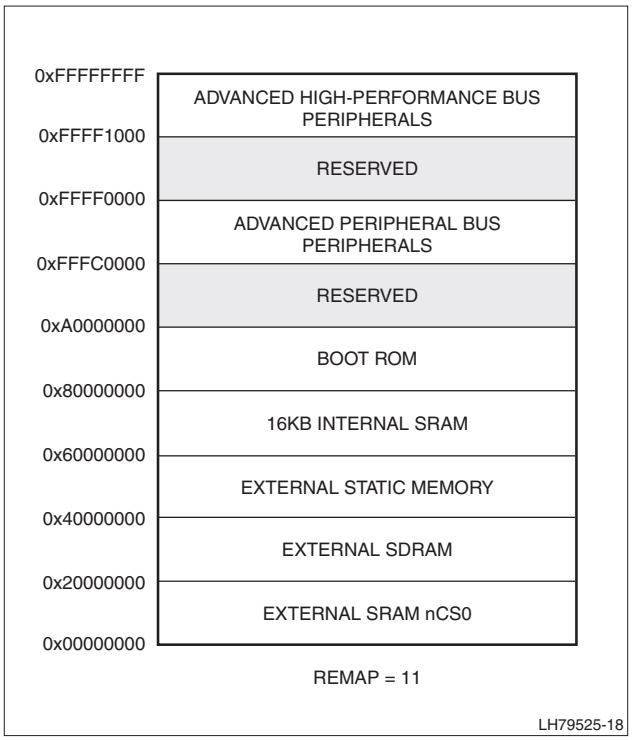


Figure 6. Memory Remap '11'

DMA Controller

The DMA Controller provides support for DMA-capable peripherals. The LCD controller uses its own DMA port, connecting directly to memory for retrieving display data.

- Simultaneous servicing of up to 4 data streams
- Three transfer modes are supported:
  - Memory to Memory
  - Peripheral to Memory
  - Memory to Peripheral
- Identical source and destination capabilities
- Transfer Size Programmable (byte, half-word, word)
- Burst Size Programmable
- Address Increment or Address Freeze
- Transfer Error interrupt for each stream
- 16-word FIFO array with pack and unpack logic

Handles all combinations of byte, half-word or word transfers from input to output.

Color LCD Controller (CLCDC)

The CLCDC provides all the necessary control and drive signals to interface directly with a variety of color and monochrome LCD panels.

- LH79524 has 16 LCD Data bits; LH79525 has 12 LCD Data bits.
- Supports single and dual scan color and monochrome Super Twisted Nematic (STN) displays with 4- or 8-bit interfaces (LH79524 only)
- Supports Thin Film Transistor (TFT) color displays
- Programmable resolution up to 1,024 × 1,024
- 15 gray-level mono, 3,375 color STN, and 64 k color TFT support
- 1, 2, or 4 bits-per-pixel (BPP) for monochrome STN
- 1-, 2-, 4-, or 8-BPP palettized color displays for color STN and TFT (1-, 2-, or 4-bit only on LH79525)
- True-color non-palettized, for color STN and TFT
- Programmable timing for different display panels
- 256-entry, 16-bit palette fast-access RAM
- Frame, line and pixel clock signals
- AC bias signal for STN or data enable signal for TFT panels
- Patented grayscale algorithm
- Interrupt Generation Events
- Dual 16-deep programmable 32-bit wide FIFOs for buffering incoming data.

ADVANCED LCD INTERFACE

The Advanced LCD Interface (ALI) allows for direct connection to ultra-thin panels that do not include a timing ASIC. It converts TFT signals from the Color LCD controller to provide the proper signals, timing and levels for direct connection to a panel's Row and Column drivers for AD-TFT, HR-TFT, or any technology of panel that allows for a connection of this type. The Advanced LCD Interface peripheral also provides a bypass mode that allows the LH79524/LH79525 to interface to the built-in timing ASIC in standard TFT and STN panels.

Synchronous Serial Port (SSP)

The SSP is a master or slave interface for synchronous serial communication with master or slave peripheral devices that support protocols for Motorola SPI, National Semiconductor MICROWIRE, or Texas Instruments Synchronous Serial Interface.

- Master or slave operation
- Programmable clock rate
- Separate transmit FIFO and receive FIFO buffers, 16 bits wide, 8 locations deep
- DMA for transmit and receive
- Programmable interface protocols: Motorola SPI, National Semiconductor MICROWIRE, or Texas Instruments Synchronous Serial Port
- Programmable data frame size from 4 to 16 bits
- Independent masking of transmit FIFO, receive FIFO and receive overrun interrupts
- Available internal loopback test mode.

Ethernet MAC Controller

The on-board Ethernet MAC Controller (EMAC) is compatible with IEEE 802.3, and has passed the University of New Hampshire (UNH) testing. It supports both 10- and 100-Mbit/s, and full and half duplex operation. Other features include:

- Statistics counter registers for RMON/MIB
- MII interface to the physical layer
- Interrupt generation to signal receive and transmit completion
- Transmit and receive FIFOs
- Automatic pad and CRC generation on transmitted frames
- Automatic discard of frames received with errors
- Address checking logic supports up to four specific (hardware) 48-bit addresses
- Supports promiscuous mode where all valid received frames are copied to memory
- Hash matching of unicast and multicast destination addresses
- Supports physical layer management through MDIO interface
- Supports serial network interface operation
- Support for:
  - Half duplex flow control by forcing collisions on incoming frames
  - Full duplex flow control with recognition of incoming pause frames and hardware generation of transmitted pause frames
  - 802.Q VLAN tagging with recognition of incoming VLAN and priority tagged frames
- Multiple buffers per receive and transmit frame
- Software configures the MAC address
- Jumbo frames of up to 10,240 bytes supported.

I^2C Controller

The I^2C Controller includes a two-wire I^2C serial interface capable of operating in either Master or Slave mode. The block conforms to the I^2C 2.1 Bus Specification for data rates up to 400 kbit/s. The two wires are SCL (serial clock) and SDA (serial data). The I^2C module provides the following features:

- Two-wire synchronous serial interface
- Operates in both the standard mode, for data rates up to 100 kbit/s, and the fast mode, with data rates up to 400 kbit/s
- Communicates with devices in the fast mode as well as the standard mode if both are attached to the bus.

SSP To I^2S Converter

The SSP to I^2S converter is an interface that converts a synchronous serial communication stream in TI DSP-compatible mode into an I^2S compliant synchronous serial stream. The I^2S converter operates on serial data in both master and slave mode.

The I^2S converter provides:

- Programmable Word Select (WS) delay
- Left/right channel information:
  - Current WS value at the pin
  - WS value associated with next entry written to TX FIFO
  - WS value associated with next entry read from RX FIFO
- Ability to invert WS state
- Ability to invert the bit clock
- Supports frame size of 16 bits only. Any other frame size will result in a frame size error. Each frame transmits starting with the most-significant bit.
- Master and slave modes supported
- As with the SSP, a single combined interrupt is generated as an OR function of the individual interrupt requests. This interrupt replaces the SSP interrupt, which is used solely as an input to the I^2S converter.
- Additional interrupts:
  - Transmit FIFO underrun
  - Transmit frame size error
  - Receive frame size error
- A set of Interrupt registers contain all the information in the SSPIMSC, SSPRIS, and SSPMIS registers, plus the transmit underrun error and frame size errors
- Additional status bits:
  - Transmit FIFO Full
  - Receive FIFO Empty
- Passes SSP data unaltered when module is not enabled
- Loopback Test Mode support.

Power Supply Sequencing

When the linear regulator is *not* enabled, SHARP recommends that the 1.8 V power supply be energized before the 3.3 V supply. If this is not possible, the 1.8 V supply may not lag the 3.3 V supply by more than 100 µs. If longer delay time is needed, it is recommended that the voltage difference between the two power supplies be within 1.5 V during power supply ramp up. To avoid a potential latchup condition, voltage should be applied to input pins only after the device is powered-on as described above.

DC/AC Specifications

Unless noted, all data provided are based on:

- -40°C to +85°C (Industrial temperature range)
- VDDC = 1.7 V to 1.9 V
- VDD = 3.0 V to 3.6 V, VDDA = 1.7 V to 1.9 V.

DC SPECIFICATIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
VIH	CMOS input HIGH voltage	2.0		5.5	V	CEN = 1
VIL	CMOS input LOW voltage			0.8	V	CEN = 1
VIT+	Positive Input threshold voltage (Schmitt pins)	2.0			V	CSEN = 1
VIT-	Negative Input threshold voltage (Schmitt pins)			0.8	V	CSEN = 1
VHYST	Schmitt trigger hysteresis		0.35		V	CSEN = 1
VOH[1]	Output drive (2 mA type)	2.6			V	IOH = -2 mA
	Output drive (4 mA type)	2.6			V	IOH = -4 mA
	Output drive (8 mA type)	2.6			V	IOH = -8 mA
	Output drive (12 mA type)	2.6			V	IOH = -12 mA
VOL[1]	Output drive (2 mA type)			0.4	V	IOL = 2 mA
	Output drive (4 mA type)			0.4	V	IOL = 4 mA
	Output drive (8 mA type)			0.4	V	IOL = 7 mA
	Output drive (12 mA type)	2.6			V	IOH = 12 mA
RIN	Input leakage pull-up/pull-down resistors		40		kΩ	VIN = VDD or GND (Calculate input leakage current at desired VDD)
IACTIVE	Active current		85		mA	Note 2
ISTANDBY	Standby current		50		mA	Notes 2, 3
ISLEEP	Sleep current		3.8		mA	
ISTOP1	Stop1 current		420		µA	
ISTOP2	Stop2 current		115		µA	RTC ON, Linear Regulator ON
ISTOP2	Stop2 current		95		µA	RTC OFF, Linear Regulator ON
ISTOP2	Stop2 current		45		µA	RTC ON, Linear Regulator OFF
ISTOP2	Stop2 current		25		µA	RTC OFF, Linear Regulator OFF

NOTES:

1. Table 2 details each pin's buffer type.
2. Running Typical Application over operating range.
3. Current measured with CPU stopped and all peripherals enabled

Linear Regulator DC Characteristics.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
IQUIESCENT	Quiescent Current		75		µA
ISLEEPLR	Current with Linear Regulator disabled		8		µA
IOLR	Output Current Range	0.0		200	mA
VOLR	Output Voltage, Linear Regulator		1.84		V

Table 13. AC Signal Characteristics (Cont'd)

SIGNAL	TYPE	LOAD	SYMBOL	MIN.	MAX.	DESCRIPTION
nWE	Output	30 pF	tOVSDW		tSDCLK/2 + 4.5 ns	SDWE Write Enable Valid
			tOHSDW	tSDCLK/2 – 4.0 ns		SDWE Write Enable Hold
SDCKE	Output	30 pF	tOVC0		tSDCLK/2 + 4.5 ns	SDCKE Clock Enable Valid
			tOHC0	tSDCLK/2 – 4.0 ns		SDCKE Clock Enable Hold
DQM[3:0]	Output	30 pF	tOVDQ		tSDCLK/2 + 5.0 ns	DQM Data Mask Valid
			tOHDQ	tSDCLK/2 – 4.0 ns		DQM Data Mask Hold
nSDCS[1:0]	Output	30 pF	tOVSC		tSDCLK/2 + 4.5 ns	SDCS Data Mask Valid
			tOHSC	tSDCLK/2 – 4.0 ns		SDCS Data Mask Hold
SDCLK	Output	30 pF	tSDCLK	19.37 ns		SDRAM Clock Period
SYNCHRONOUS SERIAL PORT (SSP)						
SSPFRM	Output	50 pF	tOVSSPFRM		14 ns	tOVSSPFRM Output Valid, Referenced to SSPCLK
SSPTX	Output	50 pF	tOVSSPTX		14 ns	SSP Transmit Valid
SSPRX	Input		tISSPRX	20 ns		SSP Receive Setup
ETHERNET MAC CONTROLLER (EMC)						
ETHERTXER	Output	50 pF	tOVTXER		25 ns	Transmit Data Valid after ETHERTXCLK
			tOHTXER	ETHERTXCLK/2 + 2.0 ns		Transmit Data Hold after ETHERTXCLK
ETHERTX[3:0]	Output	50 pF	tOVTXD		25 ns	Transmit Data Valid after ETHERTXCLK
			tOHTXD	ETHERTXCLK/2 + 2.0 ns		Transmit Data Hold after ETHERTXCLK
ETHERTXEN	Output	50 pF	tOVTXEN		25 ns	Transmit Data Valid after ETHERTXCLK
			tOHTXEN	ETHERTXCLK/2 + 2.0 ns		Transmit Data Hold after ETHERTXCLK
ETHERRXDV	Input		tISRXDV	10 ns		Receive Data Setup prior to ETHERRXCLK
			tIHRXDV	10 ns		Receive Data Hold prior to ETHERRXCLK
ETHERRX[3:0]	Input		tISRXD	10 ns		Receive Data Setup prior to ETHERRXCLK
			tIHRXD	10 ns		Receive Data Hold prior to ETHERRXCLK

External Memory Controller Waveforms

The External Memory Controller (EMC) handles transactions with both static and dynamic memory.

STATIC MEMORY WAVEFORMS

This section illustrates static memory transaction waveforms. Each wait state is one HCLK period.

nWAIT Input

The EMC's Static Memory Controller supports an nWAIT input that can be used by an external device to extend the wait time during a memory access. The SMC samples nWAIT at the beginning of at the beginning of each system clock cycle. The system clock cycle in which the nCSx signal is asserted counts as the first wait state. See Figure 9 through Figure 18.

Read and Write Waveforms

Figure 15 shows the Read cycle with zero wait states. As shown in the figure, SWAITOENx and SWAITRDx are programmed to 0 for minimum Read cycle time.

The zero programmed into the SWAITRDx indicates that the read occurs with zero wait states, on the first rising edge following Address Valid. After a small propagation delay, nOE is deasserted (as is nCSx), latching the data into the SoC. The address line is held valid one more HCLK period ('C' in the figure). Thus, the minimum Read cycle is two HCLK periods.

Figure 16 shows the minimum write cycle time with both SWAITWRx and SWAITWENx programmed to zero. The write access time is determined by the number of wait states programmed in the SWAITWRx register.

In Figure 16, nCSx is asserted coincident (following a small propagation delay) with Valid Address. Data becomes valid another small propagation delay later. Unlike Read transactions, nWE (or nBLEx) assertion is always delayed one HCLK cycle. The nBLEx signal has the same timing as nWE for write to 8-bit devices that use the byte lane enables instead of the write enables.

The nWE (or nBLEx) signal remains asserted for one HCLK cycle when the nWE (or nBLEx) signal is deasserted and the data is latched into the external memory device. Valid address is held for one additional cycle before deassertion ('C' in the figure), as is the Chip Select. The minimum Write cycle is three HCLK periods.

Read wait state programming uses the SWAITRDx register. Figure 17 shows the results of programming SWAITRDx to 0x3, setting the EMC for three wait states. The deassertion of nOE is delayed from the first rising HCLK edge following Valid Address, as in Figure 15, to the fourth rising edge, a delay of 3 HCLK periods.

Figure 18 shows the results of programming the SWAITWRx and SWAITWENx registers for two Write wait states: register SWAITWENx = 0x0, and SWAITWRx = 0x2. Assertion of nCSx precedes nWE (nBLEx) by one HCLK period. Then, instead of the nWE (nBLEx) signal deasserting one HCLK period after assertion, it is delayed two wait states and the signal deasserts on the rising edge following two wait states.

Chapter 7 of the User's Guide has detailed register descriptions and additional programming examples.

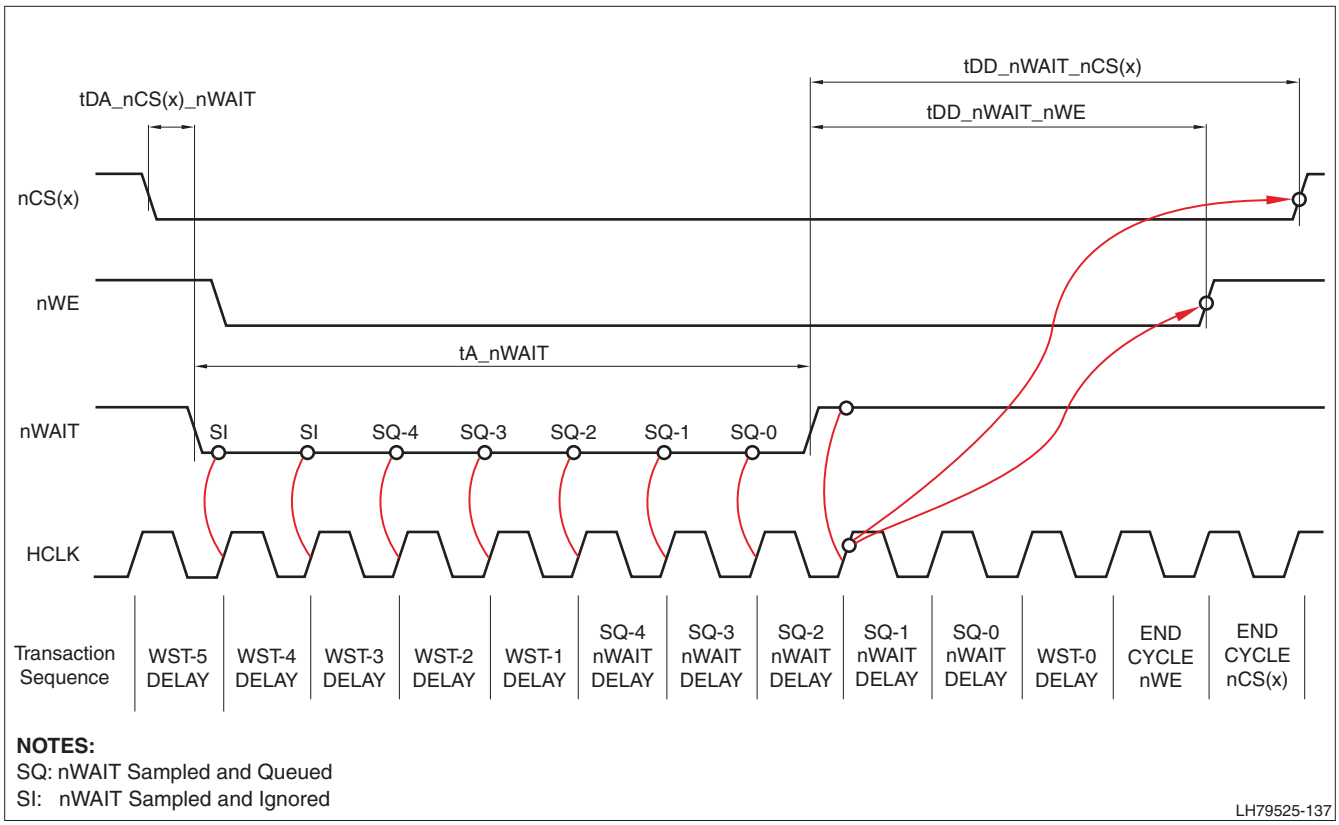


Figure 13. nWAIT Write Sequence (SWAITWRx = 5)

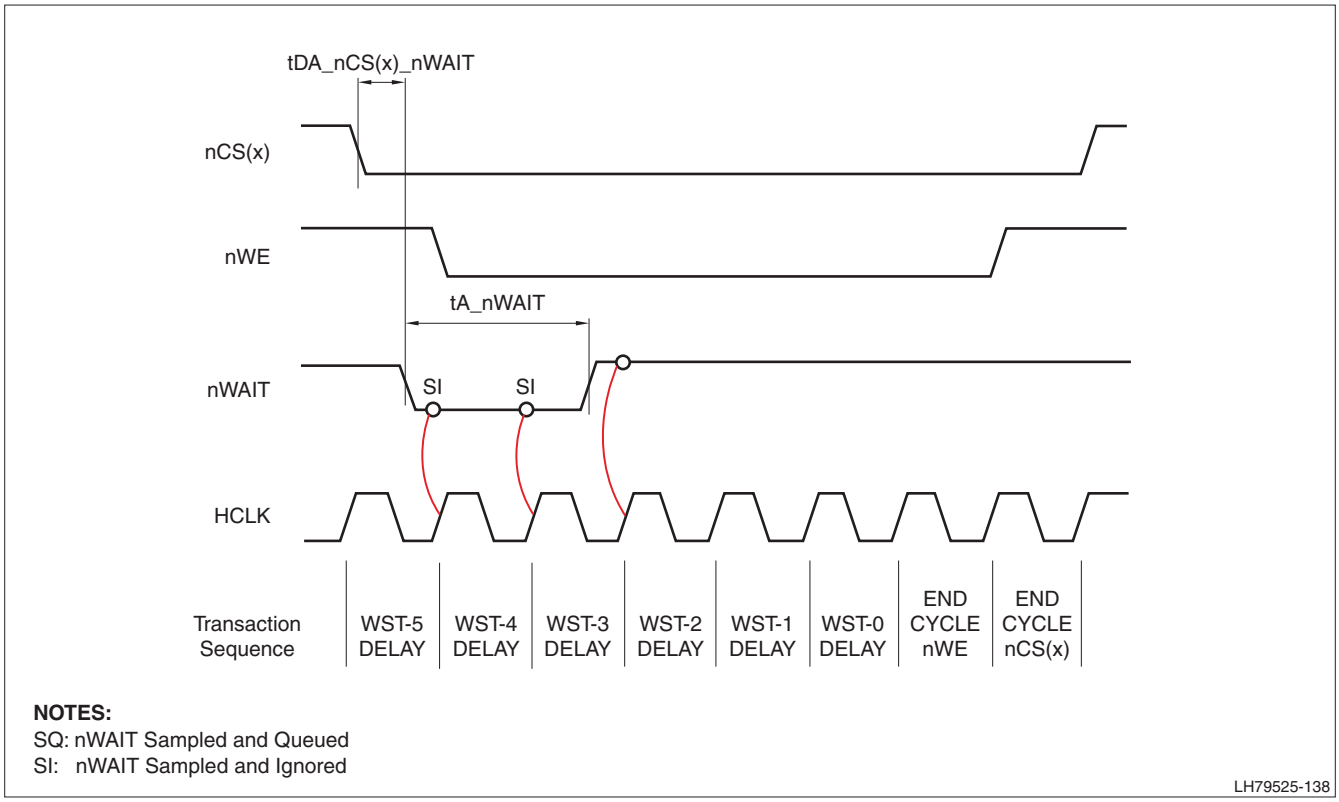


Figure 14. nWAIT Write Sequence (SWAITWRx = 5): nWAIT has no effect on the current transaction

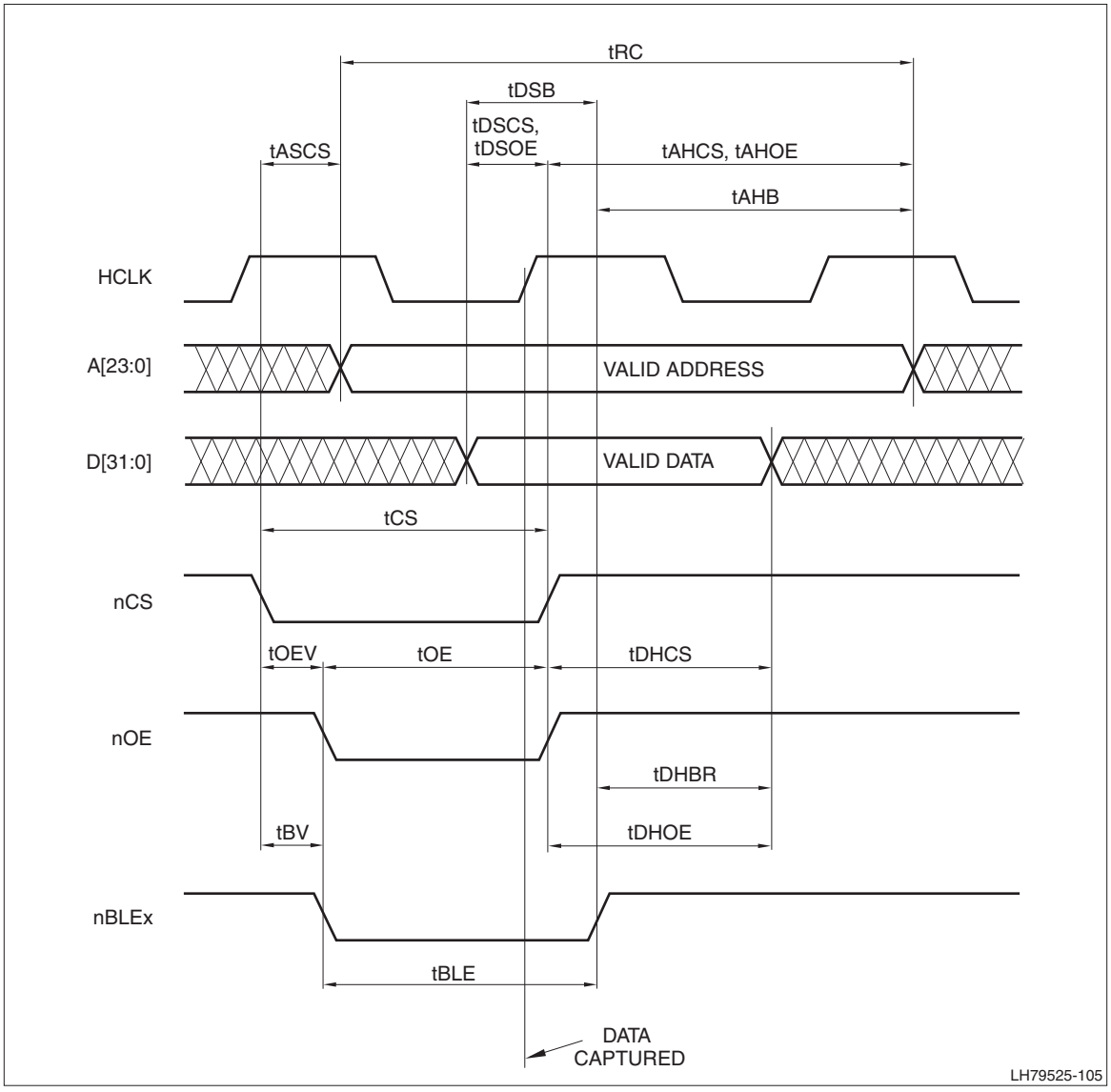


Figure 15. External Static Memory Read, Zero Wait States

Color LCD Controller Timing Diagrams

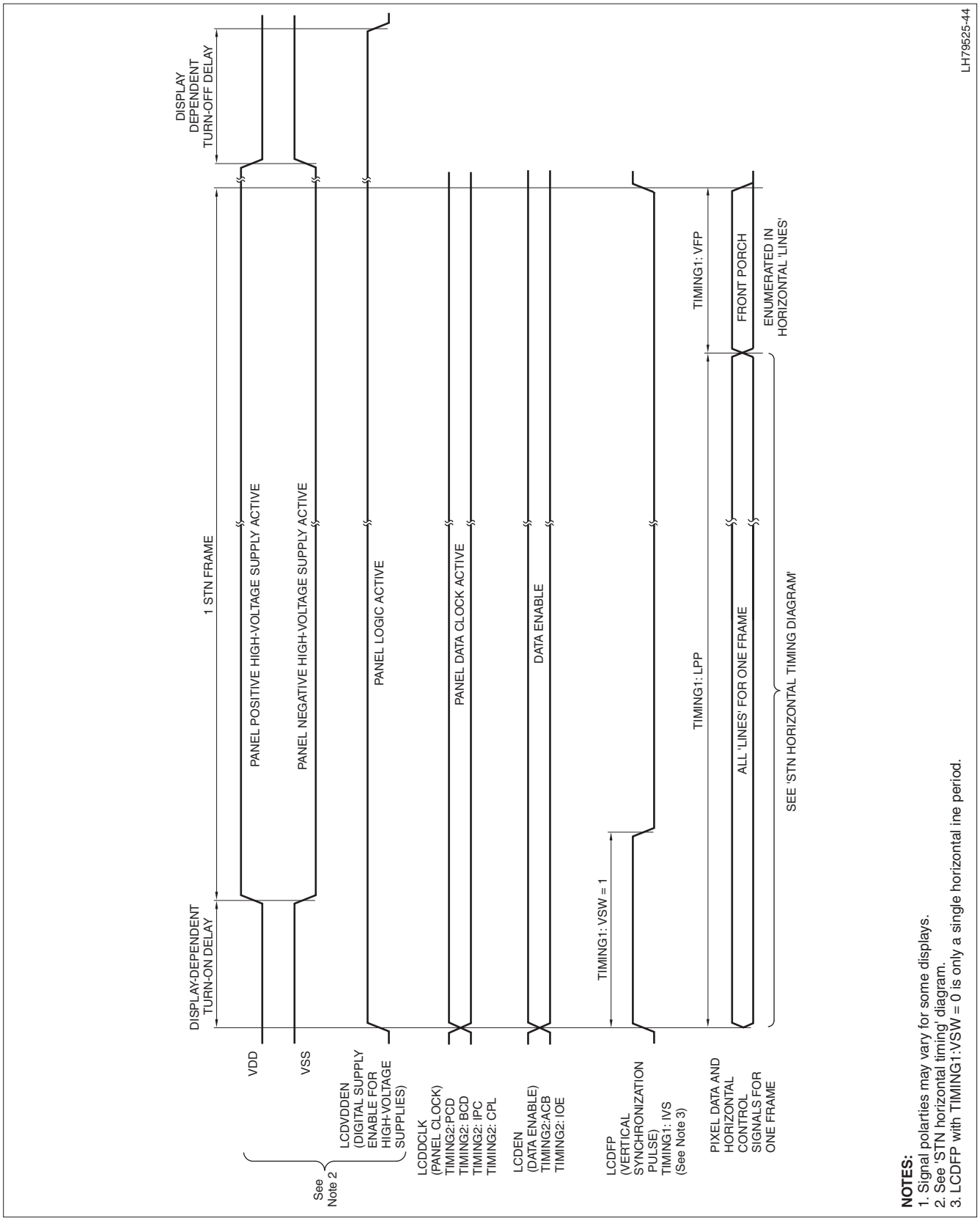


Figure 26. STN Horizontal Timing

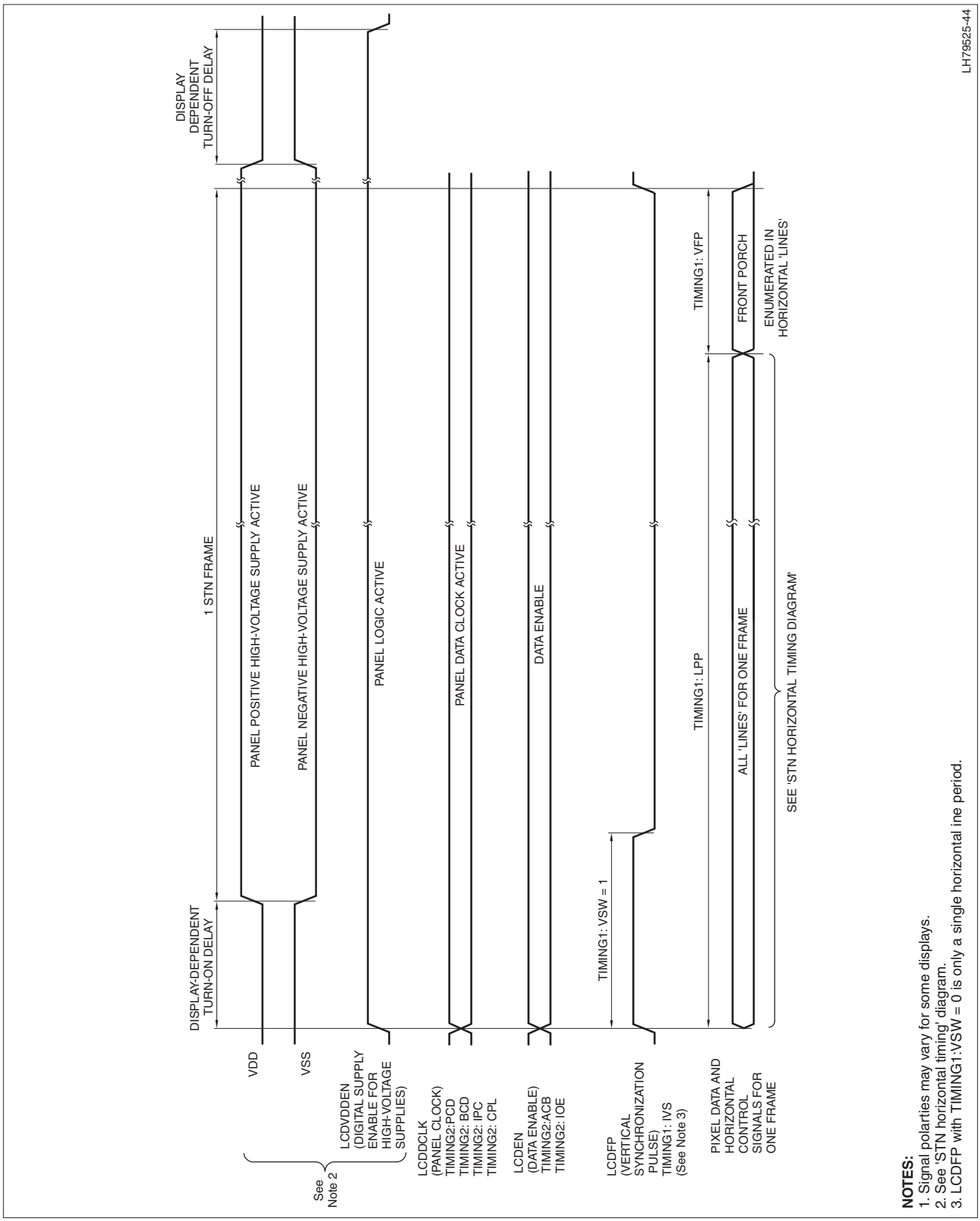


Figure 27. STN Vertical Timing

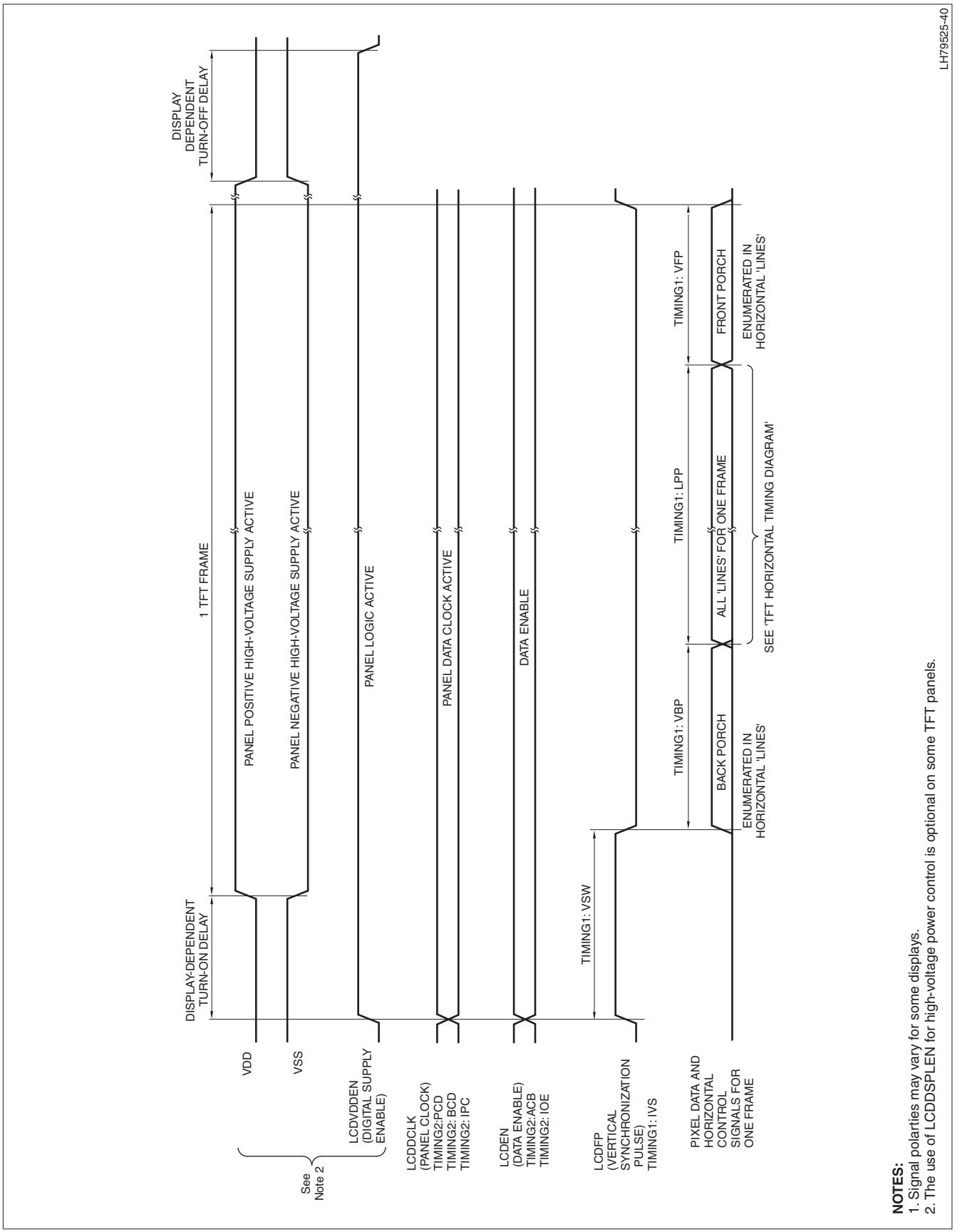


Figure 29. TFT Vertical Timing

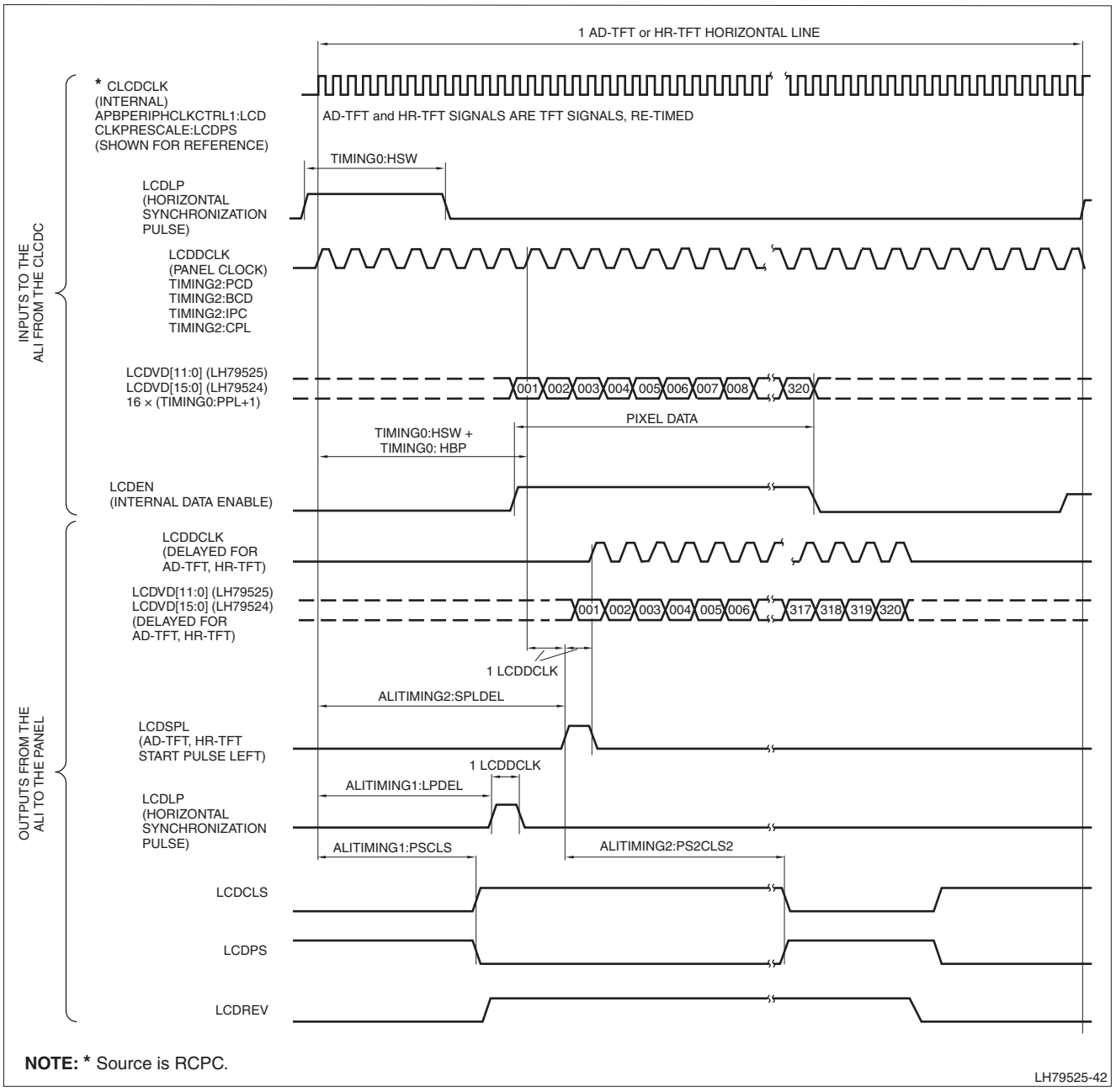


Figure 30. AD-TFT, HR-TFT Horizontal Timing

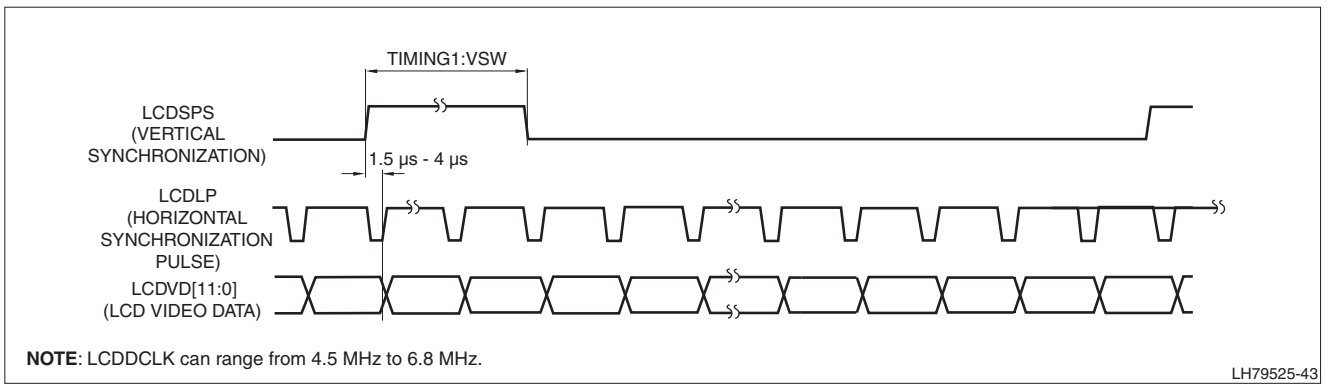


Figure 31. AD-TFT, HR-TFT Vertical Timing

Ethernet MAC Controller Waveforms

The timing for the EMC is presented in the following two illustrations. Figure 33 shows an Ethernet transmit and Figure 34 shows an Ethernet receive.

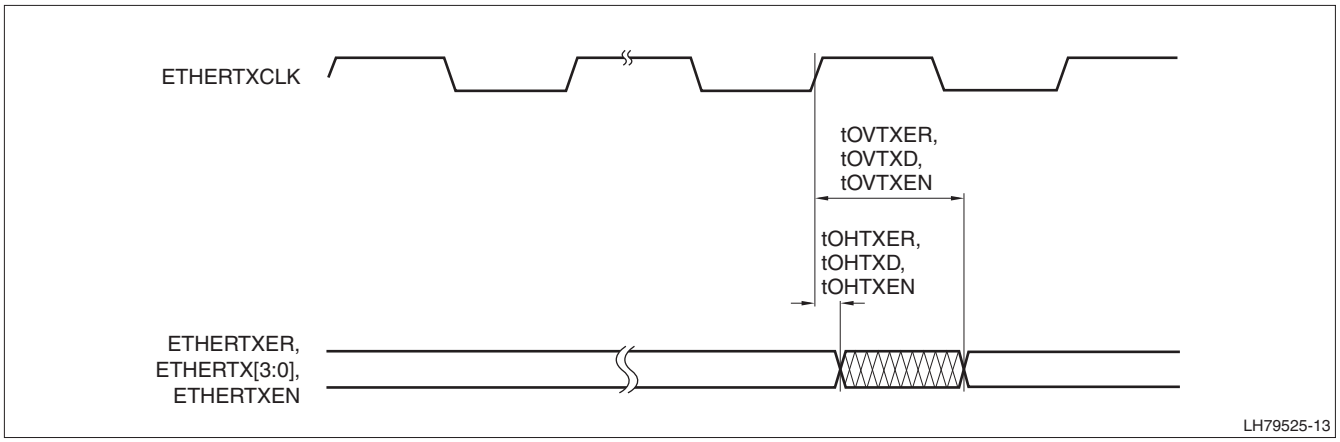


Figure 33. Ethernet Transmit Timing

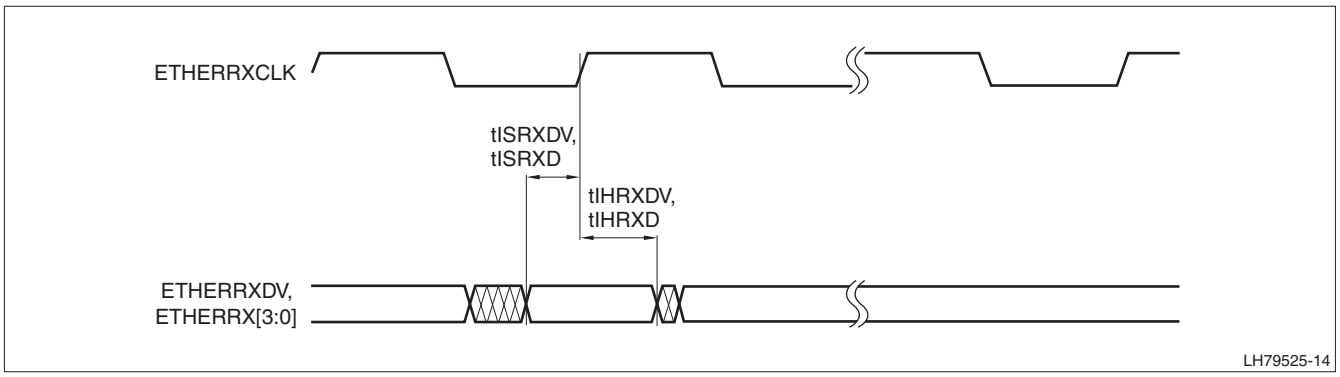
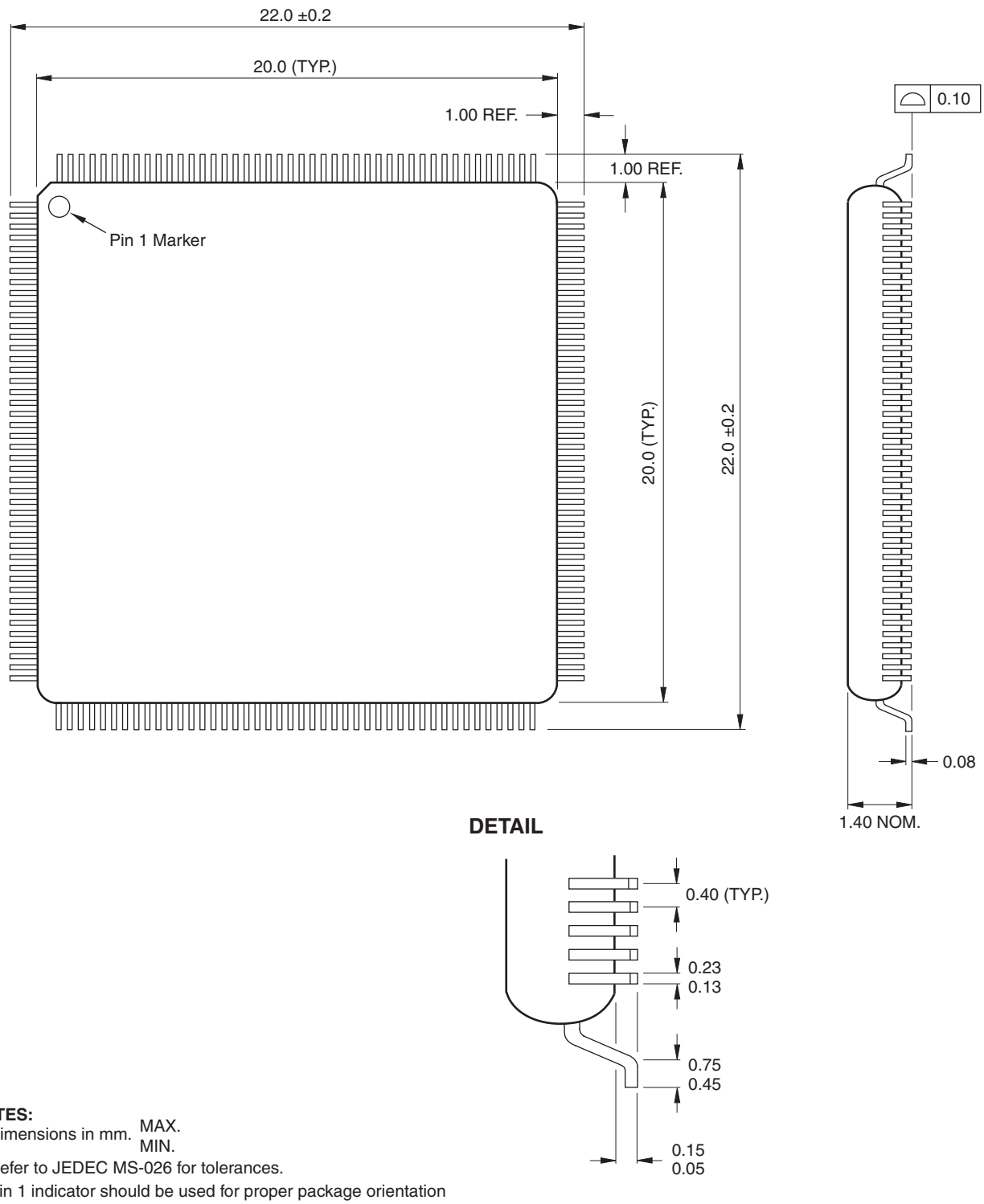


Figure 34. Ethernet Receive Timing

PACKAGE SPECIFICATIONS

176LQFP (JEDEC MS-026)



NOTES:
1. Dimensions in mm. MAX. MIN.
2. Refer to JEDEC MS-026 for tolerances.
3. Pin 1 indicator should be used for proper package orientation (device marking orientation may change with respect to the Pin 1 indicator).

176LQFP-JEDEC

Figure 39. LH79525: 176-pin LQFP

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SHARP®

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SHARP Microelectronics of the Americas
5700 NW Pacific Rim Blvd.
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Phone: (1) 360-834-2500
Fax: (1) 360-834-8903
www.sharpsma.com

EUROPE

SHARP Microelectronics Europe
Division of Sharp Electronics (Europe) GmbH
Sonninstrasse 3
20097 Hamburg, Germany
Phone: (49) 40-2376-2286
Fax: (49) 40-2376-2232
www.sharpsme.com

JAPAN

SHARP Corporation
Electronic Components & Devices
22-22 Nagaike-cho, Abeno-Ku
Osaka 545-8522, Japan
Phone: (81) 6-6621-1221
Fax: (81) 6117-725300/6117-725301
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TAIWAN

SHARP Electronic Components
(Taiwan) Corporation
8F-A, No. 16, Sec. 4, Nanking E. Rd.
Taipei, Taiwan, Republic of China
Phone: (886) 2-2577-7341
Fax: (886) 2-2577-7326/2-2577-7328

SINGAPORE

SHARP Electronics (Singapore) PTE., Ltd.
438A, Alexandra Road, #05-01/02
Alexandra Technopark,
Singapore 119967
Phone: (65) 271-3566
Fax: (65) 271-3855

KOREA

SHARP Electronic Components
(Korea) Corporation
RM 501 Geosung B/D, 541
Dohwa-dong, Mapo-ku
Seoul 121-701, Korea
Phone: (82) 2-711-5813 ~ 8
Fax: (82) 2-711-5819

CHINA

SHARP Microelectronics of China
(Shanghai) Co., Ltd.
28 Xin Jin Qiao Road King Tower 16F
Pudong Shanghai, 201206 P.R. China
Phone: (86) 21-5854-7710/21-5834-6056
Fax: (86) 21-5854-4340/21-5834-6057
Head Office:
No. 360, Bashen Road,
Xin Development Bldg. 22
Waigaoqiao Free Trade Zone Shanghai
200131 P.R. China
Email: smc@china.global.sharp.co.jp

HONG KONG

SHARP-ROXY (Hong Kong) Ltd.
3rd Business Division,
17/F, Admiralty Centre, Tower 1
18 Harcourt Road, Hong Kong
Phone: (852) 28229311
Fax: (852) 28660779
www.sharp.com.hk
Shenzhen Representative Office:
Room 13B1, Tower C,
Electronics Science & Technology Building
Shen Nan Zhong Road
Shenzhen, P.R. China
Phone: (86) 755-3273731
Fax: (86) 755-3273735