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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM7®
Core Size	32-Bit Single-Core
Speed	77.4MHz
Connectivity	EBI/EMI, Ethernet, I²C, SSP, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	72
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/socle/lh79525n0q100a0

Table 1. LH79524 Pin Descriptions (Cont'd)

CABGA PIN	SIGNAL NAME	TYPE	DESCRIPTION
P11	PN3/D25	I/O	General Purpose I/O Signals — Port N3; multiplexed with Data bit D25
J2	nRESETIN	I	Reset Input
H1	nRESETOUT	O	Reset Output
C16	XTALIN	I	Crystal Input
C15	XTALOUT	O	Crystal Output
D16	XTAL32IN	I	32.768 kHz Crystal Oscillator Input
D15	XTAL32OUT	O	32.768 kHz Crystal Oscillator Output
K1	CLKOUT	O	Clock Out (selectable from the internal bus clock or 32.768 kHz crystal)
D2	nTRST	I	JTAG Test Reset Input
P4	TMS	I	JTAG Test Mode Select Input
T3	TCK	I	JTAG Test Clock Input
T1	TDI	I	JTAG Test Serial Data Input
P3	TDO	O	JTAG Test Data Serial Output
T2	TEST1	I	Tie HIGH for Normal Operation; pull LOW to enable Embedded ICE Debugging
R3	TEST2	I	Tie HIGH for Normal Operation; pull HIGH to enable Embedded ICE Debugging
E3	LINREGEN	I	Linear Regulator Enable
D5, E4, E5, H13, N5	VDDC	Power	Core Power Supply
D10, F4, J13, N4	VSSC	Ground	Core GND
D7, D8, D9, F13, G4, G13, H4, J4, K4, K13, L4, N6, N8, N9, N10	VDD	Power	Input/Output Power Supply
E12, G8, G9, H7, H8, H9, H10, J7, J8, J9, J10, K8, K9, M5	VSS	Ground	Input/Output GND
D1	VDDA0	Power	Analog Power Supply for Analog-to-Digital Converter
F16	VDDA1	Power	Analog Power Supply for the USB PLL
E16	VDDA2	Power	Analog Power Supply for System PLL
J1	VSSA0	Ground	Analog GND for Analog-to-Digital Converter
F15	VSSA1	Ground	Analog GND for the USB PLL
E15	VSSA2	Ground	Analog GND for System PLL

Table 4. LH79525 Pin Descriptions (Cont'd)

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION
53	PC6/A22/nFWE	I/O	General Purpose I/O Signal — Port C6; multiplexed with Address A22 and NAND Flash Write Enable
52	PC7/A23/nFRE	I/O	General Purpose I/O Signal — Port C7; multiplexed with Address A23 and NAND Flash Read Enable
90	PD0/D8	I/O	General Purpose I/O Signal — Port D0; multiplexed with Data D8
89	PD1/D9	I/O	General Purpose I/O Signal — Port D1; multiplexed with Data D9
88	PD2/D10	I/O	General Purpose I/O Signal — Port D2; multiplexed with Data D10
87	PD3/D11	I/O	General Purpose I/O Signal — Port D3; multiplexed with Data D11
85	PD4/D12	I/O	General Purpose I/O Signal — Port D4; multiplexed with Data D12
84	PD5/D13	I/O	General Purpose I/O Signal — Port D5; multiplexed with Data D13
83	PD6/D14	I/O	General Purpose I/O Signal — Port D6; multiplexed with Data D14
82	PD7/D15	I/O	General Purpose I/O Signal — Port D7; multiplexed with Data D15
141	PE0/LCDLP/ LCDHRLP	I/O	General Purpose I/O Signals — Port E0; multiplexed with LCD Line Pulse and AD-TFT/HR-TFT Line Pulse
139	PE1/LCDDCLK	I/O	General Purpose I/O Signals — Port E1; multiplexed with LCD Data Clock
138	PE2/LCDPS	I/O	General Purpose I/O Signals — Port E2; multiplexed with LCD Power Save
137	PE3/LCDCLS	I/O	General Purpose I/O Signals — Port E3; multiplexed with LCD Row Driver Clock
136	PE4/LCDDSPLEN/ LCDREV	I/O	General Purpose I/O Signals — Port E4; multiplexed with LCD Panel Power Enable and LCD Reverse
134	PE5/LCDVDDEN	I/O	General Purpose I/O Signals — Port E5; multiplexed with LCD VDD Enable
133	PE6LCDVEEN/ LCDMOD	I/O	General Purpose I/O Signals — Port E6; multiplexed with LCD Analog Power Enable and MOD
120	PE7/nWAIT/nDEOT	I/O	General Purpose I/O Signals — Port E7; multiplexed with nWAIT and DMA End of Transfer
153	PF0/LCDVD6	I/O	General Purpose I/O Signals — Port F0; multiplexed with LCD Video Data bit 6
151	PF1/LCDVD7	I/O	General Purpose I/O Signals — Port F1; multiplexed with LCD Video Data bit 7
149	PF2/LCDVD8	I/O	General Purpose I/O Signals — Port F2; multiplexed with LCD Video Data bit 8
147	PF3/LCDVD9	I/O	General Purpose I/O Signals — Port F3; multiplexed with LCD Video Data bit 9
146	PF4/LCDVD10	I/O	General Purpose I/O Signals — Port F4; multiplexed with LCD Video Data bit 10
145	PF5/LCDVD11	I/O	General Purpose I/O Signals — Port F5; multiplexed with LCD Video Data bit 11
143	PF6/LCDEN/ LCDSPL	I/O	General Purpose I/O Signals — Port F6; multiplexed with LCD Start Pulse Left
142	PF7/LCDFP/ LCDSPS	I/O	General Purpose I/O Signals — Port F7; multiplexed with LCD Row Driver Counter reset
162	PG0/ETHERTXEN	I/O	General Purpose I/O Signals — Port G0; multiplexed with Ethernet Transmit Enable
161	PG1/ETHERTXCLK	I/O	General Purpose I/O Signals — Port G1; multiplexed with Ethernet Clock
159	PG2/LCDVD0	I/O	General Purpose I/O Signals — Port G2; multiplexed with LCD Video Data bit 0
158	PG3/LCDVD1	I/O	General Purpose I/O Signals — Port G3; multiplexed with LCD Video Data bit 1
157	PG4/LCDVD2	I/O	General Purpose I/O Signals — Port G4; multiplexed with LCD Video Data bit 2
156	PG5/LCDVD3	I/O	General Purpose I/O Signals — Port G5; multiplexed with LCD Video Data bit 3
155	PG6/LCDVD4	I/O	General Purpose I/O Signals — Port G6; multiplexed with LCD Video Data bit 4
154	PG7/LCDVD5	I/O	General Purpose I/O Signals — Port G7; multiplexed with LCD Video Data bit 5
171	PH0/ETHERRX3	I/O	General Purpose I/O Signals — Port H0; multiplexed with Ethernet Receive Channel 3
170	PH1/ETHERRXDV	I/O	General Purpose I/O Signals — Port H1; multiplexed with Ethernet Data Valid
169	PH2/ETHERRXCLK	I/O	General Purpose I/O Signals — Port H2; multiplexed with Ethernet Receive Clock
167	PH3/ETHERTXER	I/O	General Purpose I/O Signals — Port H3; multiplexed with Ethernet Transmit Error
166	PH4/ETHERTX0	I/O	General Purpose I/O Signals — Port H4; multiplexed with Ethernet Transmit Channel 0
165	PH5/ETHERTX1	I/O	General Purpose I/O Signals — Port H5; multiplexed with Ethernet Transmit Channel 1

Table 5. LH79525 Numerical Pin List

PIN NO.	FUNCTION AT RESET	MULTIPLEXED FUNCTION(S)	OUTPUT DRIVE	NOTES
1	PI2	ETHERCOL	8 mA	1
2	PI1	ETHERMDIO	8 mA	2
3	VDD			
4	PI0	ETHERMDC	8 mA	1
5	VSS			
6	VDDC			
7	VSSC			
8	nTRST			2, 3
9	LINREGEN			
10	VDDA0			
11	AN0/UL/X+			
12	AN6	PJ7/INT7		
13	AN7	PJ6/INT6		
14	AN1/UR/X-			
15	AN5	PJ5/INT5		
16	AN8	PJ4		
17	AN2/LL/Y+	PJ3		
18	AN9	PJ2		
19	AN4/WIPER	PJ1		
20	AN3/LR/Y-	PJ0		
21	VSSA0			
22	nRESETOUT		8 mA	
23	CLKOUT		8 mA	
24	nRESETIN			2, 3
25	CTCLK	INT4/BATCNTL	8 mA	2, 3
26	VDD			
27	VSS			
28	PA7	CTCAP2B/CTCMP2B/ SCL	8 mA	2, 3
29	PA6	CTCAP2A/CTCMP2A/ SDA	8 mA	2, 3
30	PA5	CTCAP1B/CTCMP1B	8 mA	1, 3
31	PA4	CTCAP1A/CTCMP1A	8 mA	1, 3
32	PA3	CTCAP0B/CTCMP0B	8 mA	1, 3
33	VDD			
34	PA2	CTCAP0A/CTCMP0A	8 mA	1, 3
35	PA1	INT3/UARTTX2/ UARTIRTX2	8 mA	1, 3
36	PA0	INT2/UARTRX2/ UARTIRRX2	8 mA	1, 3
37	PB7	INT1/UARTTX0/ UARTIRTX0	8 mA	1, 3
38	PB6	INT0/UARTRX0/ UARTIRRX0	8 mA	1, 3
39	PB5	SSPTX/I2STXD/ UARTTX1/UARTIRTX1	8 mA	1
40	PB4	SSPRX/I2SRXD/ UARTRX1/UARTIRRX1	8 mA	2
41	PB3	SSPCLK/I2SCLK	8 mA	1
42	PB2	SSPFRM/I2SWS	8 mA	2
43	PB1	DREQ/nUARTRTS0	8 mA	2
44	PB0	nDACK/nUARTCTS0	8 mA	2
45	TDO		4 mA	

Table 5. LH79525 Numerical Pin List (Cont'd)

PIN NO.	FUNCTION AT RESET	MULTIPLEXED FUNCTION(S)	OUTPUT DRIVE	NOTES
46	TDI			2, 3
47	TEST1			2, 3
48	TEST2			2, 3
49	VSS			
50	TMS			2, 3
51	TCK			2, 3
52	PC7	A23/nFRE	8 mA	1
53	PC6	A22/nFWE	8 mA	1
54	PC5	A21	8 mA	1
55	PC4	A20	8 mA	1
56	PC3	A19	8 mA	1
57	VDD			
58	PC2	A18	8 mA	1
59	PC1	A17	8 mA	1
60	PC0	A16	8 mA	1
61	A15		8 mA	
62	A14		8 mA	
63	A13		8 mA	
64	VSSC			
65	A12		8 mA	
66	VDDC			
67	A11		8 mA	
68	VSS			
69	A10		8 mA	
70	A9		8 mA	
71	A8		8 mA	
72	A7		8 mA	
73	A6		8 mA	
74	A5		8 mA	
75	VDD			
76	A4		8 mA	
77	A3		8 mA	
78	A2		8 mA	
79	A1		8 mA	
80	A0		8 mA	
81	VSS			
82	PD7	D15	8 mA	1
83	PD6	D14	8 mA	1
84	PD5	D13	8 mA	1
85	PD4	D12	8 mA	1
86	VDD			
87	PD3	D11	8 mA	1
88	PD2	D10	8 mA	1
89	PD1	D9	8 mA	1
90	PD0	D8	8 mA	1
91	D7		8 mA	1
92	VSS			
93	D6		8 mA	1
94	D5		8 mA	1
95	D4		8 mA	1
96	D3		8 mA	1

External Memory Controller

An integrated External Memory Controller (EMC) provides a glueless interface to external SDRAM, Low Power SDRAM, Flash, SRAM, ROM, and burst ROM. Three remap options for the physical memory are selectable by software, as shown in Figure 3 through Figure 6.

The EMC supports six banks of external memory. Two chip selects for synchronous memory, and either two (LH79525) or four (LH79524) static memory chip selects are available. The static interface also includes two (LH79525) or four (LH79524) byte lane enable signals.

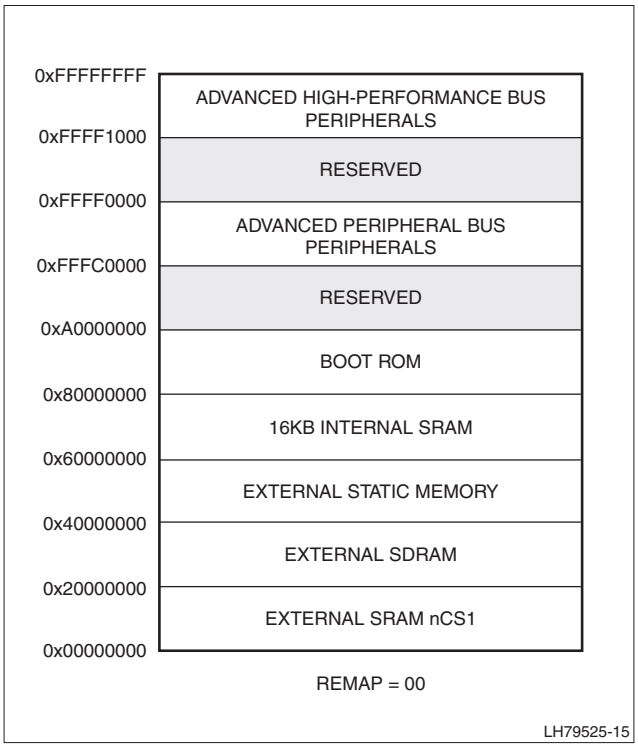


Figure 3. Memory Remap '00'

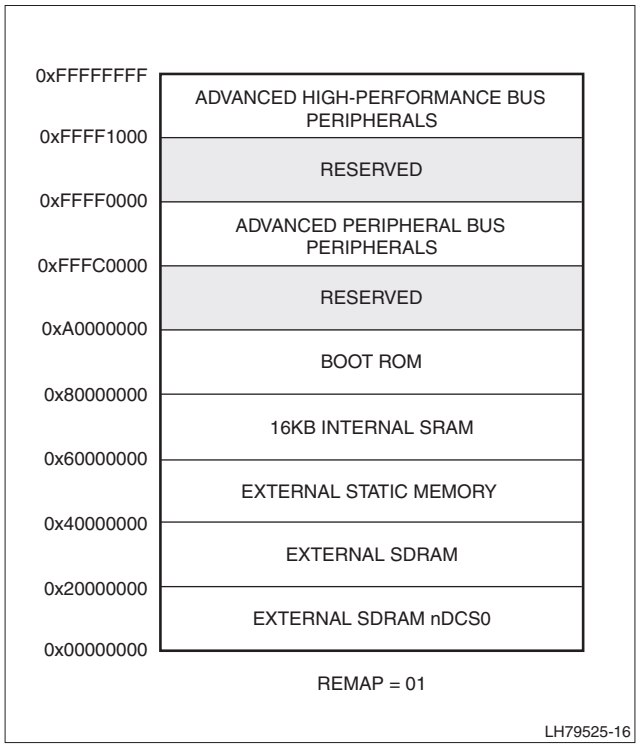


Figure 4. Memory Remap '01'

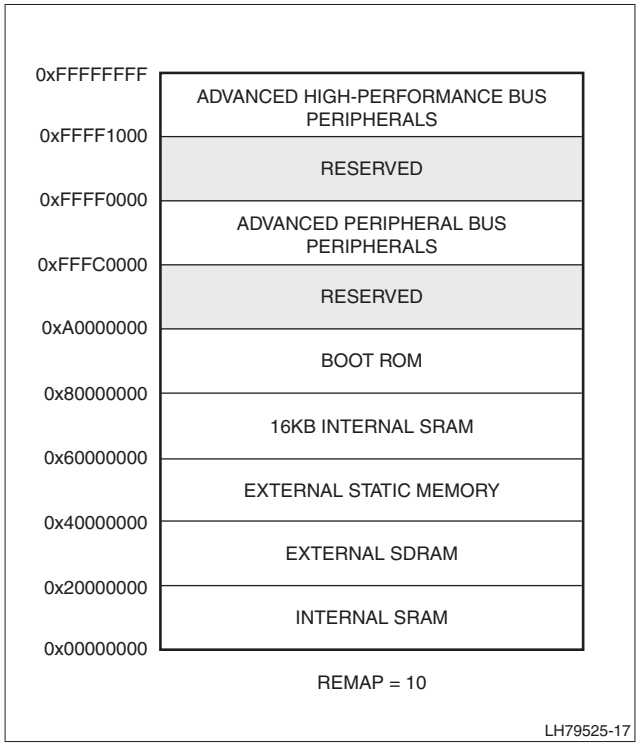


Figure 5. Memory Remap '10'

Universal Asynchronous Receiver Transmitter (UART)

The LH79524/LH79525 incorporates three UARTs. UART0, UART1, and UART2 offer similar functionality to the industry-standard 16C550. They perform serial-to-parallel conversion on data received from a peripheral device and parallel-to-serial conversion on data transmitted to the UART. The CPU reads and writes data and control status information through the AMBA APB interface. The transmit and receive paths are buffered with internal FIFO memories that support programmable-service 'trigger levels', and overrun protection. These FIFO memories enable up to 32 characters to be stored independently in both transmit and receive modes.

- Programmable bits-per-character (5, 6, 7, or 8)
- Optional nine-bit mode to tag and recognize characters as either data or address
- Nine-bit Transmit FIFO and 12-bit Receive FIFO
- Programmable FIFO trigger points
- DMA support for UART0
- Programmable IrDA SIR input/output for each UART
- Separate 16-byte transmit and receive FIFOs to reduce CPU interrupts
- Programmable FIFO disabling for 1-byte depth
- Programmable baud rate generator
- Independent masking of transmit FIFO, receive FIFO, receive timeout and modem status interrupts
- False start bit detection
- Line break generation and detection
- Fully-programmable serial interface characteristics:
  - 5-, 6-, 7-, or 8-bit data word length
  - Even-, odd-, or no-parity bit generation and detection
  - 1 or 2 stop bit generation
- IrDA SIR Encode/Decode block, providing:
  - Programmable use of IrDA SIR or UART input/output
  - Supports data rates up to 115.2 kbit/s half-duplex
  - Programmable internal clock generator, allowing division of the Reference clock in increments of 1 to 512 for low-power mode bit durations.
  - Loopback for testing

Vectored Interrupt Controller (VIC)

The Vectored Interrupt Controller combines the interrupt request signals from 20 internal and eight external interrupt sources and applies them, after masking and prioritization, to the IRQ and FIQ interrupt inputs of the ARM7TDMI processor core.

The Interrupt Controller incorporates a hardware interrupt vector logic with programmable priority for up to 16 interrupt sources. This logic reduces the interrupt response time for IRQ type interrupts compared to solutions using software polling to determine the highest priority interrupt source. This significantly improves the real-time capabilities of the LH79524/LH79525 in embedded control applications.

- 20 internal and eight external interrupt sources
  - Individually maskable
  - Status accessible for software polling
- IRQ interrupt vector logic for up to 16 channels with programmable priorities
- All of the interrupt channels, with the exception of the Watchdog Timer interrupt, can be programmed to generate:
  - FIQ interrupt request
  - Non-vectored IRQ interrupt request (software to poll IRQ source)
  - Vectored IRQ interrupt request (up to 16 channels total)
- The Watchdog timer can only generate FIQ interrupt requests
- External interrupt inputs programmable
  - Edge triggered or level triggered
  - Rising edge/active HIGH or falling edge/active LOW

The 32 interrupt channels are shown in Table 9.

Table 9. Interrupt Channels

CHANNEL	INTERRUPT SOURCE
0	WDT
1	Not Used
2	COMRX (used for debug)
3	COMTX (used for debug)
4	Counter/Timer0 Combined
5	Counter/Timer1 Combined
6	Counter/Timer2 Combined
7	External Interrupt 0
8	External Interrupt 1
9	External Interrupt 2
10	External Interrupt 3
11	External Interrupt 4
12	External Interrupt 5
13	External Interrupt 6
14	External Interrupt 7
15	RTC_ALARM
16	ACD TSIRQ Combined
17	ADC Brown Out INTR

Table 9. Interrupt Channels (Cont'd)

CHANNEL	INTERRUPT SOURCE
18	ADC Pen IRQ
19	CLCD Combined Interrupt
20	DMA Stream 0
21	DMA Stream 1
22	DMA Stream 2
23	DMA Stream 3
24	SSP I^2S Interrupt
25	Ethernet Interrupt
26	USB Interrupt
27	UART 0 Interrupt
28	UART 1 Interrupt
29	UART 2 Interrupt
30	USB DMA Interrupt
31	I^2C Interrupt

Reset, Clock, and Power Controller (RCPC)

The RCPC generates the various clock signals for the operation of the LH79524/LH79525 and provides for an orderly start-up after power-on and during a wake-up from one of the power saving operating modes. The RCPC allows the software to individually select the frequency of the various on-chip clock signals as required to operate the chip in the most power-efficient mode. The maximum speeds of the various clocks in the SoC are shown in Table 10. More detailed descriptions of each clock appear in the User's Guide.

The RCPC features:

- 10 - 20 MHz crystal oscillator and PLL for on-chip Clock generation (11.2896 MHz recommended)
- External Clock input if on-chip oscillator and PLL are not used
- 32.768 kHz crystal oscillator generating 1 Hz clock for Real Time Clock
- Individually controlled clocks for peripherals and CPU
- Programmable clock prescalers for UARTs and PWMs
- Five global power control modes are available:
  - Active
  - Standby
  - Sleep
  - Stop1
  - Stop2
- CPU/Bus clock frequency can be changed on the fly
- Selectable clock output
- Hardware reset (nRESETIN) and software reset.

Table 10. Maximum Clock Speeds

NAME	FREQUENCY (MAX.)
Oscillator Clock (CLK OSC)	20.0 MHz
PLL System Clock (CLK PLL)	304.819 MHz
PLL USB Clock	48.0 MHz
32.768 kHz Oscillator Clock	32.768 kHz
AHB Clock (HCLK)	50.803 MHz
AHB Fast CPU Clock (FCLK CPU)	76.205 MHz
Ethernet Clock	50.803 MHz
DMA Clock	50.803 MHz
External Memory Controller Clock	50.803 MHz
SSP Clock	50.803 MHz
CLCD Clock	50.803 MHz
UART[2:0] Clock	20.0 MHz
RTC Clock	1.0 Hz

Table 11. Clock Activity for Different Power Modes

DEVICE	ACTIVE	STANDBY	SLEEP	STOP1	STOP2
RTC 32 kHz Oscillator	ON	ON	ON	ON	ON
10 - 20 MHz Oscillator	ON	ON	ON	ON	OFF
PLL	ON	ON	ON	OFF	OFF
Peripheral Clock	ON	ON	OFF	OFF	OFF
CPU Clock	ON	OFF	OFF	OFF	OFF

Real Time Clock

The RTC provides an alarm or long time base counter. An interrupt is generated following counting a programmed number of one-second periods. The 1 Hz RTC clock is internally derived. The RTC features:

- 32-bit up counter with programmable load
- Programmable 32-bit match compare register
- Software maskable interrupt when counter and compare registers are identical.

RTC input clock sources:

- PLL clock
- 32.768 kHz clock
- 1 Hz clock (default).

Power Supply Sequencing

When the linear regulator is *not* enabled, SHARP recommends that the 1.8 V power supply be energized before the 3.3 V supply. If this is not possible, the 1.8 V supply may not lag the 3.3 V supply by more than 100 µs. If longer delay time is needed, it is recommended that the voltage difference between the two power supplies be within 1.5 V during power supply ramp up. To avoid a potential latchup condition, voltage should be applied to input pins only after the device is powered-on as described above.

DC/AC Specifications

Unless noted, all data provided are based on:

- -40°C to +85°C (Industrial temperature range)
- VDDC = 1.7 V to 1.9 V
- VDD = 3.0 V to 3.6 V, VDDA = 1.7 V to 1.9 V.

DC SPECIFICATIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
VIH	CMOS input HIGH voltage	2.0		5.5	V	CEN = 1
VIL	CMOS input LOW voltage			0.8	V	CEN = 1
VIT+	Positive Input threshold voltage (Schmitt pins)	2.0			V	CSEN = 1
VIT-	Negative Input threshold voltage (Schmitt pins)			0.8	V	CSEN = 1
VHYST	Schmitt trigger hysteresis		0.35		V	CSEN = 1
VOH[1]	Output drive (2 mA type)	2.6			V	IOH = -2 mA
	Output drive (4 mA type)	2.6			V	IOH = -4 mA
	Output drive (8 mA type)	2.6			V	IOH = -8 mA
	Output drive (12 mA type)	2.6			V	IOH = -12 mA
VOL[1]	Output drive (2 mA type)			0.4	V	IOL = 2 mA
	Output drive (4 mA type)			0.4	V	IOL = 4 mA
	Output drive (8 mA type)			0.4	V	IOL = 7 mA
	Output drive (12 mA type)	2.6			V	IOH = 12 mA
RIN	Input leakage pull-up/pull-down resistors		40		kΩ	VIN = VDD or GND (Calculate input leakage current at desired VDD)
IACTIVE	Active current		85		mA	Note 2
ISTANDBY	Standby current		50		mA	Notes 2, 3
ISLEEP	Sleep current		3.8		mA	
ISTOP1	Stop1 current		420		µA	
ISTOP2	Stop2 current		115		µA	RTC ON, Linear Regulator ON
ISTOP2	Stop2 current		95		µA	RTC OFF, Linear Regulator ON
ISTOP2	Stop2 current		45		µA	RTC ON, Linear Regulator OFF
ISTOP2	Stop2 current		25		µA	RTC OFF, Linear Regulator OFF

NOTES:

1. Table 2 details each pin's buffer type.
2. Running Typical Application over operating range.
3. Current measured with CPU stopped and all peripherals enabled

Linear Regulator DC Characteristics.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
IQUIESCENT	Quiescent Current		75		µA
ISLEEPLR	Current with Linear Regulator disabled		8		µA
IOLR	Output Current Range	0.0		200	mA
VOLR	Output Voltage, Linear Regulator		1.84		V

Analog-To-Digital Converter Electrical Characteristics

Table 14 shows the ADC electrical characteristics. See Figure 8 for the ADC transfer characteristics.

Table 14. ADC Electrical Characteristics

PARAMETER	MIN.	TYP.	MAX.	UNITS	NOTES
A/D Resolution	10		10	Bits	
Throughput Conversion	17			CLK Cycles	1
Acquisition Time	3			CLK Cycles	
Data Format		binary			
CLK Frequency	500		5,000	ns	
Differential Non-Linearity	-0.99		3.0	LSB	
Integral Non-Linearity	-3.0		+3.0	LSB	
Offset Error	-10		+10	mV	
Gain Error	-2.0		+2.0	LSB	
Reference Voltage Output	1.85	2.0	2.15	V	
VREF-	VSSA	VSSA	(VREF+) -1.0 V	V	2
VREF+	(VREF-) +1.0 V	VREF	VDDA	V	2
Crosstalk between channels		-60		dB	
Analog Input Voltage Range	0		VDDA	V	3
Analog Input Current			5	µA	
Reference Input Current			5	µA	
Analog input capacitance			15	pF	
Operating Supply Voltage	3.0		3.6	V	
Operating Current, VDDA0		590	1000	µA	
Powerdown Current, VDDA0		1	10	µA	
Standby Current		180	300	µA	4
Brown Out Trip Point (falling point)	2.36	2.63	2.9	V	
Brown Out Hysterisis		120		mV	
Operating Temperature	-40		85	°C	

NOTES:

1. The analog section of the ADC takes 16 × A2DCLK cycles per conversion plus 1 × A2DCLK cycles to be made available in the PCLK domain. An additional 3 × PCLK cycles are required before being available on the APB.
2. The internal voltage reference is driven to nominal value VREF = 2.0 V. Using the Reference Multiplexer, alternative low impedance (RS < 500) voltages can be selected as reference voltages. The range of voltages allowed are specified above. However, the on-chip reference cannot drive the ADC unless the reference buffer is switched on.
3. The analog input pins can be driven anywhere between the power supply rails. If the voltage at the input to the ADC exceeds VREF+ or is below VREF-, the A/D result will saturate appropriately at positive or negative full scale. Trying to pull the analog input pins above or below the power supply rails will cause protection diodes to be forward-biased, resulting in large current source/sink and possible damage to the ADC.
4. Bandgap and other low-bandwidth circuitry operating. All other ADC blocks shut down.

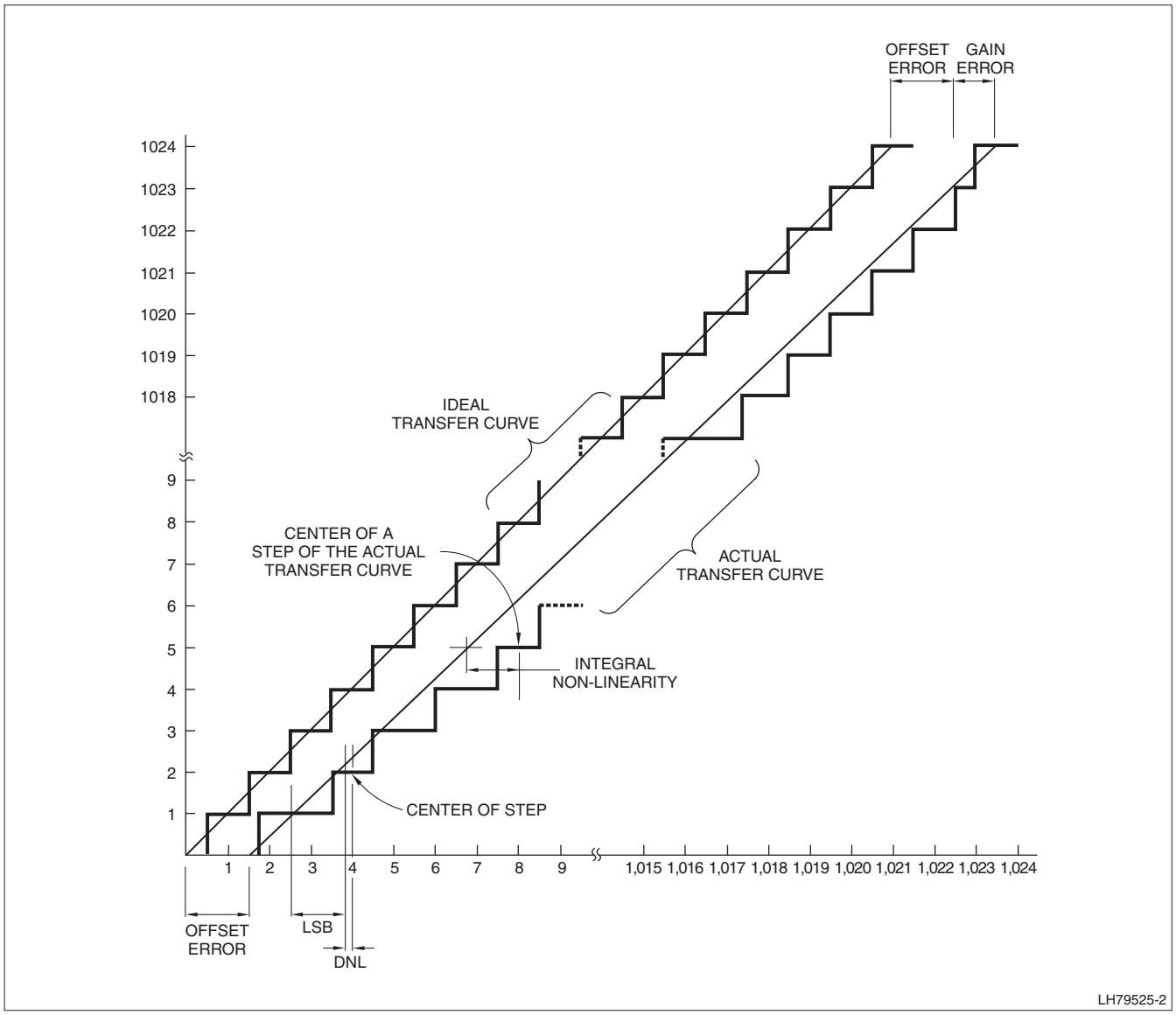


Figure 8. ADC Transfer Characteristics

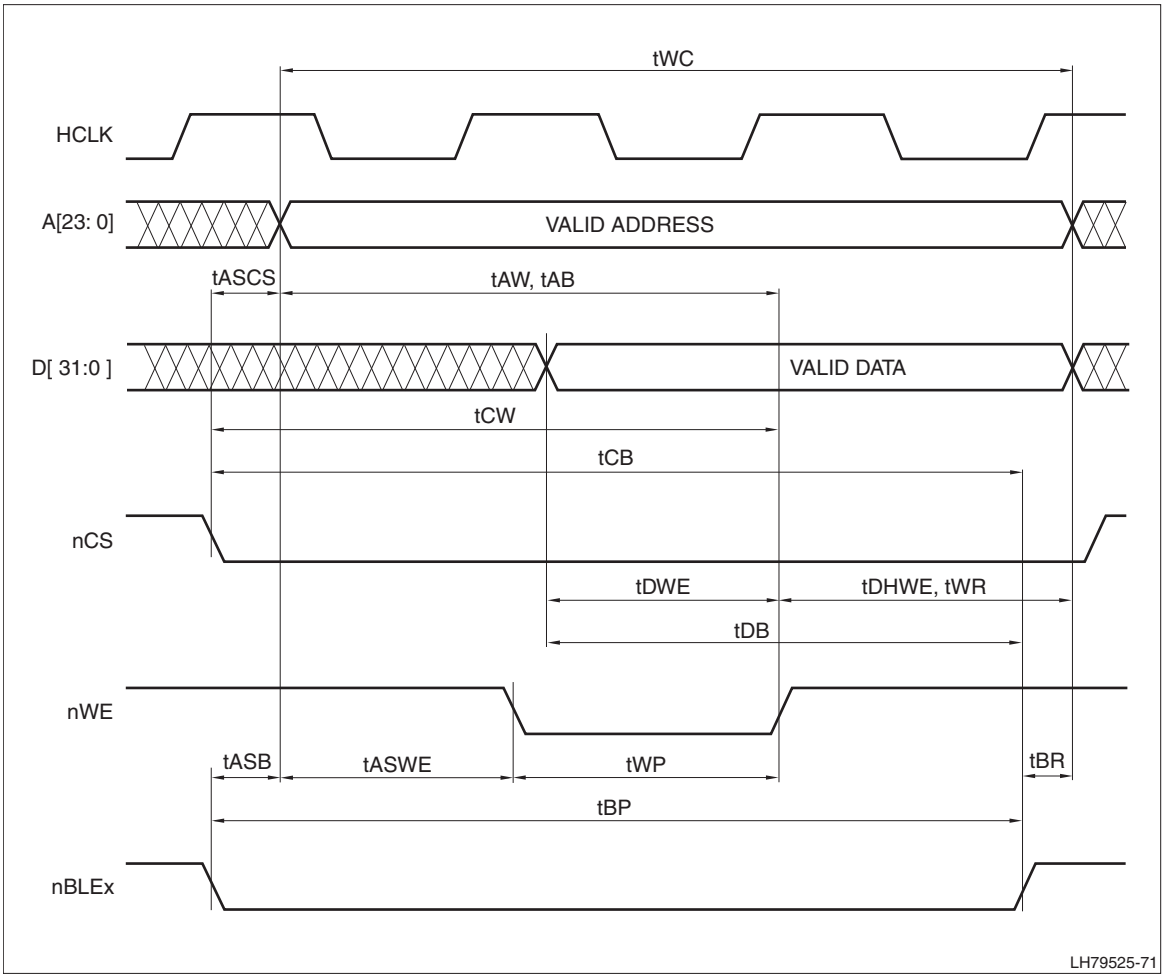


Figure 16. External Static Memory Write, Zero Wait States

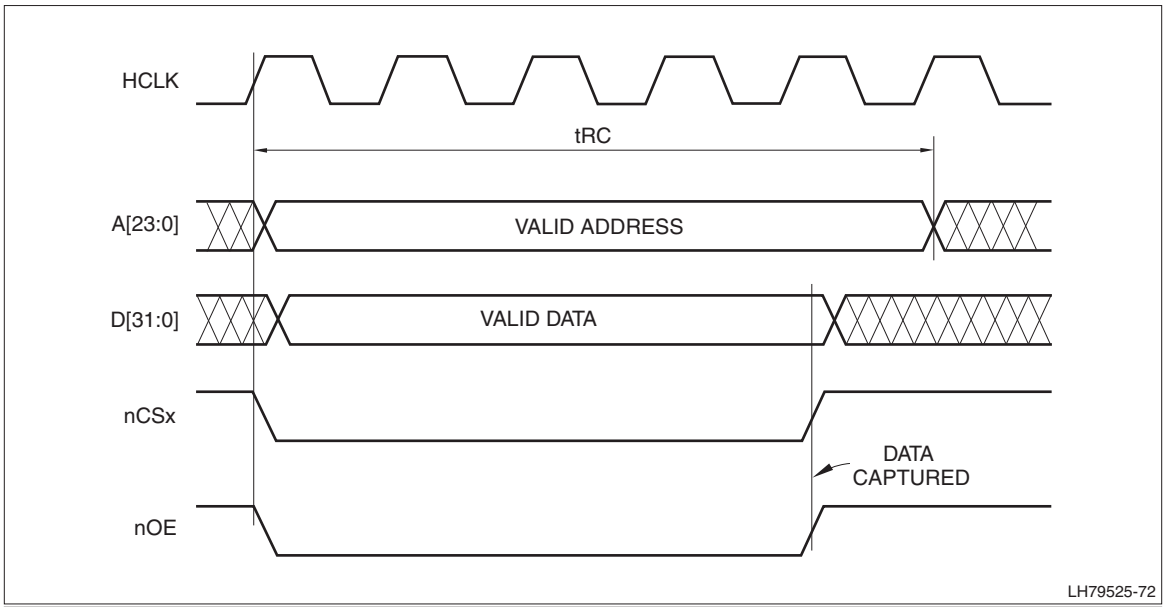


Figure 17. External Static Memory Read with Three Wait States

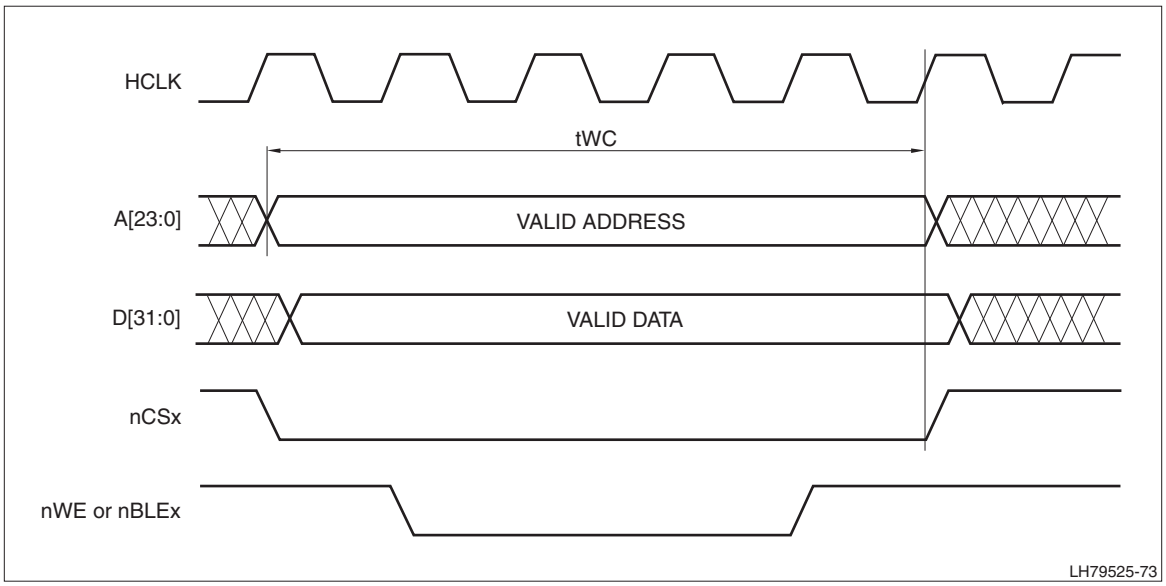


Figure 18. External Static Memory Write with Two Wait States

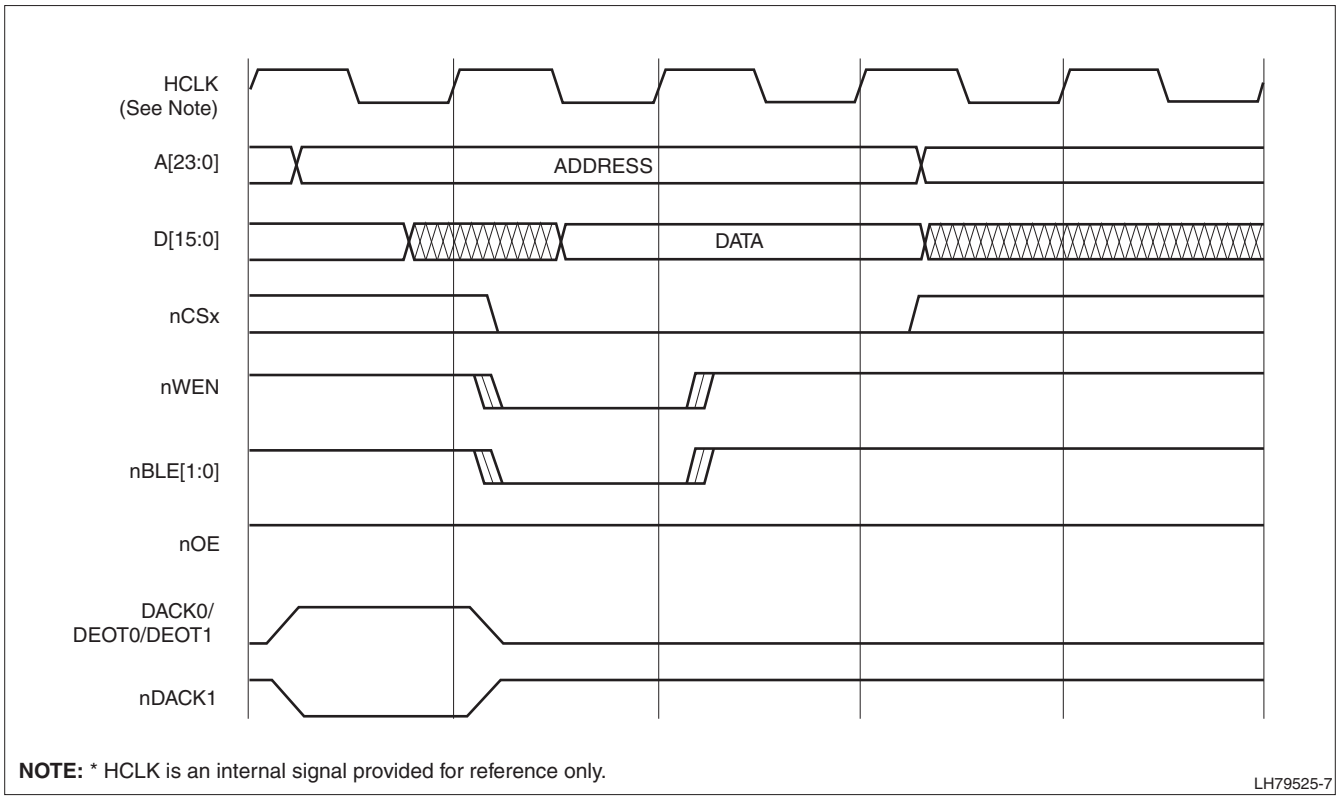


Figure 23. Write, from Memory to Peripheral, Burst Size = 1

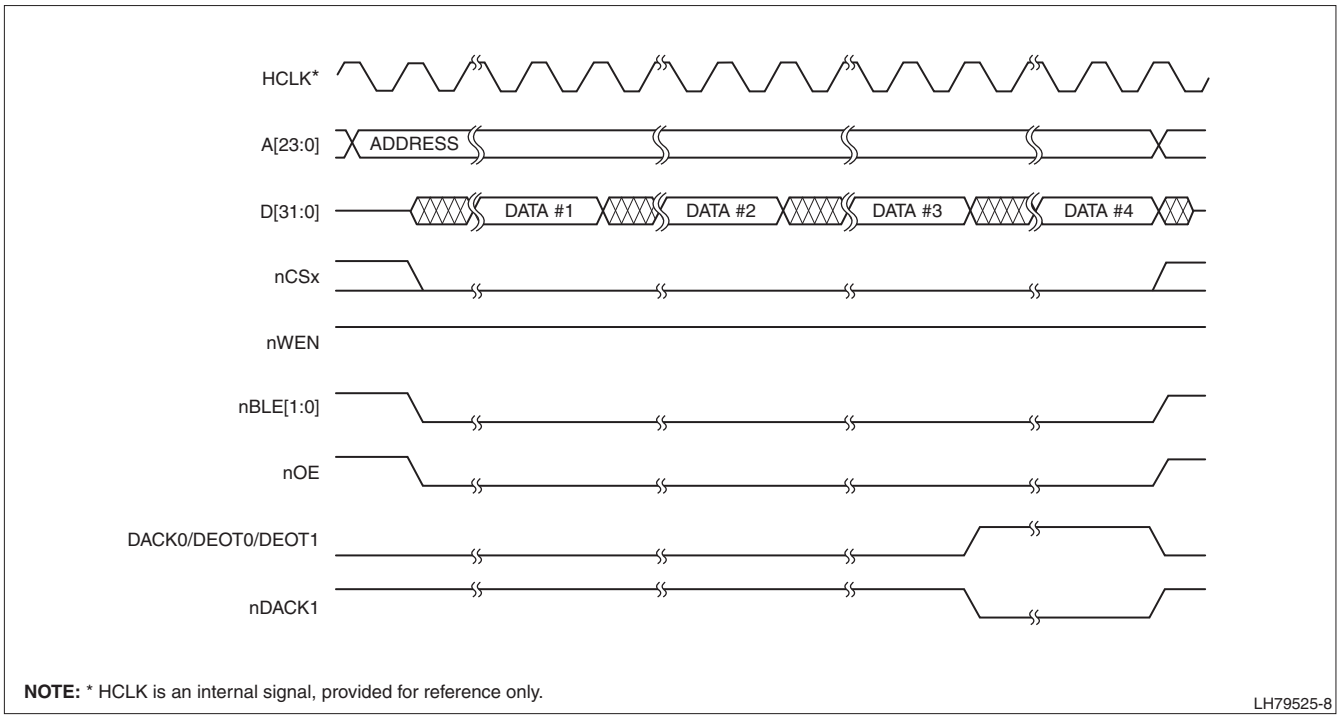


Figure 24. Read, Peripheral to Memory: Peripheral Burst Size = 4

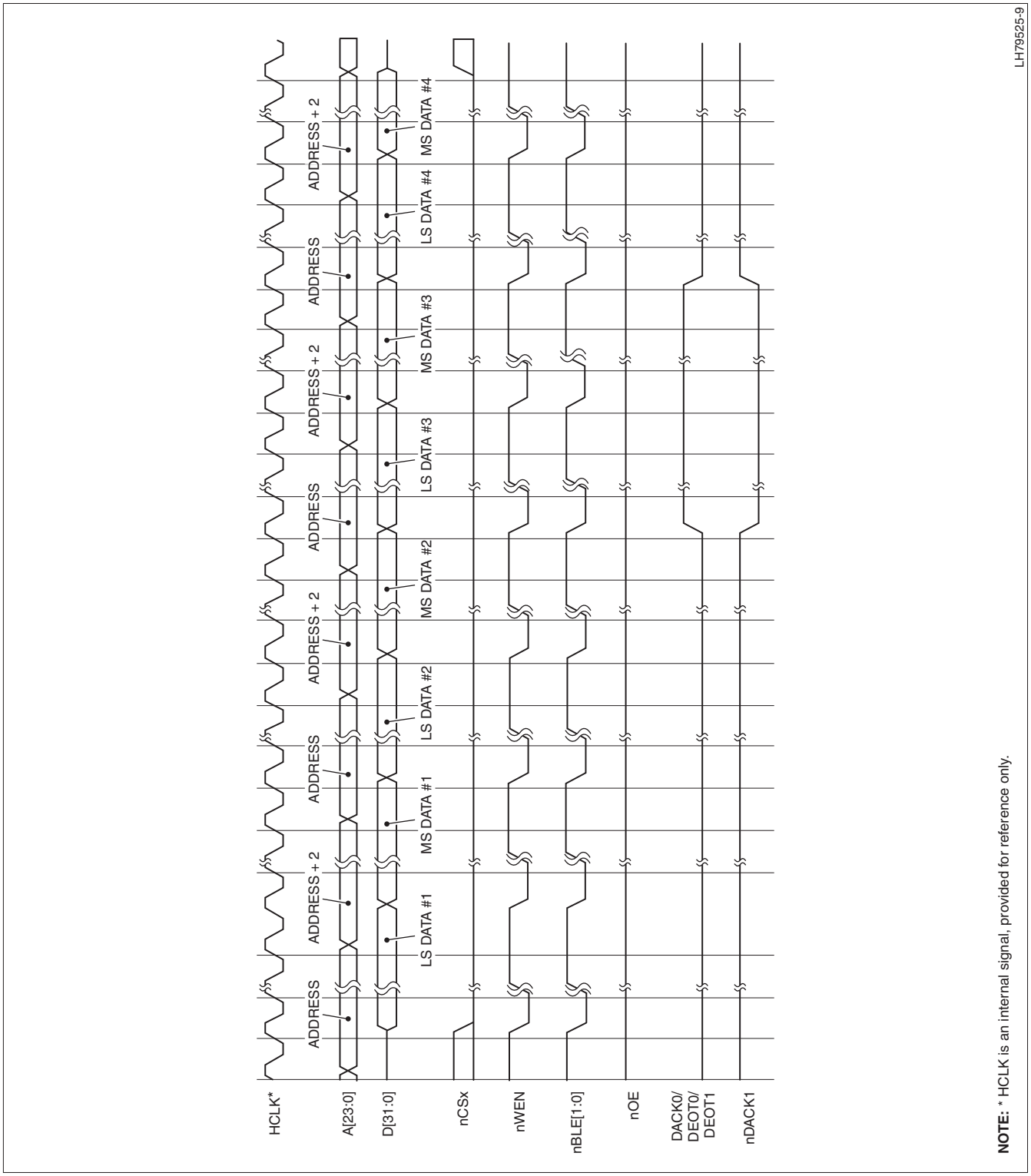


Figure 25. Write, Memory-to-Peripheral: Burst Size = 4; Destination Width > External Access Width

Color LCD Controller Timing Diagrams

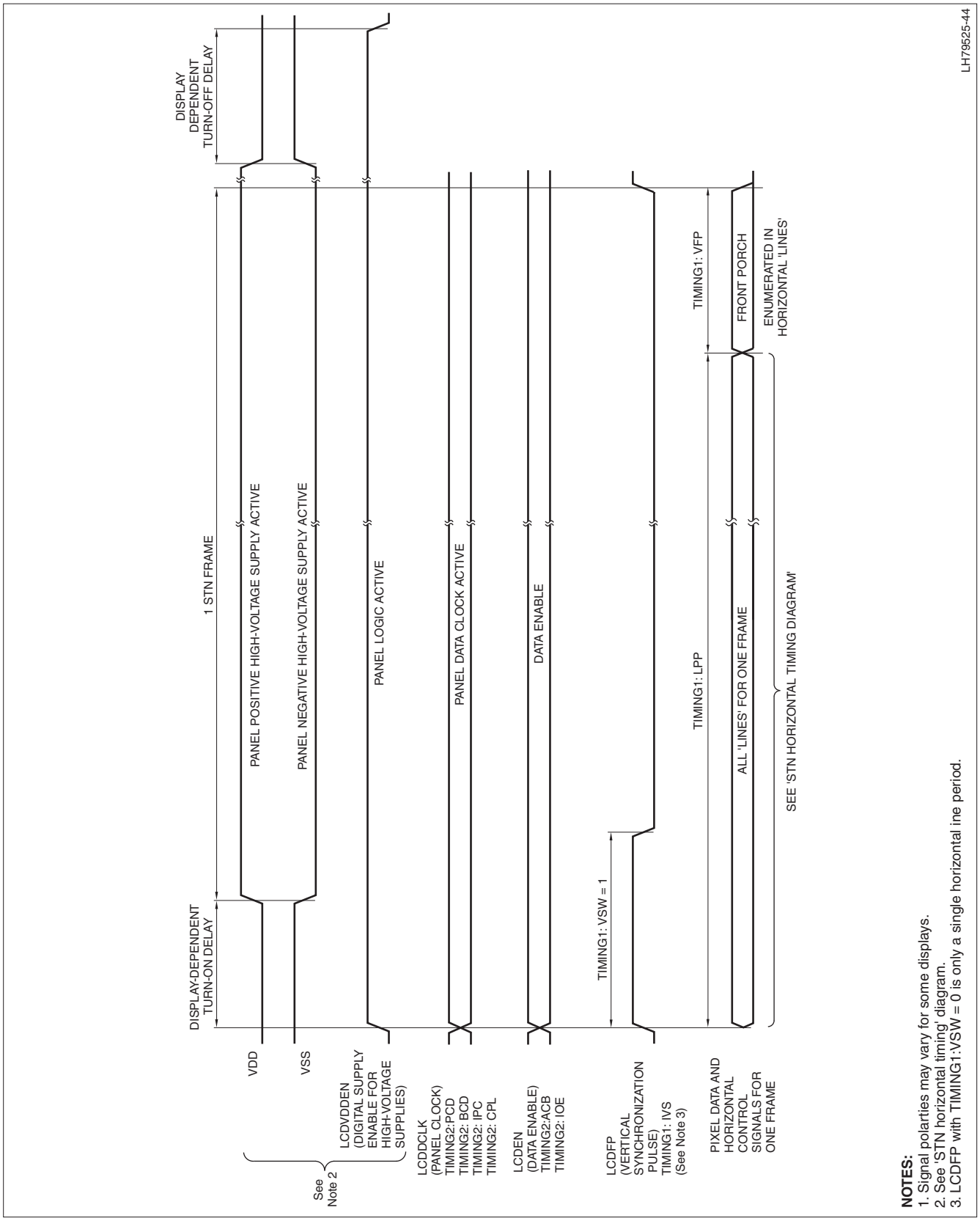


Figure 26. STN Horizontal Timing

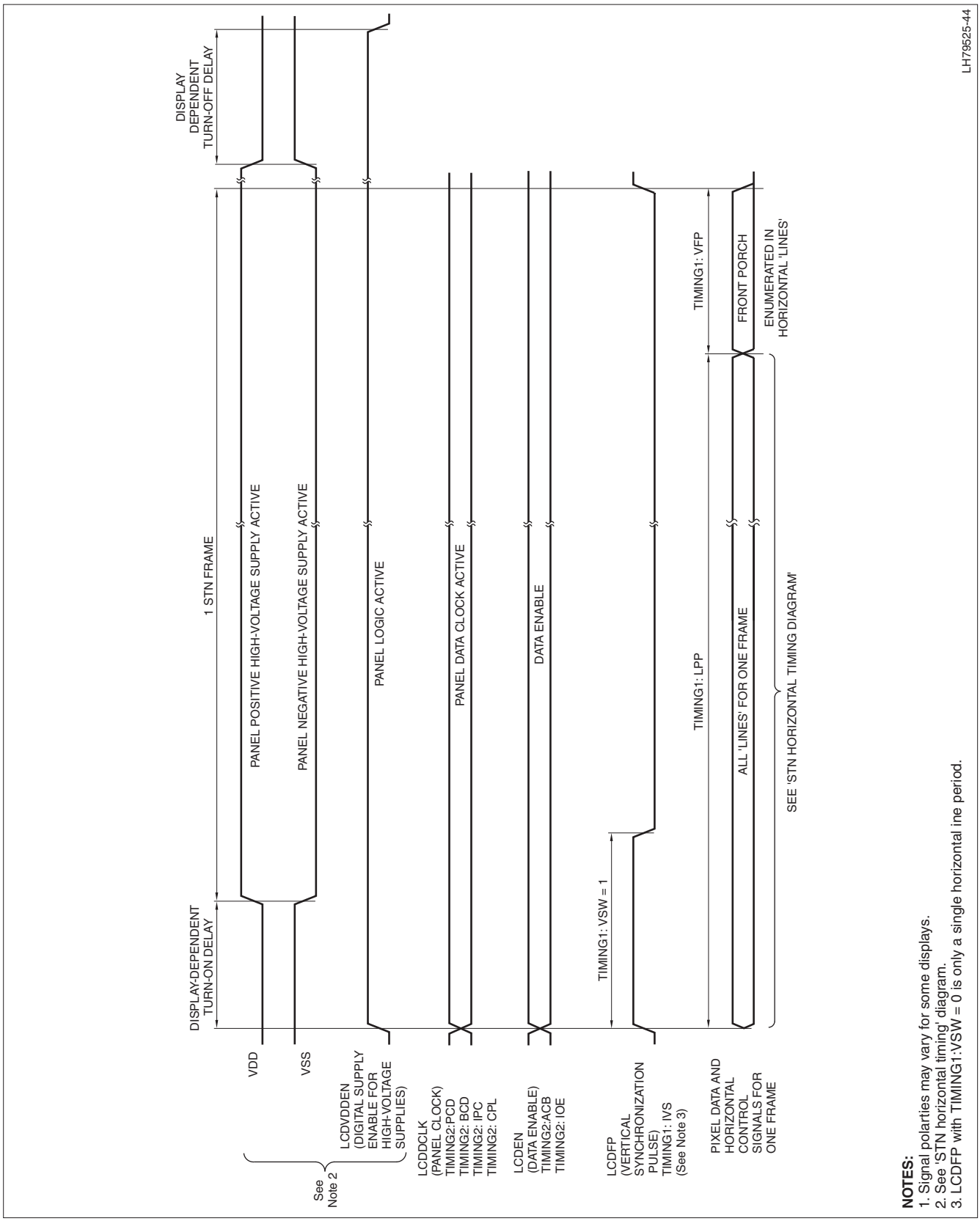


Figure 27. STN Vertical Timing

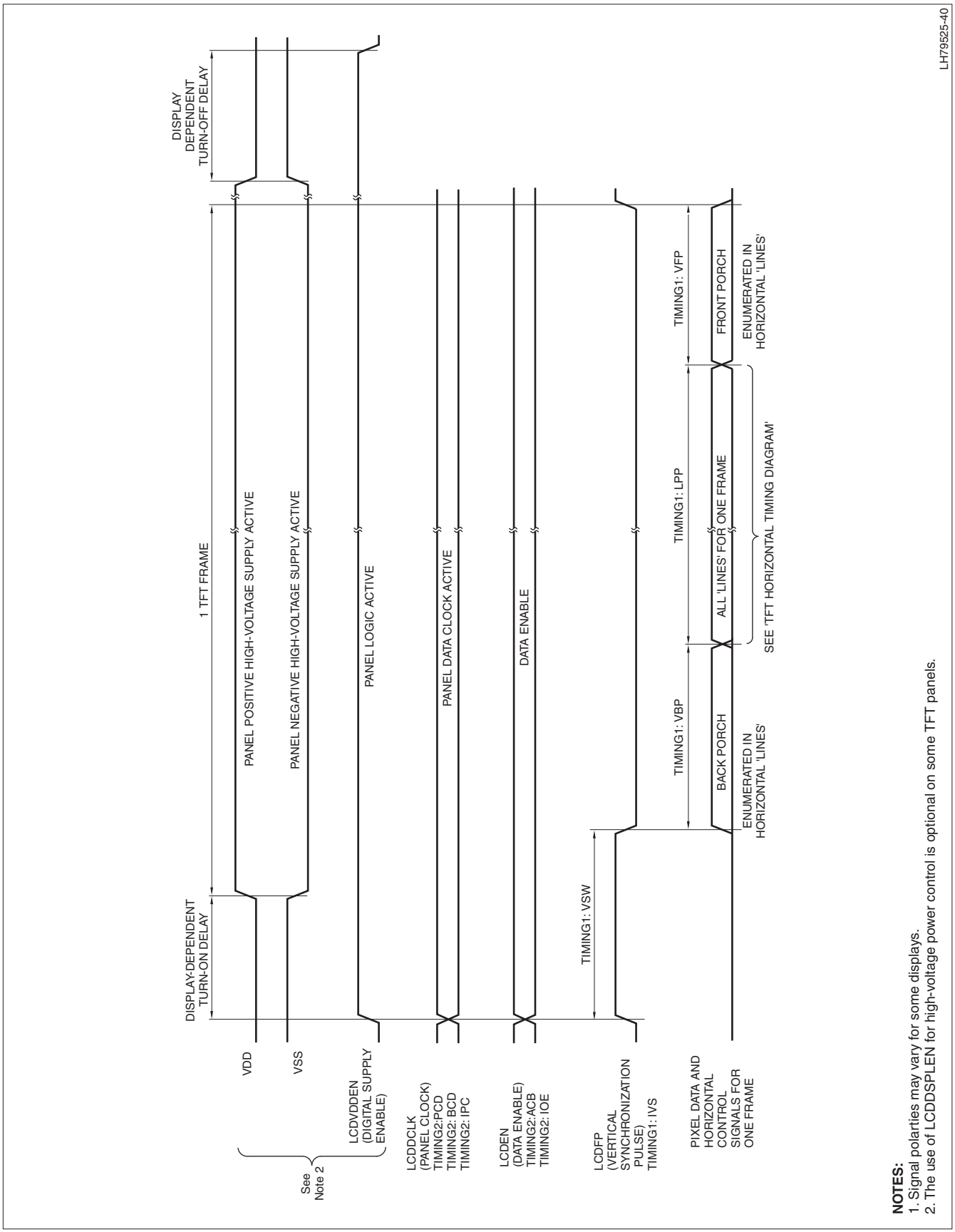


Figure 28. TFT Horizontal Timing

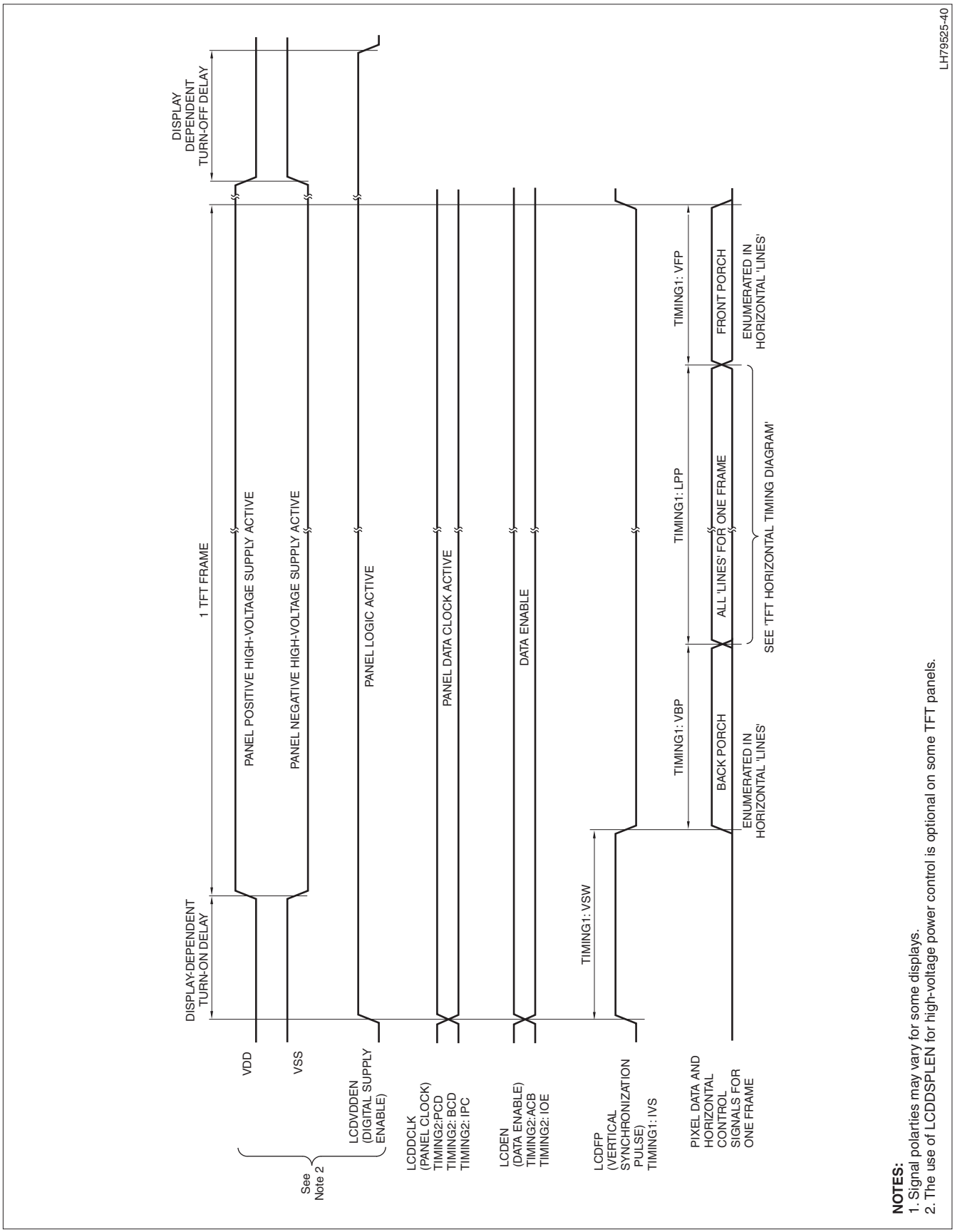


Figure 29. TFT Vertical Timing

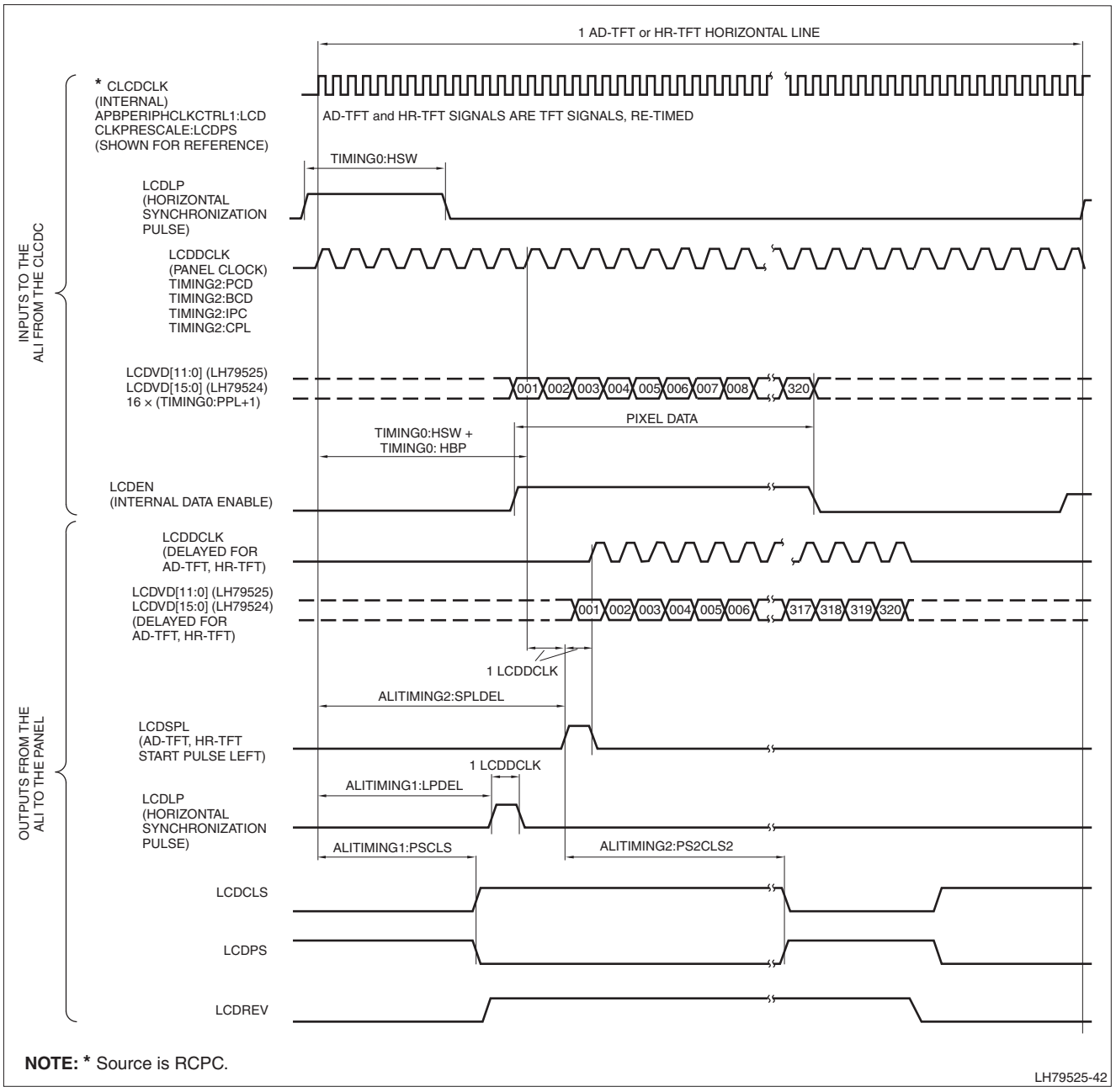


Figure 30. AD-TFT, HR-TFT Horizontal Timing

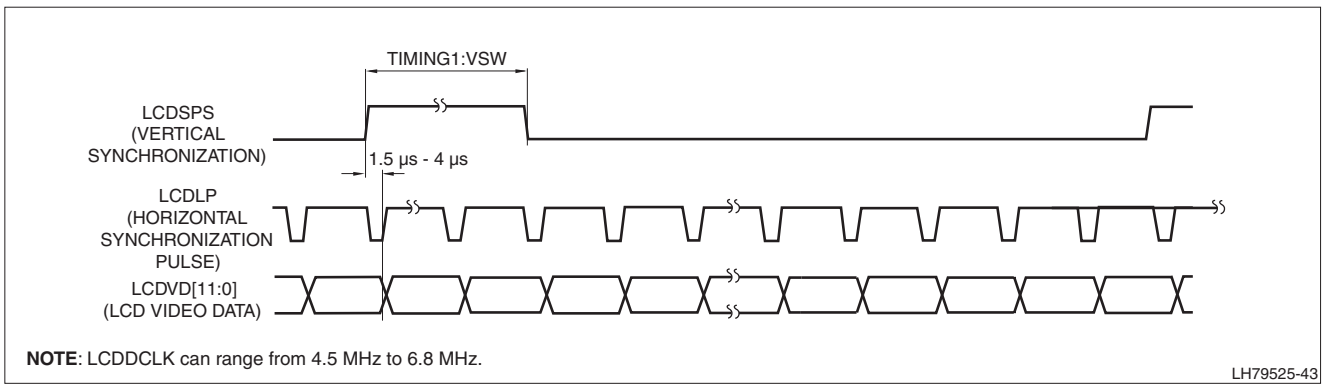
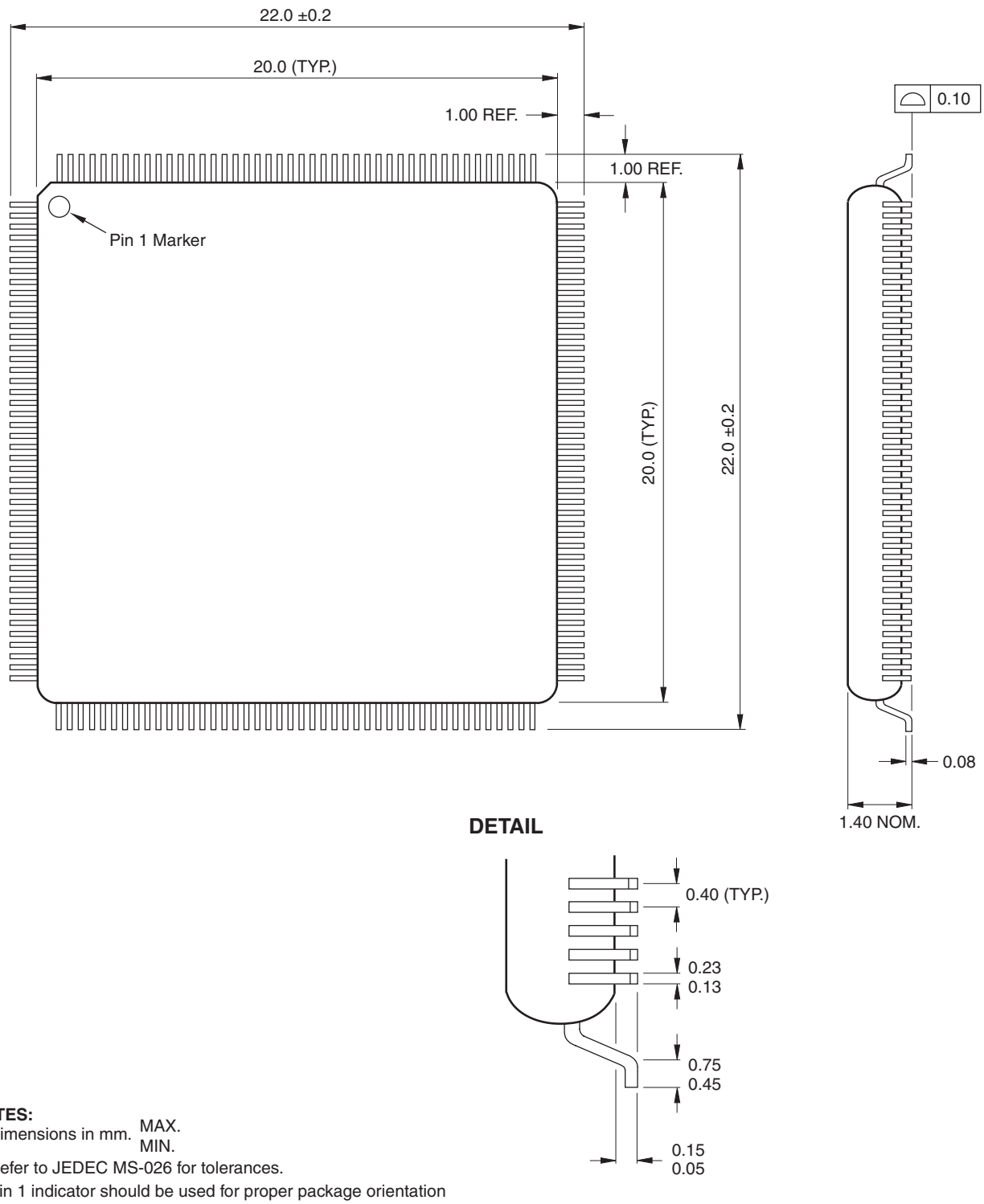


Figure 31. AD-TFT, HR-TFT Vertical Timing

PACKAGE SPECIFICATIONS

176LQFP (JEDEC MS-026)



NOTES:
1. Dimensions in mm. MAX. MIN.
2. Refer to JEDEC MS-026 for tolerances.
3. Pin 1 indicator should be used for proper package orientation (device marking orientation may change with respect to the Pin 1 indicator).

176LQFP-JEDEC

Figure 39. LH79525: 176-pin LQFP

Table 18. Record of Revisions

DATE	PAGE NO.	PARAGRAPH OR ILLUSTRATION	SUMMARY OF CHANGES
3/6/06	1	5 V Tolerant bullet	Added text denoting that the oscillator pins are NOT 5V tolerant.
	4, 9, 12, 15	Pinout Tables	UART0 and UART1 positions reversed in Pinout Tables; UART0 functions muxed with PB[7:6] and UART1 functions muxed with PB[5:4].
	10	Notes	Added 'The internal pullup and pulldown resistance on all digital I/O pins is 50KΩ to notes 1 and 2.
	16	Notes	Added 'The internal pullup and pulldown resistance on all digital I/O pins is 50KΩ to notes 1 and 2.
	22	Table 11	Added 'RTC 32 kHz Oscillator' row to table.
	26	DC Specifications	IOL corrected to 7 mA instead of 8 mA.
	30	Analog-To-Digital Converter Electrical Characteristics	Corrected VREF+ and VREF– maximum/minimum values.
5/22/06	—	Throughout	"Commercial" temperature range references removed.
	1	Features	SDRAM data bus width corrected to 15 bits.
	8, 16	Table 2, Table 5	SDCLK drive changed to 12 mA
	10	Notes	Note 8 added (unused analog pins and XTAL32IN).
	16	Notes	Note 8 added (unused analog pins and XTAL32IN).
	25	Recommended Operating Conditions	Footnote 4 added.
	26	Power Supply Sequencing	Section added.
	26	DC Specifications	Added 12 mA-capable pins to VOH and VOL.
	28	Table	Revamped Asynchronous Memory timing values for A.1 silicon.
	29	Table 9	Updated Output Hold times for Ethernet Transmit signals.
	28	Table 9	For Synchronous Memory, Changed tIHD to 1.5ns; all Output Hold signals changed to: tSDCLK/2 - 4.0 ns.
	30	Analog-To-Digital Converter Electrical Characteristics	Inserted new values for A.1 for Offset, Gain, and INL Min.
	37, 38	Figure 15, Figure 16	Replaced with updated figures for A.1 silicon.
	55, 56	Figure 39, Figure 40	Added note about pin/ball 1 designation.
10/31/06	All	Throughout	Version number changed to 1.0.
	33	Figure 9	Figure replaced with updated figure.
	34 – 36	Figure 10 – Figure 14	nWAIT figures added.
	33 & 35	Table 15 and Table 16	nWAIT parameter definition tables added.