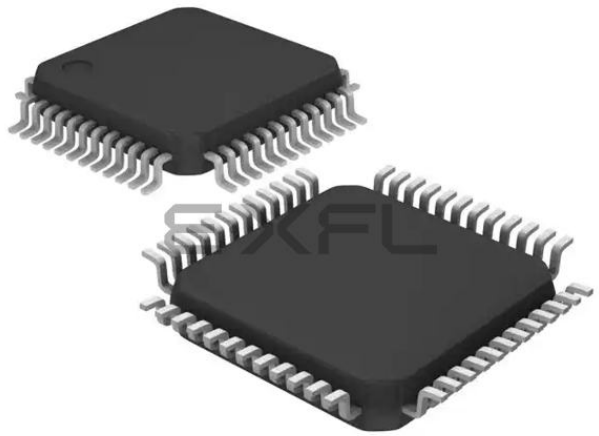

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Details	
Product Status	Active
Core Processor	HCS12
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, EBI/EMI, SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	31
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s12c128cfae

1.2 Memory Map and Registers

1.2.1 Device Memory Map

Table 1-1 shows the device register map after reset. Figure 1-2 through Figure 1-6 illustrate the full device memory map.

Table 1-1. Device Register Map Overview

Address	Module	Size
0x0000–0x0017	Core (ports A, B, E, modes, inits, test)	24
0x0018	Reserved	1
0x0019	Voltage regulator (VREG)	1
0x001A–0x001B	Device ID register	2
0x001C–0x001F	Core (MEMSIZ, IRQ, HPRIO)	4
0x0020–0x002F	Core (DBG)	16
0x0030–0x0033	Core (PPAGE[1])	4
0x0034–0x003F	Clock and reset generator (CRG)	12
0x0040–0x006F	Standard timer module (TIM)	48
0x0070–0x007F	Reserved	16
0x0080–0x009F	Analog-to-digital converter (ATD)	32
0x00A0–0x00C7	Reserved	40
0x00C8–0x00CF	Serial communications interface (SCI)	8
0x00D0–0x00D7	Reserved	8
0x00D8–0x00DF	Serial peripheral interface (SPI)	8
0x00E0–0x00FF	Pulse width modulator (PWM)	32
0x0100–0x010F	Flash control register	16
0x0110–0x013F	Reserved	48
0x0140–0x017F	Scalable controller area network (MSCAN)[2]	64
0x0180–0x023F	Reserved	192
0x0240–0x027F	Port integration module (PIM)	64
0x0280–0x03FF	Reserved	384

1. External memory paging is not supported on this device (Section 1.7.1, “PPAGE”).
2. Not available on MC9S12GC Family devices

Table 1-2. Detailed MSCAN Foreground Receive and Transmit Buffer Layout (continued)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0xXXX2	Extended ID	Read:	ID14	ID13	ID12	ID11	ID10	ID9	ID8	ID7
	Standard ID	Read:								
	CANxRIDR2	Write:								
0xXXX3	Extended ID	Read:	ID6	ID5	ID4	ID3	ID2	ID1	ID0	RTR
	Standard ID	Read:								
	CANxRIDR3	Write:								
0xXXX4–0xXXXB	CANxRDSR0–CANxRDSR7	Read:	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
		Write:								
0xXXXC	CANRxDLR	Read:					DLC3	DLC2	DLC1	DLC0
		Write:								
0xXXXD	Reserved	Read:								
		Write:								
0xXXXE	CANxRTSRH	Read:	TSR15	TSR14	TSR13	TSR12	TSR11	TSR10	TSR9	TSR8
		Write:								
0xXXXF	CANxRTSRL	Read:	TSR7	TSR6	TSR5	TSR4	TSR3	TSR2	TSR1	TSR0
		Write:								
0xxx10	Extended ID CANxTIDR0	Read:	ID28	ID27	ID26	ID25	ID24	ID23	ID22	ID21
		Write:								
	Standard ID	Read:	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3
		Write:								
0xxx11	Extended ID CANxTIDR1	Read:	ID20	ID19	ID18	SRR=1	IDE=1	ID17	ID16	ID15
		Write:								
	Standard ID	Read:	ID2	ID1	ID0	RTR	IDE=0			
		Write:								
0xxx12	Extended ID CANxTIDR2	Read:	ID14	ID13	ID12	ID11	ID10	ID9	ID8	ID7
		Write:								
	Standard ID	Read:								
		Write:								
0xxx13	Extended ID CANxTIDR3	Read:	ID6	ID5	ID4	ID3	ID2	ID1	ID0	RTR
		Write:								
	Standard ID	Read:								
		Write:								
0xxx14–0xxx1B	CANxTDSR0–CANxTDSR7	Read:	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
		Write:								
0xxx1C	CANxTDLR	Read:					DLC3	DLC2	DLC1	DLC0
		Write:								
0xxx1D	CONxTTBPR	Read:	PRIO7	PRIO6	PRIO5	PRIO4	PRIO3	PRIO2	PRIO1	PRIO0
		Write:								
0xxx1E	CANxTTSRH	Read:	TSR15	TSR14	TSR13	TSR12	TSR11	TSR10	TSR9	TSR8
		Write:								
0xxx1F	CANxTTSRL	Read:	TSR7	TSR6	TSR5	TSR4	TSR3	TSR2	TSR1	TSR0
		Write:								

1.3.4.13 PE2 / R/$\overline{W}$ — Port E I/O Pin [2] / Read/Write

In all modes this pin can be used as a general-purpose I/O and is an input with an active pull-up out of reset. If the read/write function is required it should be enabled by setting the RDWE bit in the PEAR register. External writes will not be possible until enabled. This pin is not available in the 48- / 52-pin package versions.

1.3.4.14 PE1 / $\overline{IRQ}$ — Port E Input Pin [1] / Maskable Interrupt Pin

The $\overline{IRQ}$ input provides a means of applying asynchronous interrupt requests to the MCU. Either falling edge-sensitive triggering or level-sensitive triggering is program selectable (INTCR register). $\overline{IRQ}$ is always enabled and configured to level-sensitive triggering out of reset. It can be disabled by clearing IRQEN bit (INTCR register). When the MCU is reset the $\overline{IRQ}$ function is masked in the condition code register. This pin is always an input and can always be read. There is an active pull-up on this pin while in reset and immediately out of reset. The pull-up can be turned off by clearing PUPEE in the PUCR register.

1.3.4.15 PE0 / $\overline{XIRQ}$ — Port E input Pin [0] / Non Maskable Interrupt Pin

The $\overline{XIRQ}$ input provides a means of requesting a non-maskable interrupt after reset initialization. During reset, the X bit in the condition code register (CCR) is set and any interrupt is masked until MCU software enables it. Because the $\overline{XIRQ}$ input is level sensitive, it can be connected to a multiple-source wired-OR network. This pin is always an input and can always be read. There is an active pull-up on this pin while in reset and immediately out of reset. The pull-up can be turned off by clearing PUPEE in the PUCR register.

1.3.4.16 PAD[7:0] / AN[7:0] — Port AD I/O Pins [7:0]

PAD7–PAD0 are general purpose I/O pins and also analog inputs for the analog to digital converter. In order to use a PAD pin as a standard input, the corresponding ATDDIEN register bit must be set. These bits are cleared out of reset to configure the PAD pins for A/D operation.

When the A/D converter is active in multi-channel mode, port inputs are scanned and converted irrespective of Port AD configuration. Thus Port AD pins that are configured as digital inputs or digital outputs are also converted in the A/D conversion sequence.

1.3.4.17 PP[7] / KWP[7] — Port P I/O Pin [7]

PP7 is a general purpose input or output pin, shared with the keypad interrupt function. When configured as an input, it can generate interrupts causing the MCU to exit stop or wait mode. This pin is not available in the 48- / 52-pin package versions.

1.3.4.18 PP[6] / KWP[6]/ROMCTL — Port P I/O Pin [6]

PP6 is a general purpose input or output pin, shared with the keypad interrupt function. When configured as an input, it can generate interrupts causing the MCU to exit stop or wait mode. This pin is not available in the 48- / 52-pin package versions. During MCU expanded modes of operation, this pin is used to enable

1.3.5.4 V_{DDA}, V_{SSA} — Power Supply Pins for ATD and VREG

V_{DDA}, V_{SSA} are the power supply and ground input pins for the voltage regulator reference and the analog to digital converter.

1.3.5.5 V_{RH}, V_{RL} — ATD Reference Voltage Input Pins

V_{RH} and V_{RL} are the reference voltage input pins for the analog to digital converter.

1.3.5.6 V_{DDPLL}, V_{SSPLL} — Power Supply Pins for PLL

Provides operating voltage and ground for the oscillator and the phased-locked loop. This allows the supply voltage to the oscillator and PLL to be bypassed independently. This 2.5V voltage is generated by the internal voltage regulator.

Table 1-6. Power and Ground Connection Summary

Mnemonic	Nominal Voltage (V)	Description
$V_{DD1, VDD2}$	2.5	Internal power and ground generated by internal regulator. These also allow an external source to supply the core V_{DD}/V_{SS} voltages and bypass the internal voltage regulator. In the 48 and 52 LQFP packages V_{DD2} and V_{SS2} are not available.
$V_{SS1, VSS2}$	0	
V_{DDR}	5.0	External power and ground, supply to internal voltage regulator.
V_{SSR}	0	
V_{DDX}	5.0	External power and ground, supply to pin drivers.
V_{SSX}	0	
V_{DDA}	5.0	Operating voltage and ground for the analog-to-digital converters and the reference for the internal voltage regulator, allows the supply voltage to the A/D to be bypassed independently.
V_{SSA}	0	
V_{RH}	5.0	Reference voltage low for the ATD converter. In the 48 and 52 LQFP packages V_{RL} is bonded to V_{SSA}.
V_{RL}	0	
V_{DDPLL}	2.5	Provides operating voltage and ground for the phased-locked loop. This allows the supply voltage to the PLL to be bypassed independently. Internal power and ground generated by internal regulator.
V_{SSPLL}	0	

NOTE

All V_{SS} pins must be connected together in the application. Because fast signal transitions place high, short-duration current demands on the power supply, use bypass capacitors with high-frequency characteristics and place them as close to the MCU as possible. Bypass requirements depend on MCU pin load.

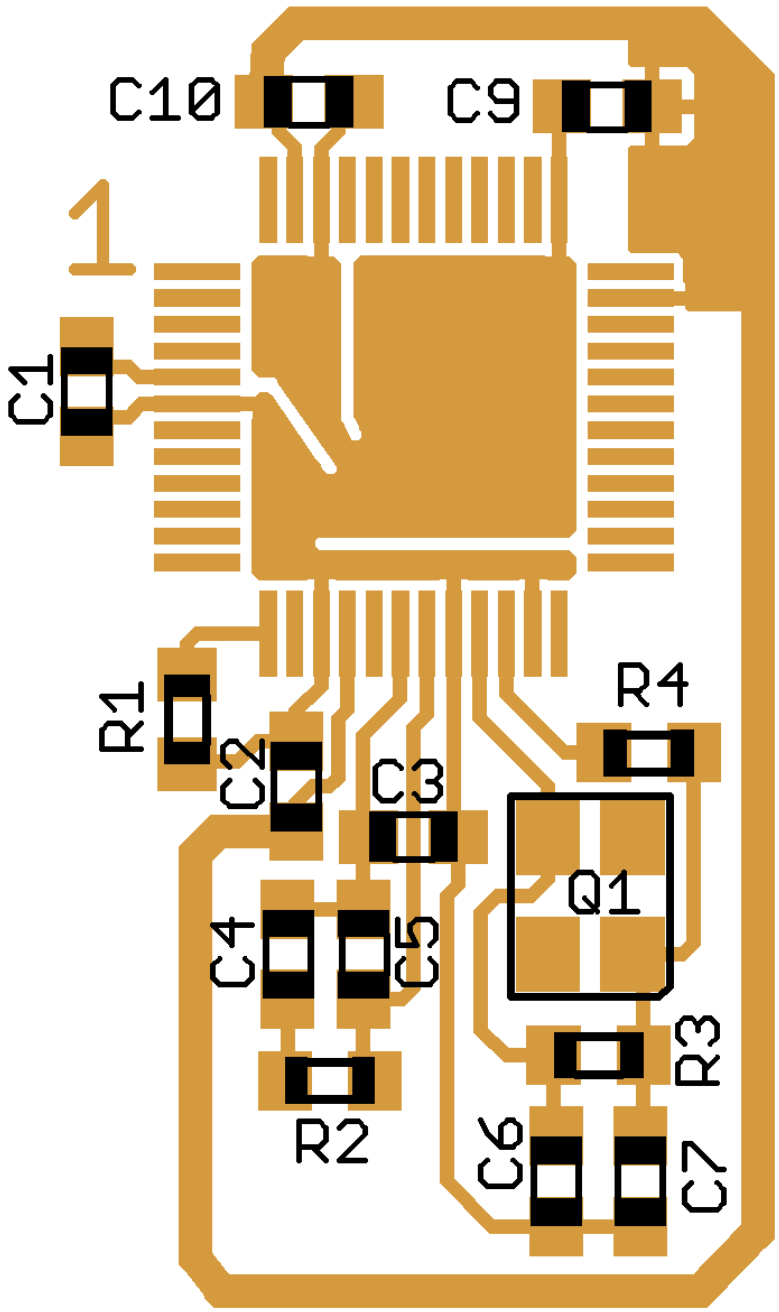


Figure 1-18. Recommended PCB Layout for 48 LQFP Pierce Oscillator

Chapter 2
Port Integration Module (PIM9C32) Block Description

2.1 Introduction

The Port Integration Module establishes the interface between the peripheral modules and the I/O pins for all ports.

This chapter covers:

- Port A, B, and E related to the core logic and the multiplexed bus interface
- Port T connected to the TIM module (PWM module can be routed to port T as well)
- Port S connected to the SCI module
- Port M associated to the MSCAN and SPI module
- Port P connected to the PWM module, external interrupt sources available
- Port J pins can be used as external interrupt sources and standard I/O's

The following I/O pin configurations can be selected:

- Available on all I/O pins:
  - Input/output selection
  - Drive strength reduction
  - Enable and select of pull resistors
- Available on all Port P and Port J pins:
  - Interrupt enable and status flags

The implementation of the Port Integration Module is device dependent.

2.1.1 Features

A standard port has the following minimum features:

- Input/output selection
- 5-V output drive with two selectable drive strength
- 5-V digital and analog input
- Input with selectable pull-up or pull-down device

Optional features:

- Open drain for wired-OR connections
- Interrupt inputs with glitch filtering

Table 4-8. MODC, MODB, and MODA Write Capability[1]

MODC	MODB	MODA	Mode	MODx Write Capability
0	0	0	Special single chip	MODC, MODB, and MODA write anytime but not to 110[2]
0	0	1	Emulation narrow	No write
0	1	0	Special test	MODC, MODB, and MODA write anytime but not to 110[2]
0	1	1	Emulation wide	No write
1	0	0	Normal single chip	MODC write never, MODB and MODA write once but not to 110
1	0	1	Normal expanded narrow	No write
1	1	0	Special peripheral	No write
1	1	1	Normal expanded wide	No write

1. No writes to the MOD bits are allowed while operating in a secure mode. For more details, refer to the device overview chapter.
2. If you are in a special single-chip or special test mode and you write to this register, changing to normal single-chip mode, then one allowed write to this register remains. If you write to normal expanded or emulation mode, then no writes remain.

4.3.2.10 Pull Control Register (PUCR)

Module Base + 0x000C
Starting address location affected by INITRG register setting.

	7	6	5	4	3	2	1	0
R	PUPKE	0	0	PUPEE	0	0	PUPBE	PUPAE
W								
Reset[1]	1	0	0	1	0	0	0	0

NOTES:
1. The default value of this parameter is shown. Please refer to the device overview chapter to determine the actual reset state of this register.

= Unimplemented or Reserved

Figure 4-14. Pull Control Register (PUCR)

Read: Anytime (provided this register is in the map).

Write: Anytime (provided this register is in the map).

This register is used to select pull resistors for the pins associated with the core ports. Pull resistors are assigned on a per-port basis and apply to any pin in the corresponding port that is currently configured as an input. The polarity of these pull resistors is determined by chip integration. Please refer to the device overview chapter to determine the polarity of these resistors.

7.4.2.6 Capture Modes

The DBG in DBG mode can operate in four capture modes. These modes are described in the following subsections.

7.4.2.6.1 Normal Mode

In normal mode, the DBG module uses comparator A and B as triggering devices. Change-of-flow information or data will be stored depending on TRG in DBGSC.

7.4.2.6.2 Loop1 Mode

The intent of loop1 mode is to prevent the trace buffer from being filled entirely with duplicate information from a looping construct such as delays using the DBNE instruction or polling loops using BRSET/BRCLR instructions. Immediately after address information is placed in the trace buffer, the DBG module writes this value into the C comparator and the C comparator is placed in ignore address mode. This will prevent duplicate address entries in the trace buffer resulting from repeated bit-conditional branches. Comparator C will be cleared when the ARM bit is set in loop1 mode to prevent the previous contents of the register from interfering with loop1 mode operation. Breakpoints based on comparator C are disabled.

Loop1 mode only inhibits duplicate source address entries that would typically be stored in most tight looping constructs. It will not inhibit repeated entries of destination addresses or vector addresses, because repeated entries of these would most likely indicate a bug in the user's code that the DBG module is designed to help find.

NOTE

In certain very tight loops, the source address will have already been fetched again before the C comparator is updated. This results in the source address being stored twice before further duplicate entries are suppressed. This condition occurs with branch-on-bit instructions when the branch is fetched by the first P-cycle of the branch or with loop-construct instructions in which the branch is fetched with the first or second P cycle. See examples below:

```
LOOP   INCX                    ; 1-byte instruction fetched by 1st P-cycle of BRCLR
       BRCLR CMPTMP,#$0c,LOOP  ; the BRCLR instruction also will be fetched by 1st P-cycle of BRCLR

LOOP2  BRN   *                 ; 2-byte instruction fetched by 1st P-cycle of DBNE
       NOP                     ; 1-byte instruction fetched by 2nd P-cycle of DBNE
       DBNE  A,LOOP2           ; this instruction also fetched by 2nd P-cycle of DBNE
```

NOTE

Loop1 mode does not support paged memory, and inhibits duplicate entries in the trace buffer based solely on the CPU address. There is a remote possibility of an erroneous address match if program flow alternates between paged and unpaged memory space.

8.3.2.3 ATD Control Register 2 (ATDCTL2)

This register controls power down, interrupt, and external trigger. Writes to this register will abort current conversion sequence but will not start a new sequence.

Module Base + 0x0002

	7	6	5	4	3	2	1	0
R	ADPU	AFFC	AWAI	ETRIGLE	ETRIGP	ETRIGE	ASCIE	ASCIF
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 8-5. ATD Control Register 2 (ATDCTL2)

Read: Anytime

Write: Anytime

Table 8-1. ATDCTL2 Field Descriptions

Field	Description
7 ADPU	**ATD Power Down** — This bit provides on/off control over the ATD10B8C block allowing reduced MCU power consumption. Because analog electronic is turned off when powered down, the ATD requires a recovery time period after ADPU bit is enabled. 0 Power down ATD 1 Normal ATD functionality
6 AFFC	**ATD Fast Flag Clear All** 0 ATD flag clearing operates normally (read the status register ATDSTAT1 before reading the result register to clear the associate CCF flag). 1 Changes all ATD conversion complete flags to a fast clear sequence. Any access to a result register will cause the associate CCF flag to clear automatically.
5 AWAI	**ATD Power Down in Wait Mode** — When entering Wait Mode this bit provides on/off control over the ATD10B8C block allowing reduced MCU power. Because analog electronic is turned off when powered down, the ATD requires a recovery time period after exit from Wait mode. 0 ATD continues to run in Wait mode 1 Halt conversion and power down ATD during Wait mode After exiting Wait mode with an interrupt conversion will resume. But due to the recovery time the result of this conversion should be ignored.
4 ETRIGLE	**External Trigger Level/Edge Control** — This bit controls the sensitivity of the external trigger signal. See Table 8-2 for details.
3 ETRIGP	**External Trigger Polarity** — This bit controls the polarity of the external trigger signal. See Table 8-2 for details.
2 ETRIGE	**External Trigger Mode Enable** — This bit enables the external trigger on ATD channel 7. The external trigger allows to synchronize sample and ATD conversions processes with external events. 0 Disable external trigger 1 Enable external trigger **Note:** The conversion results for the external trigger ATD channel 7 have no meaning while external trigger mode is enabled.

Table 9-12. Outcome of Clock Loss in Pseudo-Stop Mode (continued)

CME	SCME	SCMIE	CRG Actions
1	1	1	Clock failure --> – VREG enabled, – PLL enabled, – SCM activated, – Start Clock Quality Check, – SCMIF set. SCMIF generates Self-Clock Mode wakeup interrupt. – Exit Pseudo-Stop Mode in SCM using PLL clock (f_{SCM}) as system clock, – Continue to perform a additional Clock Quality Checks until OSCCLK is o.k. again.

9.4.10.2 Wake-up from Full Stop (PSTP=0)

The MCU requires an external interrupt or an external reset in order to wake-up from stop mode.

If the MCU gets an external reset during full stop mode active, the CRG asynchronously restores all configuration bits in the register space to its default settings and will perform a maximum of 50 clock *check_windows* (see Section 9.4.4, “Clock Quality Checker”). After completing the clock quality check the CRG starts the reset generator. After completing the reset sequence processing begins by fetching the normal reset vector. Full stop mode is exited and the MCU is in run mode again.

If the MCU is woken-up by an interrupt, the CRG will also perform a maximum of 50 clock *check_windows* (see Section 9.4.4, “Clock Quality Checker”). If the clock quality check is successful, the CRG will release all system and core clocks and will continue with normal operation. If all clock checks within the timeout-window are failing, the CRG will switch to self-clock mode or generate a clock monitor reset (CMRESET) depending on the setting of the SCME bit.

Because the PLL has been powered-down during stop mode the PLLSEL bit is cleared and the MCU runs on OSCCLK after leaving stop mode. The software must manually set the PLLSEL bit again, in order to switch system and core clocks to the PLLCLK.

NOTE

In full stop mode, the clock monitor is disabled and any loss of clock will not be detected.

9.5 Resets

This section describes how to reset the CRGV4 and how the CRGV4 itself controls the reset of the MCU. It explains all special reset requirements. Because the reset generator for the MCU is part of the CRG, this section also describes all automatic actions that occur during or as a result of individual reset conditions. The reset values of registers and signals are provided in Section 9.3, “Memory Map and Register

Table 10-33. Time Segment Syntax

Syntax	Description
SYNC_SEG	System expects transitions to occur on the CAN bus during this period.
Transmit Point	A node in transmit mode transfers a new value to the CAN bus at this point.
Sample Point	A node in receive mode samples the CAN bus at this point. If the three samples per bit option is selected, then this point marks the position of the third sample.

The synchronization jump width (see the Bosch CAN specification for details) can be programmed in a range of 1 to 4 time quanta by setting the SJW parameter.

The SYNC_SEG, TSEG1, TSEG2, and SJW parameters are set by programming the MSCAN bus timing registers (CANBTR0, CANBTR1) (see Section 10.3.2.3, "MSCAN Bus Timing Register 0 (CANBTR0)" and Section 10.3.2.4, "MSCAN Bus Timing Register 1 (CANBTR1)").

Table 10-34 gives an overview of the CAN compliant segment settings and the related parameter values.

NOTE

It is the user's responsibility to ensure the bit time settings are in compliance with the CAN standard.

Table 10-34. CAN Standard Compliant Bit Time Segment Settings

Time Segment 1	TSEG1	Time Segment 2	TSEG2	Synchronization Jump Width	SJW
5 .. 10	4 .. 9	2	1	1 .. 2	0 .. 1
4 .. 11	3 .. 10	3	2	1 .. 3	0 .. 2
5 .. 12	4 .. 11	4	3	1 .. 4	0 .. 3
6 .. 13	5 .. 12	5	4	1 .. 4	0 .. 3
7 .. 14	6 .. 13	6	5	1 .. 4	0 .. 3
8 .. 15	7 .. 14	7	6	1 .. 4	0 .. 3
9 .. 16	8 .. 15	8	7	1 .. 4	0 .. 3

10.4.4 Modes of Operation

10.4.4.1 Normal Modes

The MSCAN module behaves as described within this specification in all normal system operation modes.

10.4.4.2 Special Modes

The MSCAN module behaves as described within this specification in all special system operation modes.

13.4.4.2 Character Reception

During an SCI reception, the receive shift register shifts a frame in from the **Rx input** signal. The SCI data register is the read-only buffer between the internal data bus and the receive shift register.

After a complete frame shifts into the receive shift register, the data portion of the frame transfers to the SCI data register. The receive data register full flag, RDRF, in SCI status register 1 (SCISR1) becomes set, indicating that the received byte can be read. If the receive interrupt enable bit, RIE, in SCI control register 2 (SCICR2) is also set, the RDRF flag generates an RDRF interrupt request.

13.4.4.3 Data Sampling

The receiver samples the **Rx input** signal at the RT clock rate. The RT clock is an internal signal with a frequency 16 times the baud rate. To adjust for baud rate mismatch, the RT clock (see Figure 13-13) is re-synchronized:

- After every start bit
- After the receiver detects a data bit change from logic 1 to logic 0 (after the majority of data bit samples at RT8, RT9, and RT10 returns a valid logic 1 and the majority of the next RT8, RT9, and RT10 samples returns a valid logic 0)

To locate the start bit, data recovery logic does an asynchronous search for a logic 0 preceded by three logic 1s.When the falling edge of a possible start bit occurs, the RT clock begins to count to 16.

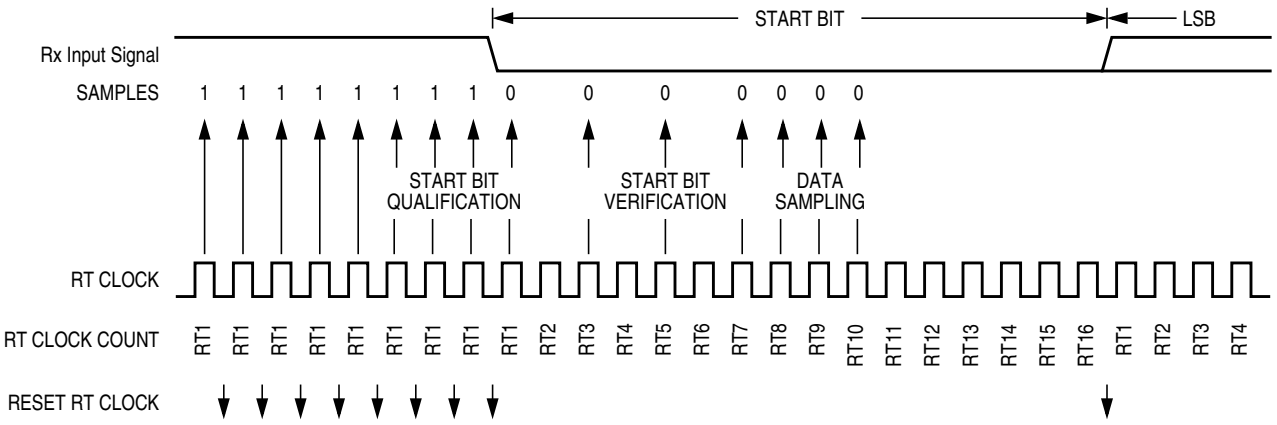


Figure 13-13. Receiver Data Sampling

To verify the start bit and to detect noise, data recovery logic takes samples at RT3, RT5, and RT7. Table 13-11 summarizes the results of the start bit verification samples.

Table 13-11. Start Bit Verification

RT3, RT5, and RT7 Samples	Start Bit Verification	Noise Flag
000	Yes	0
001	Yes	1
010	Yes	1
011	No	0

Table 17-12. FSTAT Field Descriptions

Field	Description
5 PVIOL	**Protection Violation** — The PVIOL flag indicates an attempt was made to program or erase an address in a protected Flash array memory area. The PVIOL flag is cleared by writing a 1 to PVIOL. Writing a 0 to the PVIOL flag has no effect on PVIOL. While PVIOL is set, it is not possible to launch another command. 0 No protection violation detected 1 Protection violation has occurred
4 ACCERR	**Access Error** — The ACCERR flag indicates an illegal access to the Flash array caused by either a violation of the command write sequence, issuing an illegal command (illegal combination of the CMDBx bits in the FCMD register) or the execution of a CPU STOP instruction while a command is executing (CCIF=0). The ACCERR flag is cleared by writing a 1 to ACCERR. Writing a 0 to the ACCERR flag has no effect on ACCERR. While ACCERR is set, it is not possible to launch another command. 0 No access error detected 1 Access error has occurred
2 BLANK	**Flash Array Has Been Verified as Erased** — The BLANK flag indicates that an erase verify command has checked the Flash array and found it to be erased. The BLANK flag is cleared by hardware when CBEIF is cleared as part of a new valid command write sequence. Writing to the BLANK flag has no effect on BLANK. 0 If an erase verify command has been requested, and the CCIF flag is set, then a 0 in BLANK indicates the array is not erased 1 Flash array verifies as erased
1 FAIL	**Flag Indicating a Failed Flash Operation** — In special modes, the FAIL flag will set if the erase verify operation fails (Flash array verified as not erased). Writing a 0 to the FAIL flag has no effect on FAIL. The FAIL flag is cleared by writing a 1 to FAIL. While FAIL is set, it is not possible to launch another command. 0 Flash operation completed without error 1 Flash operation failed
0 DONE	**Flag Indicating a Failed Operation is not Active** — In special modes, the DONE flag will clear if a program, erase, or erase verify operation is active. 0 Flash operation is active 1 Flash operation is not active

17.3.2.7 Flash Command Register (FCMD)

The FCMD register defines the Flash commands.

Module Base + 0x0006

	7	6	5	4	3	2	1	0
R	0	CMDB6	CMDB5	0	0	CMDB2	0	CMDB0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 17-11. Flash Command Register (FCMD)

Bits CMDB6, CMDB5, CMDB2, and CMDB0 are readable and writable during a command write sequence while bits 7, 4, 3, and 1 read 0 and are not writable.

Module Base + 0x0009

	7	6	5	4	3	2	1	0
R W	FABLO							
Reset	0	0	0	0	0	0	0	0

Figure 17-14. Flash Address Low Register (FADDRLO)

In normal modes, all FABHI and FABLO bits read 0 and are not writable. In special modes, the FABHI and FABLO bits are readable and writable. For sector erase, the MCU address bits [8:0] are ignored. For mass erase, any address within the Flash array is valid to start the command.

17.3.2.10 Flash Data Register (FDATA)

FDATAHI and FDATALO are the Flash data registers.

Module Base + 0x000A

	7	6	5	4	3	2	1	0
R W	FDHI							
Reset	0	0	0	0	0	0	0	0

Figure 17-15. Flash Data High Register (FDATAHI)

Module Base + 0x000B

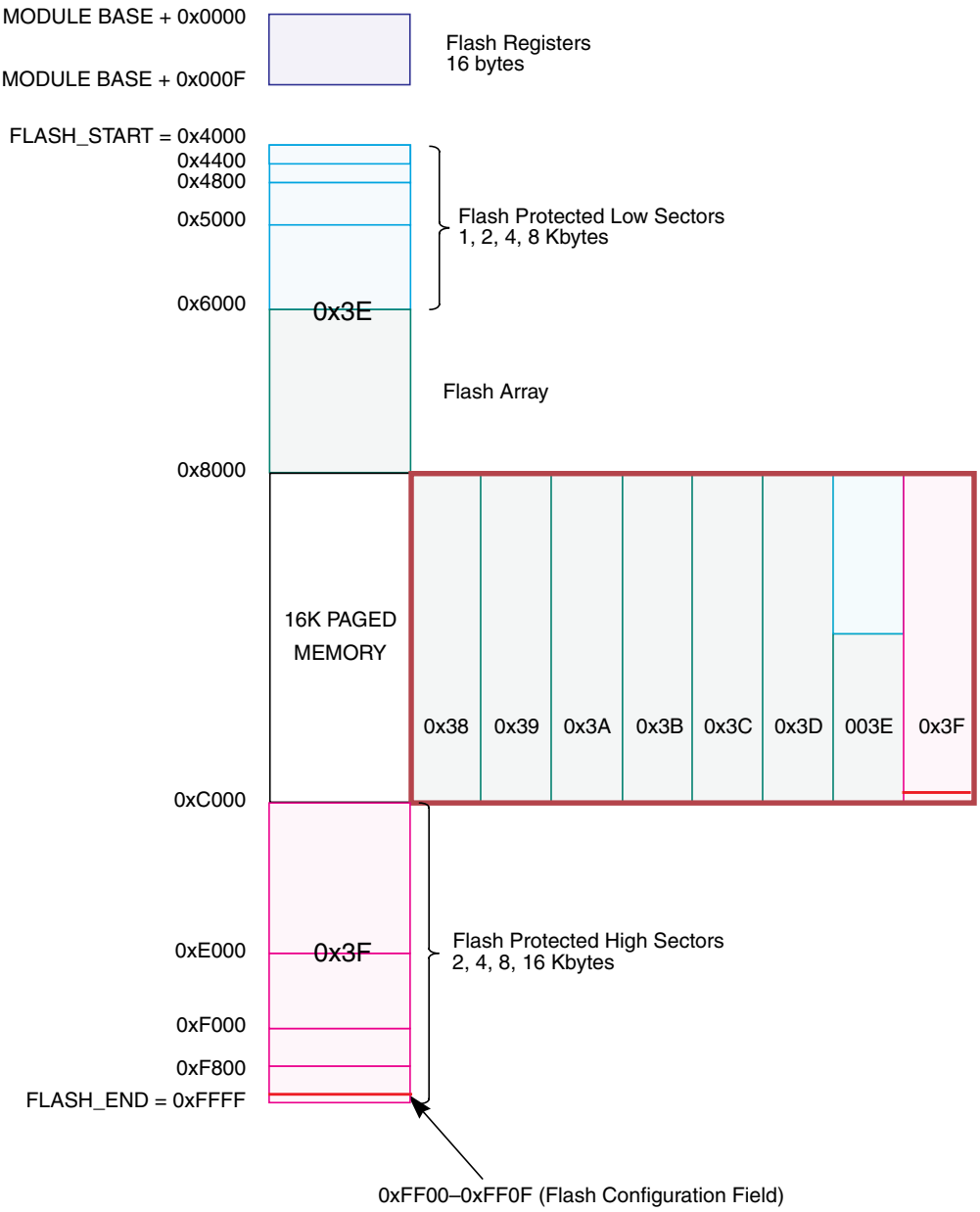
	7	6	5	4	3	2	1	0
R W	FDLO							
Reset	0	0	0	0	0	0	0	0

Figure 17-16. Flash Data Low Register (FDATALO)

In normal modes, all FDATAHI and FDATALO bits read 0 and are not writable. In special modes, all FDATAHI and FDATALO bits are readable and writable when writing to an address within the Flash address range.

17.3.2.11 RESERVED3

This register is reserved for factory testing and is not accessible to the user.



Note: 0x38–0x3F correspond to the PPAGE register content

Figure 20-3. Flash Memory Map

21.4.1.3.1 Erase Verify Command

The erase verify operation will verify that a Flash array is erased.

An example flow to execute the erase verify operation is shown in Figure 21-22. The erase verify command write sequence is as follows:

1. Write to a Flash array address to start the command write sequence for the erase verify command. The address and data written will be ignored.
2. Write the erase verify command, 0x05, to the FCMD register.
3. Clear the CBEIF flag in the FSTAT register by writing a 1 to CBEIF to launch the erase verify command.

After launching the erase verify command, the CCIF flag in the FSTAT register will set after the operation has completed unless a new command write sequence has been buffered. Upon completion of the erase verify operation, the BLANK flag in the FSTAT register will be set if all addresses in the Flash array are verified to be erased. If any address in the Flash array is not erased, the erase verify operation will terminate and the BLANK flag in the FSTAT register will remain clear.

A.1.8 Power Dissipation and Thermal Characteristics

Power dissipation and thermal characteristics are closely related. The user must assure that the maximum operating junction temperature is not exceeded. The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \bullet \Theta_{JA})$$

T_J = Junction Temperature, [°C]

T_A = Ambient Temperature, [°C]

P_D = Total Chip Power Dissipation, [W]

Θ_{JA} = Package Thermal Resistance, [°C/W]

The total power dissipation can be calculated from:

$$P_D = P_{INT} + P_{IO}$$

P_{INT} = Chip Internal Power Dissipation, [W]

Two cases with internal voltage regulator enabled and disabled must be considered:

1. Internal Voltage Regulator disabled

$$P_{INT} = I_{DD} \cdot V_{DD} + I_{DDPLL} \cdot V_{DDPLL} + I_{DDA} \cdot V_{DDA}$$

$$P_{IO} = \sum_i R_{DSON} \cdot I_{IO_i}^2$$

Which is the sum of all output currents on I/O ports associated with V_{DDX} and V_{DDM}.
For R_{DSON} is valid:

$$R_{DSON} = \frac{V_{OL}}{I_{OL}}; \text{for outputs driven low}$$

respectively

$$R_{DSON} = \frac{V_{DD5} - V_{OH}}{I_{OH}}; \text{for outputs driven high}$$

2. Internal voltage regulator enabled

$$P_{INT} = I_{DDR} \cdot V_{DDR} + I_{DDA} \cdot V_{DDA}$$

I_{DDR} is the current shown in Table A-8 and not the overall current flowing into VDDR, which additionally contains the current flowing into the external loads with output high.

$$P_{IO} = \sum_i R_{DSON} \cdot I_{IO_i}^2$$

Which is the sum of all output currents on I/O ports associated with V_{DDX} and V_{DDR}.

Table A-17. PLL Characteristics

Conditions are shown in Table A-4 unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Self Clock Mode frequency	f_{SCM}	1	—	5.5	MHz
2	D	VCO locking range	f_{VCO}	8	—	50	MHz
3	D	Lock Detector transition from Acquisition to Tracking mode	$\|\Delta_{trk}\|$	3	—	4	%(1)
4	D	Lock Detection	$\|\Delta_{Lock}\|$	0	—	1.5	%[1]
5	D	Un-Lock Detection	$\|\Delta_{unl}\|$	0.5	—	2.5	%[1]
6	D	Lock Detector transition from Tracking to Acquisition mode	$\|\Delta_{unt}\|$	6	—	8	%[1]
7	C	PLLON Total Stabilization delay (Auto Mode) (2)	t_{stab}	—	0.5	—	ms
8	D	PLLON $_{Acquisition}$ mode stabilization delay [2]	t_{acq}	—	0.3	—	ms
9	D	PLLON Tracking mode stabilization delay [2]	t_{al}	—	0.2	—	ms
10	D	Fitting parameter VCO loop gain	K_1	—	-100	—	MHz/V
11	D	Fitting parameter VCO loop frequency	f_1	—	60	—	MHz
12	D	Charge pump current acquisition mode	$\| i_{ch} \|$	—	38.5	—	µA
13	D	Charge pump current tracking mode	$\| i_{ch} \|$	—	3.5	—	µA
14	C	Jitter fit parameter 1[2]	j_1	—	—	1.1	%
15	C	Jitter fit parameter 2[2]	j_2	—	—	0.13	%

1. % deviation from target frequency
2. f_{OSC} = 4MHz, f_{BUS} = 25MHz equivalent f_{VCO} = 50MHz: REFDV = #$03, SYNR = #$018, Cs = 4.7nF, Cp = 470pF, Rs = 10KΩ.

A.5 NVM, Flash, and EEPROM

A.5.1 NVM Timing

The time base for all NVM program or erase operations is derived from the oscillator. A minimum oscillator frequency f_{NVMOSC} is required for performing program or erase operations. The NVM modules do not have any means to monitor the frequency and will not prevent program or erase operation at frequencies above or below the specified minimum. Attempting to program or erase the NVM modules at a lower frequency a full program or erase transition is not assured.

The Flash program and erase operations are timed using a clock derived from the oscillator using the FCLKDIV and ECLKDIV registers respectively. The frequency of this clock must be set within the limits specified as f_{NVMOP}.

The minimum program and erase times shown in Table A-18 are calculated for maximum f_{NVMOP} and maximum f_{bus}. The maximum times are calculated for minimum f_{NVMOP} and a f_{bus} of 2MHz.

Appendix E
Ordering Information

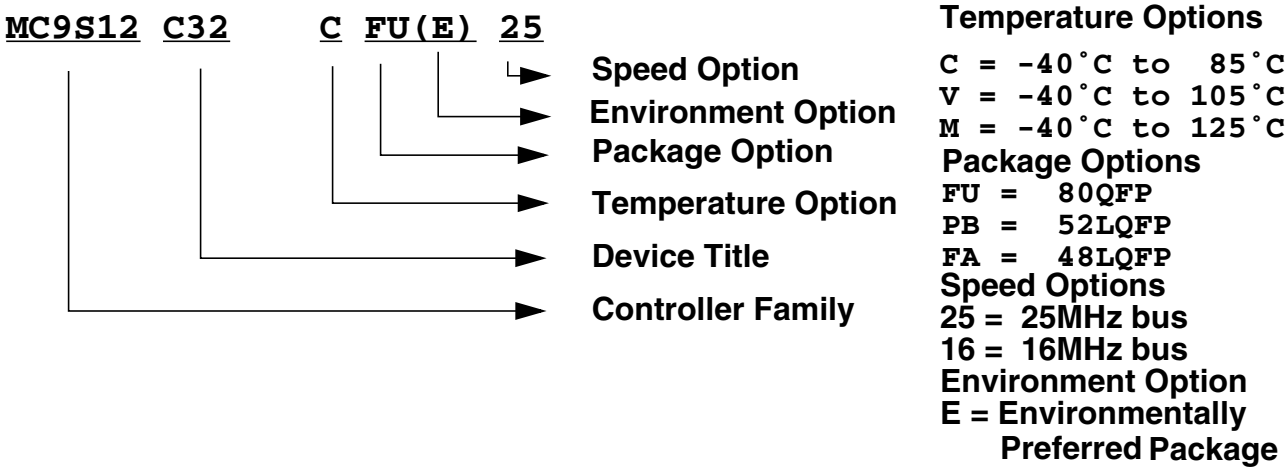


Figure E-1. Order Part number Coding

Table E-1. lists C-family part number coding based on package, speed and temperature and die options.

Table E-2. lists CG-family part number coding based on package, speed and temperature and die options.

Table E-1. MC9S12C-Family / MC9S12GC-Family Part Number Coding

Part Number	Mask[1] set	Temp.	Package	Speed	Die Type	Flash	RAM	I/O[2], [3]
MC9S12C128CFA	XL09S/0M66G	-40˚C, 85˚C	48LQFP	25MHz	C128 die	128K	4K	31
MC9S12C128CPB	XL09S/0M66G	-40˚C, 85˚C	52LQFP	25MHz	C128 die	128K	4K	35
MC9S12C128CFU	XL09S/0M66G	-40˚C, 85˚C	80QFP	25MHz	C128 die	128K	4K	60
MC9S12C128VFA	XL09S/0M66G	-40˚C,105˚C	48LQFP	25MHz	C128 die	128K	4K	31
MC9S12C128VPB	XL09S/0M66G	-40˚C,105˚C	52LQFP	25MHz	C128 die	128K	4K	35
MC9S12C128VFU	XL09S/0M66G	-40˚C, 105˚C	80QFP	25MHz	C128 die	128K	4K	60
MC9S12C128MFA	XL09S/0M66G	-40˚C,125˚C	48LQFP	25MHz	C128 die	128K	4K	31
MC9S12C128MPB	XL09S/0M66G	-40˚C,125˚C	52LQFP	25MHz	C128 die	128K	4K	35
MC9S12C128MFU	XL09S/0M66G	-40˚C, 125˚C	80QFP	25MHz	C128 die	128K	4K	60
MC9S12C96CFA	XL09S/0M66G	-40˚C, 85˚C	48LQFP	25MHz	C128 die	96K	4K	31
MC9S12C96CPB	XL09S/0M66G	-40˚C, 85˚C	52LQFP	25MHz	C128 die	96K	4K	35
MC9S12C96CFU	XL09S/0M66G	-40˚C, 85˚C	80QFP	25MHz	C128 die	96K	4K	60
MC9S12C96VFA	XL09S/0M66G	-40˚C,105˚C	48LQFP	25MHz	C128 die	96K	4K	31
MC9S12C96VPB	XL09S/0M66G	-40˚C,105˚C	52LQFP	25MHz	C128 die	96K	4K	35
MC9S12C96VFU	XL09S/0M66G	-40˚C, 105˚C	80QFP	25MHz	C128 die	96K	4K	60
MC9S12C96MFA	XL09S/0M66G	-40˚C,125˚C	48LQFP	25MHz	C128 die	96K	4K	31
MC9S12C96MPB	XL09S/0M66G	-40˚C,125˚C	52LQFP	25MHz	C128 die	96K	4K	35
MC9S12C96MFU	XL09S/0M66G	-40˚C, 125˚C	80QFP	25MHz	C128 die	96K	4K	60
MC9S12C64CFA	XL09S/0M66G	-40˚C, 85˚C	48LQFP	25MHz	C128 die	64K	4K	31
MC9S12C64CPB	XL09S/0M66G	-40˚C, 85˚C	52LQFP	25MHz	C128 die	64K	4K	35

Part Number	Mask[1] set	Temp.	Package	Speed	Die Type	Flash	RAM	I/O[2], [3]
MC9S12GC32MFU	xL45J / xM34C	-40˚C, 125˚C	80QFP	25MHz	C32 die	32K	2K	60
MC9S12GC16CFA	xL45J / xM34C	-40˚C, 85˚C	48LQFP	25MHz	C32 die	16K	1K	31
MC9S12GC16CPB	xL45J / xM34C	-40˚C, 85˚C	52LQFP	25MHz	C32 die	16K	1K	35
MC9S12GC16CFU	xL45J / xM34C	-40˚C, 85˚C	80QFP	25MHz	C32 die	16K	1K	60
MC9S12GC16VFA	xL45J / xM34C	-40˚C,105˚C	48LQFP	25MHz	C32 die	16K	1K	31
MC9S12GC16VPB	xL45J / xM34C	-40˚C,105˚C	52LQFP	25MHz	C32 die	16K	1K	35
MC9S12GC16VFU	xL45J / xM34C	-40˚C, 105˚C	80QFP	25MHz	C32 die	16K	1K	60
MC9S12GC16MFA	xL45J / xM34C	-40˚C,125˚C	48LQFP	25MHz	C32 die	16K	1K	31
MC9S12GC16MPB	xL45J / xM34C	-40˚C,125˚C	52LQFP	25MHz	C32 die	16K	1K	35
MC9S12GC16MFU	xL45J / xM34C	-40˚C, 125˚C	80QFP	25MHz	C32 die	16K	1K	60

1. XL09S denotes all minor revisions of L09S maskset
   XL45J denotes all minor revisions of L45J maskset
   Maskset dependent errata can be accessed at
   http://e-www.motorola.com/wbapp/sps/site/prod_summary.jsp
2. All C-Family derivatives feature 1 CAN, 1 SCI, 1 SPI, an 8-channel A/D, a 6-channel PWM and an 8 channel timer. The GC-Family members do not have the CAN module
3. I/O is the sum of ports capable to act as digital input or output.