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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	HCS12
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, EBI/EMI, SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	60
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-QFP
Supplier Device Package	80-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s12c128cfue

1.3.2 Signal Properties Summary

Table 1-5. Signal Properties

Pin Name Function 1	Pin Name Function 2	Pin Name Function 3	Power Domain	Internal Pull Resistor		Description
				CTRL	Reset State	
EXTAL	—	—	V_{DDPLL}	NA	NA	Oscillator pins
XTAL	—	—	V_{DDPLL}	NA	NA	
$\overline{RESET}$	—	—	V_{DDX}	None	None	External reset pin
XFC	—	—	V_{DDPLL}	NA	NA	PLL loop filter pin
TEST	V_{PP}	—	V_{SSX}	NA	NA	Test pin only
BKGD	MODC	$\overline{TAGHI}$	V_{DDX}	Up	Up	Background debug, mode pin, tag signal high
PE7	NOACC	$\overline{XCLKS}$	V_{DDX}	PUCR	Up	Port E I/O pin, access, clock select
PE6	IPIPE1	MODB	V_{DDX}	While $\overline{RESET}$ pin is low: Down		Port E I/O pin and pipe status
PE5	IPIPE0	MODA	V_{DDX}	While $\overline{RESET}$ pin is low: Down		Port E I/O pin and pipe status
PE4	ECLK	—	V_{DDX}	PUCR	Mode Dep(1)	Port E I/O pin, bus clock output
PE3	LSTRB	$\overline{TAGLO}$	V_{DDX}	PUCR	Mode Dep[1]	Port E I/O pin, low strobe, tag signal low
PE2	R/$\overline{W}$	—	V_{DDX}	PUCR	Mode Dep[1]	Port E I/O pin, R/$\overline{W}$ in expanded modes
PE1	$\overline{IRQ}$	—	V_{DDX}	PUCR	Up	Port E input, external interrupt pin
PE0	$\overline{XIRQ}$	—	V_{DDX}	PUCR	Up	Port E input, non-maskable interrupt pin
PA[7:3]	ADDR[15:1]/ DATA[15:1]	—	V_{DDX}	PUCR	Disabled	Port A I/O pin and multiplexed address/data
PA[2:1]	ADDR[10:9]/ DATA[10:9]	—	V_{DDX}	PUCR	Disabled	Port A I/O pin and multiplexed address/data
PA[0]	ADDR[8]/ DATA[8]	—	V_{DDX}	PUCR	Disabled	Port A I/O pin and multiplexed address/data
PB[7:5]	ADDR[7:5]/ DATA[7:5]	—	V_{DDX}	PUCR	Disabled	Port B I/O pin and multiplexed address/data
PB[4]	ADDR[4]/ DATA[4]	—	V_{DDX}	PUCR	Disabled	Port B I/O pin and multiplexed address/data
PB[3:0]	ADDR[3:0]/ DATA[3:0]	—	V_{DDX}	PUCR	Disabled	Port B I/O pin and multiplexed address/data
PAD[7:0]	AN[7:0]	—	V_{DDA}	PERAD/P PSAD	Disabled	Port AD I/O pins and ATD inputs
PP[7]	KWP[7]	—	V_{DDX}	PERP/ PPSP	Disabled	Port P I/O pins and keypad wake-up
PP[6]	KWP[6]	ROMCTL	V_{DDX}	PERP/ PPSP	Disabled	Port P I/O pins, keypad wake-up, and ROMON enable.
PP[5]	KWP[5]	PW5	V_{DDX}	PERP/ PPSP	Disabled	Port P I/O pin, keypad wake-up, PW5 output
PP[4:3]	KWP[4:3]	PW[4:3]	V_{DDX}	PERP/ PPSP	Disabled	Port P I/O pin, keypad wake-up, PWM output

1.3.4.27 PS[3:2] — Port S I/O Pins [3:2]

PS3 and PS2 are general purpose input or output pins. These pins are not available in the 48- / 52-pin package versions.

1.3.4.28 PS1 / TXD — Port S I/O Pin 1

PS1 is a general purpose input or output pin and the transmit pin, TXD, of serial communication interface (SCI).

1.3.4.29 PS0 / RXD — Port S I/O Pin 0

PS0 is a general purpose input or output pin and the receive pin, RXD, of serial communication interface (SCI).

1.3.4.30 PT[7:5] / IOC[7:5] — Port T I/O Pins [7:5]

PT7–PT5 are general purpose input or output pins. They can also be configured as the timer system input capture or output compare pins IOC7-IOC5.

1.3.4.31 PT[4:0] / IOC[4:0] / PW[4:0]— Port T I/O Pins [4:0]

PT4–PT0 are general purpose input or output pins. They can also be configured as the timer system input capture or output compare pins IOC[n] or as the PWM outputs PW[n].

1.3.5 Power Supply Pins

1.3.5.1 V_{DDX},V_{SSX} — Power and Ground Pins for I/O Drivers

External power and ground for I/O drivers. Bypass requirements depend on how heavily the MCU pins are loaded.

1.3.5.2 V_{DDR}, V_{SSR} — Power and Ground Pins for I/O Drivers and for Internal Voltage Regulator

External power and ground for the internal voltage regulator. Connecting V_{DDR} to ground disables the internal voltage regulator.

1.3.5.3 V_{DD1}, V_{DD2}, V_{SS1}, V_{SS2} — Internal Logic Power Pins

Power is supplied to the MCU through V_{DD} and V_{SS}. This 2.5V supply is derived from the internal voltage regulator. There is no static load on those pins allowed. The internal voltage regulator is turned off, if V_{DDR} is tied to ground.

A valid edge on input is detected if 4 consecutive samples of a passive level are followed by 4 consecutive samples of an active level directly or indirectly.

The filters are continuously clocked by the bus clock in RUN and WAIT mode. In STOP mode the clock is generated by a single RC oscillator in the Port Integration Module. To maximize current saving the RC oscillator runs only if the following condition is true on any pin:

Sample count <= 4 and port interrupt enabled (PIE=1) and port interrupt flag not set (PIF=0).

2.4.2.6 Port J

In all modes, port J pins PJ[7:6] can be used for general purpose I/O or interrupt driven general purpose I/O's. During reset, port J pins are configured as inputs.

Port J offers 2 I/O ports with the same interrupt features as on port P.

2.4.3 Port A, B, E and BKGD Pin

All port and pin logic is located in the core module. Please *refer to S12_mebi Block User Guide for details.*

2.4.4 External Pin Descriptions

All ports start up as general purpose inputs on reset.

2.4.5 Low Power Options

2.4.5.1 Run Mode

No low power options exist for this module in run mode.

2.4.5.2 Wait Mode

No low power options exist for this module in wait mode.

2.4.5.3 Stop Mode

All clocks are stopped. There are asynchronous paths to generate interrupts from STOP on port P and J.

2.5 Initialization Information

The reset values of all registers are given in Section 2.3.2, "Register Descriptions".

2.5.1 Reset Initialization

All registers including the data registers get set/reset asynchronously. Table 2-39 summarizes the port properties after reset initialization.

3.1.1 Features

- Registers for mapping of address space for on-chip RAM, EEPROM, and FLASH (or ROM) memory blocks and associated registers
- Memory mapping control and selection based upon address decode and system operating mode
- Core address bus control
- Core data bus control and multiplexing
- Core security state decoding
- Emulation chip select signal generation ($\overline{\text{ECS}}$)
- External chip select signal generation ($\overline{\text{XCS}}$)
- Internal memory expansion
- External stretch and ROM mapping control functions via the MISC register
- Reserved registers for test purposes
- Configurable system memory options defined at integration of core into the system-on-a-chip (SoC).

3.1.2 Modes of Operation

Some of the registers operate differently depending on the mode of operation (i.e., normal expanded wide, special single chip, etc.). This is best understood from the register descriptions.

3.2 External Signal Description

All interfacing with the MMC sub-block is done within the core, it has no external signals.

3.3 Memory Map and Register Definition

A summary of the registers associated with the MMC sub-block is shown in Figure 3-2. Detailed descriptions of the registers and bits are given in the subsections that follow.

3.3.1 Module Memory Map

Table 3-1. MMC Memory Map

Address Offset	Register	Access
0x0010	Initialization of Internal RAM Position Register (INITRM)	R/W
0x0011	Initialization of Internal Registers Position Register (INITRG)	R/W
0x0012	Initialization of Internal EEPROM Position Register (INITEE)	R/W
0x0013	Miscellaneous System Control Register (MISC)	R/W
0x0014	Reserved	—
. .	. .	—

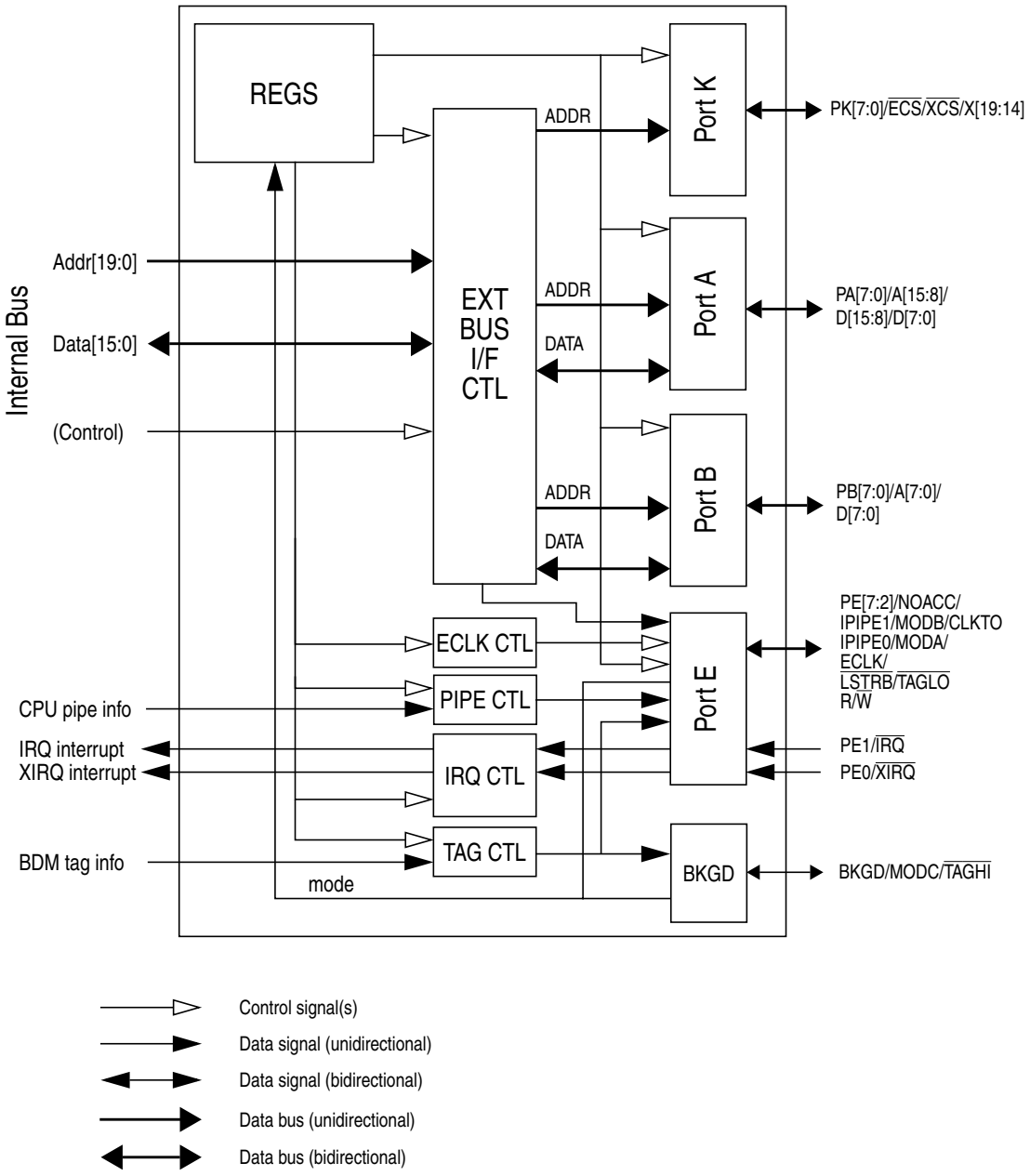

Figure 4-1. MEBI Block Diagram

4.4.3.2 Special Operating Modes

There are two special operating modes that correspond to normal operating modes. These operating modes are commonly used in factory testing and system development.

4.4.3.2.1 Special Single-Chip Mode

When the MCU is reset in this mode, the background debug mode is enabled and active. The MCU does not fetch the reset vector and execute application code as it would in other modes. Instead the active background mode is in control of CPU execution and BDM firmware is waiting for additional serial commands through the BKGD pin. When a serial command instructs the MCU to return to normal execution, the system will be configured as described below unless the reset states of internal control registers have been changed through background commands after the MCU was reset.

There is no external expansion bus after reset in this mode. Ports A and B are initially simple bidirectional I/O pins that are configured as high-impedance inputs with internal pull resistors disabled; however, writing to the mode select bits in the MODE register (which is allowed in special modes) can change this after reset. All of the Port E pins (except PE4/ECLK) are initially configured as general purpose high-impedance inputs with internal pull resistors enabled. PE4/ECLK is configured as the E clock output in this mode.

The pins associated with Port E bits 6, 5, 3, and 2 cannot be configured for their alternate functions IPIPE1, IPIPE0, $\overline{\text{LSTRB}}$, and R/$\overline{\text{W}}$ while the MCU is in single chip modes. In single chip modes, the associated control bits PIPOE, LSTRE and RDWE are reset to zero. Writing the opposite value into these bits in single chip mode does not change the operation of the associated Port E pins.

Port E, bit 4 can be configured for a free-running E clock output by clearing NECLK=0. Typically the only use for an E clock output while the MCU is in single chip modes would be to get a constant speed clock for use in the external application system.

4.4.3.2.2 Special Test Mode

In expanded wide modes, Ports A and B are configured as a 16-bit multiplexed address and data bus and Port E provides bus control and status signals. In special test mode, the write protection of many control bits is lifted so that they can be thoroughly tested without needing to go through reset.

4.4.3.3 Test Operating Mode

There is a test operating mode in which an external master, such as an I.C. tester, can control the on-chip peripherals.

4.4.3.3.1 Peripheral Mode

This mode is intended for factory testing of the MCU. In this mode, the CPU is inactive and an external (tester) bus master drives address, data and bus control signals in through Ports A, B and E. In effect, the whole MCU acts as if it was a peripheral under control of an external CPU. This allows faster testing of on-chip memory and peripherals than previous testing methods. Since the mode control register is not accessible in peripheral mode, the only way to change to another mode is to reset the MCU into a different

Chapter 7
Debug Module (DBGV1) Block Description

7.1 Introduction

This section describes the functionality of the debug (DBG) sub-block of the HCS12 core platform.

The DBG module is designed to be fully compatible with the existing BKP_HCS12_A module (BKP mode) and furthermore provides an on-chip trace buffer with flexible triggering capability (DBG mode). The DBG module provides for non-intrusive debug of application software. The DBG module is optimized for the HCS12 16-bit architecture.

7.1.1 Features

The DBG module in BKP mode includes these distinctive features:

- Full or dual breakpoint mode
  - Compare on address and data (full)
  - Compare on either of two addresses (dual)
- BDM or SWI breakpoint
  - Enter BDM on breakpoint (BDM)
  - Execute SWI on breakpoint (SWI)
- Tagged or forced breakpoint
  - Break just before a specific instruction will begin execution (TAG)
  - Break on the first instruction boundary after a match occurs (Force)
- Single, range, or page address compares
  - Compare on address (single)
  - Compare on address 256 byte (range)
  - Compare on any 16K page (page)
- At forced breakpoints compare address on read or write
- High and/or low byte data compares
- Comparator C can provide an additional tag or force breakpoint (enhancement for BKP mode)

Name[1]		Bit 7	6	5	4	3	2	1	Bit 0
0x0022 DBGTBH	R	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
	W								
0x0023 DBGTBL	R	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	W								
0x0024 DBGCNT	R	TBF	0	CNT					
	W								
0x0025 DBGCCX[(2)]	R	PAGSEL		EXTCMP					
	W								
0x0026 DBGCCH[2]	R	Bit 15	14	13	12	11	10	9	Bit 8
	W								
0x0027 DBGCCL[2]	R	Bit 7	6	5	4	3	2	1	Bit 0
	W								
0x0028 DBGC2 BKPCT0	R	BKABEN	FULL	BDM	TAGAB	BKCEN	TAGC	RWCEN	RWC
	W								
0x0029 DBGC3 BKPCT1	R	BKAMBH	BKAMBL	BKBMBH	BKBMBL	RWAEN	RWA	RWBEN	RWB
	W								
0x002A DBGCAX BKP0X	R	PAGSEL		EXTCMP					
	W								
0x002B DBGCAH BKP0H	R	Bit 15	14	13	12	11	10	9	Bit 8
	W								
0x002C DBGCAL BKP0L	R	Bit 7	6	5	4	3	2	1	Bit 0
	W								
0x002D DBGCBX BKP1X	R	PAGSEL		EXTCMP					
	W								
0x002E DBGCBH BKP1H	R	Bit 15	14	13	12	11	10	9	Bit 8
	W								
0x002F DBGCBL BKP1L	R	Bit 7	6	5	4	3	2	1	Bit 0
	W								

= Unimplemented or Reserved

Figure 7-3. DBG Register Summary (continued)

8.5.1.3 Step 3

Configure how many conversions you want to perform in one sequence and define other settings in ATDCTL3.

Example: Write S4C=1 to do 4 conversions per sequence.

8.5.1.4 Step 4

Configure resolution, sampling time and ATD clock speed in ATDCTL4.

Example: Use default for resolution and sampling time by leaving SRES8, SMP1 and SMP0 clear. For a bus clock of 40MHz write 9 to PR4-0, this gives an ATD clock of 0.5*40MHz/(9+1) = 2MHz which is within the allowed range for f_{ATDCLK}.

8.5.1.5 Step 5

Configure starting channel, single/multiple channel, continuous or single sequence and result data format in ATDCTL5. Writing ATDCTL5 will start the conversion, so make sure your write ATDCTL5 in the last step.

Example: Leave CC,CB,CA clear to start on channel AN0. Write MULT=1 to convert channel AN0 to AN3 in a sequence (4 conversion per sequence selected in ATDCTL3).

8.5.2 Aborting an A/D conversion

8.5.2.1 Step 1

Disable the ATD Interrupt by writing ASCIE=0 in ATDCTL2. This will also abort any ongoing conversion sequence.

It is important to clear the interrupt enable at this point, prior to step 3, as depending on the device clock gating it may not always be possible to clear it or the SCF flag once the module is disabled (ADPU=0).

8.5.2.2 Step 2

Clear the SCF flag by writing a 1 in ATDSTAT0.

(Remaining flags will be cleared with the next start of a conversions, but SCF flag should be cleared to avoid SCF interrupt.)

8.5.2.3 Step 3

Power down ATD by writing ADPU=0 in ATDCTL2.

8.6 Resets

At reset the ATD10B8C is in a power down state. The reset state of each individual bit is listed within Section 8.3.2, “Register Descriptions” which details the registers and their bit-field.

Table 9-6. RTICTL Field Descriptions

Field	Description
6:4 RTR[6:4]	**Real-Time Interrupt Prescale Rate Select Bits** — These bits select the prescale rate for the RTI. See Table 9-7.
3:0 RTR[3:0]	**Real-Time Interrupt Modulus Counter Select Bits** — These bits select the modulus counter target value to provide additional granularity. Table 9-7 shows all possible divide values selectable by the RTICTL register. The source clock for the RTI is OSCCLK.

Table 9-7. RTI Frequency Divide Rates

RTR[3:0]	RTR[6:4] =							
	000 (OFF)	**001 (2^{10})**	**010 (2^{11})**	**011 (2^{12})**	**100 (2^{13})**	**101 (2^{14})**	**110 (2^{15})**	**111 (2^{16})**
0000 (÷1)	OFF*	2^{10}	2^{11}	2^{12}	2^{13}	2^{14}	2^{15}	2^{16}
0001 (÷2)	OFF*	$2x2^{10}$	$2x2^{11}$	$2x2^{12}$	$2x2^{13}$	$2x2^{14}$	$2x2^{15}$	$2x2^{16}$
0010 (÷3)	OFF*	$3x2^{10}$	$3x2^{11}$	$3x2^{12}$	$3x2^{13}$	$3x2^{14}$	$3x2^{15}$	$3x2^{16}$
0011 (÷4)	OFF*	$4x2^{10}$	$4x2^{11}$	$4x2^{12}$	$4x2^{13}$	$4x2^{14}$	$4x2^{15}$	$4x2^{16}$
0100 (÷5)	OFF*	$5x2^{10}$	$5x2^{11}$	$5x2^{12}$	$5x2^{13}$	$5x2^{14}$	$5x2^{15}$	$5x2^{16}$
0101 (÷6)	OFF*	$6x2^{10}$	$6x2^{11}$	$6x2^{12}$	$6x2^{13}$	$6x2^{14}$	$6x2^{15}$	$6x2^{16}$
0110 (÷7)	OFF*	$7x2^{10}$	$7x2^{11}$	$7x2^{12}$	$7x2^{13}$	$7x2^{14}$	$7x2^{15}$	$7x2^{16}$
0111 (÷8)	OFF*	$8x2^{10}$	$8x2^{11}$	$8x2^{12}$	$8x2^{13}$	$8x2^{14}$	$8x2^{15}$	$8x2^{16}$
1000 (÷9)	OFF*	$9x2^{10}$	$9x2^{11}$	$9x2^{12}$	$9x2^{13}$	$9x2^{14}$	$9x2^{15}$	$9x2^{16}$
1001 (÷10)	OFF*	$10x2^{10}$	$10x2^{11}$	$10x2^{12}$	$10x2^{13}$	$10x2^{14}$	$10x2^{15}$	$10x2^{16}$
1010 (÷11)	OFF*	$11x2^{10}$	$11x2^{11}$	$11x2^{12}$	$11x2^{13}$	$11x2^{14}$	$11x2^{15}$	$11x2^{16}$
1011 (÷12)	OFF*	$12x2^{10}$	$12x2^{11}$	$12x2^{12}$	$12x2^{13}$	$12x2^{14}$	$12x2^{15}$	$12x2^{16}$
1100 (÷ 13)	OFF*	$13x2^{10}$	$13x2^{11}$	$13x2^{12}$	$13x2^{13}$	$13x2^{14}$	$13x2^{15}$	$13x2^{16}$
1101 (÷14)	OFF*	$14x2^{10}$	$14x2^{11}$	$14x2^{12}$	$14x2^{13}$	$14x2^{14}$	$14x2^{15}$	$14x2^{16}$
1110 (÷15)	OFF*	$15x2^{10}$	$15x2^{11}$	$15x2^{12}$	$15x2^{13}$	$15x2^{14}$	$15x2^{15}$	$15x2^{16}$
1111 (÷ 16)	OFF*	$16x2^{10}$	$16x2^{11}$	$16x2^{12}$	$16x2^{13}$	$16x2^{14}$	$16x2^{15}$	$16x2^{16}$

* Denotes the default value out of reset.This value should be used to disable the RTI to ensure future backwards compatibility.

10.4.7.1 Description of Interrupt Operation

The MSCAN supports four interrupt vectors (see Table 10-36), any of which can be individually masked (for details see sections from Section 10.3.2.6, "MSCAN Receiver Interrupt Enable Register (CANRIER)," to Section 10.3.2.8, "MSCAN Transmitter Interrupt Enable Register (CANTIER)").

NOTE

The dedicated interrupt vector addresses are defined in the Resets and Interrupts chapter.

Table 10-36. Interrupt Vectors

Interrupt Source	CCR Mask	Local Enable
Wake-Up Interrupt (WUPIF)	I bit	CANRIER (WUPIE)
Error Interrupts Interrupt (CSCIF, OVRIF)	I bit	CANRIER (CSCIE, OVRIE)
Receive Interrupt (RXF)	I bit	CANRIER (RXFIE)
Transmit Interrupts (TXE[2:0])	I bit	CANTIER (TXEIE[2:0])

10.4.7.2 Transmit Interrupt

At least one of the three transmit buffers is empty (not scheduled) and can be loaded to schedule a message for transmission. The TXEx flag of the empty message buffer is set.

10.4.7.3 Receive Interrupt

A message is successfully received and shifted into the foreground buffer (RxFG) of the receiver FIFO. This interrupt is generated immediately after receiving the EOF symbol. The RXF flag is set. If there are multiple messages in the receiver FIFO, the RXF flag is set as soon as the next message is shifted to the foreground buffer.

10.4.7.4 Wake-Up Interrupt

A wake-up interrupt is generated if activity on the CAN bus occurs during MSCN internal sleep mode. WUPE (see Section 10.3.2.1, "MSCAN Control Register 0 (CANCTL0)") must be enabled.

10.4.7.5 Error Interrupt

An error interrupt is generated if an overrun of the receiver FIFO, error, warning, or bus-off condition occurrs. Section 10.3.2.5, "MSCAN Receiver Flag Register (CANRFLG) indicates one of the following conditions:

- **Overrun** — An overrun condition of the receiver FIFO as described in Section 10.4.2.3, "Receive Structures," occurred.
- **CAN Status Change** — The actual value of the transmit and receive error counters control the CAN bus state of the MSCAN. As soon as the error counters skip into a critical range (Tx/Rx-warning, Tx/Rx-error, bus-off) the MSCAN flags an error condition. The status change, which caused the error condition, is indicated by the TSTAT and RSTAT flags (see Section 10.3.2.5,

In Figure 13-16, a large burst of noise is perceived as the beginning of a start bit, although the test sample at RT5 is high. The RT5 sample sets the noise flag. Although this is a worst-case misalignment of perceived bit time, the data samples RT8, RT9, and RT10 are within the bit time and data recovery is successful.

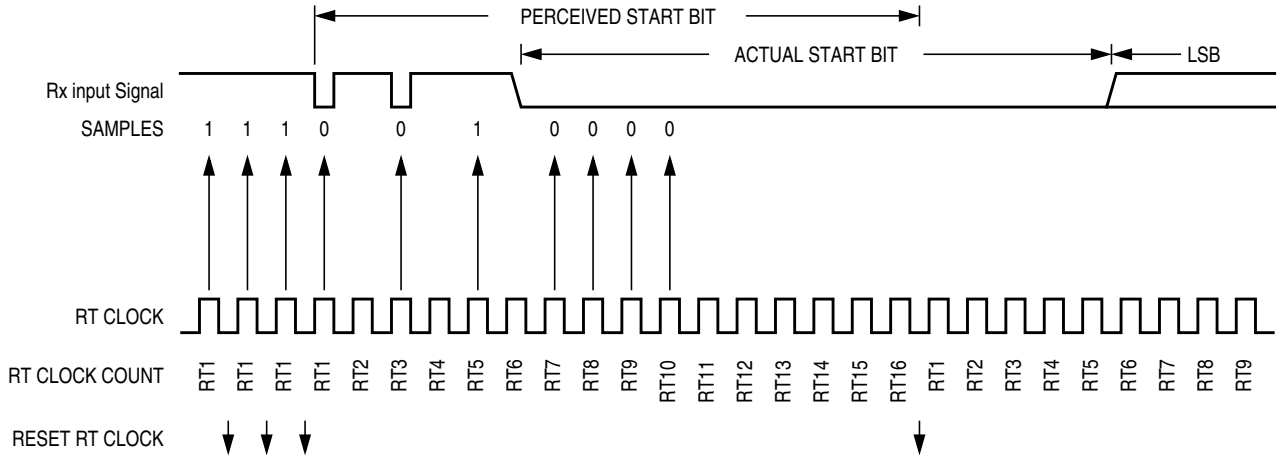

Figure 13-16. Start Bit Search Example 3

Figure 13-17 shows the effect of noise early in the start bit time. Although this noise does not affect proper synchronization with the start bit time, it does set the noise flag.

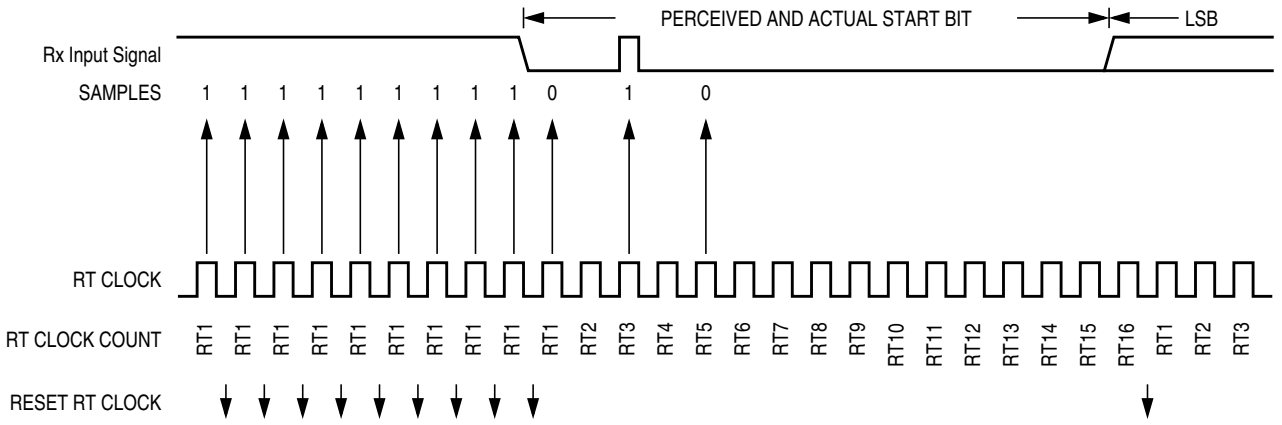

Figure 13-17. Start Bit Search Example 4

Table 14-7. Example SPI Baud Rate Selection (25 MHz Bus Clock) (continued)

SPPR2	SPPR1	SPPR0	SPR2	SPR1	SPR0	Baud Rate Divisor	Baud Rate
1	0	0	1	1	1	1280	19.53 kHz
1	0	1	0	0	0	12	2.08333 MHz
1	0	1	0	0	1	24	1.04167 MHz
1	0	1	0	1	0	48	520.83 kHz
1	0	1	0	1	1	96	260.42 kHz
1	0	1	1	0	0	192	130.21 kHz
1	0	1	1	0	1	384	65.10 kHz
1	0	1	1	1	0	768	32.55 kHz
1	0	1	1	1	1	1536	16.28 kHz
1	1	0	0	0	0	14	1.78571 MHz
1	1	0	0	0	1	28	892.86 kHz
1	1	0	0	1	0	56	446.43 kHz
1	1	0	0	1	1	112	223.21 kHz
1	1	0	1	0	0	224	111.61 kHz
1	1	0	1	0	1	448	55.80 kHz
1	1	0	1	1	0	896	27.90 kHz
1	1	0	1	1	1	1792	13.95 kHz
1	1	1	0	0	0	16	1.5625 MHz
1	1	1	0	0	1	32	781.25 kHz
1	1	1	0	1	0	64	390.63 kHz
1	1	1	0	1	1	128	195.31 kHz
1	1	1	1	0	0	256	97.66 kHz
1	1	1	1	0	1	512	48.83 kHz
1	1	1	1	1	0	1024	24.41 kHz
1	1	1	1	1	1	2048	12.21 kHz

NOTE

In slave mode of SPI S-clock speed DIV2 is not supported.

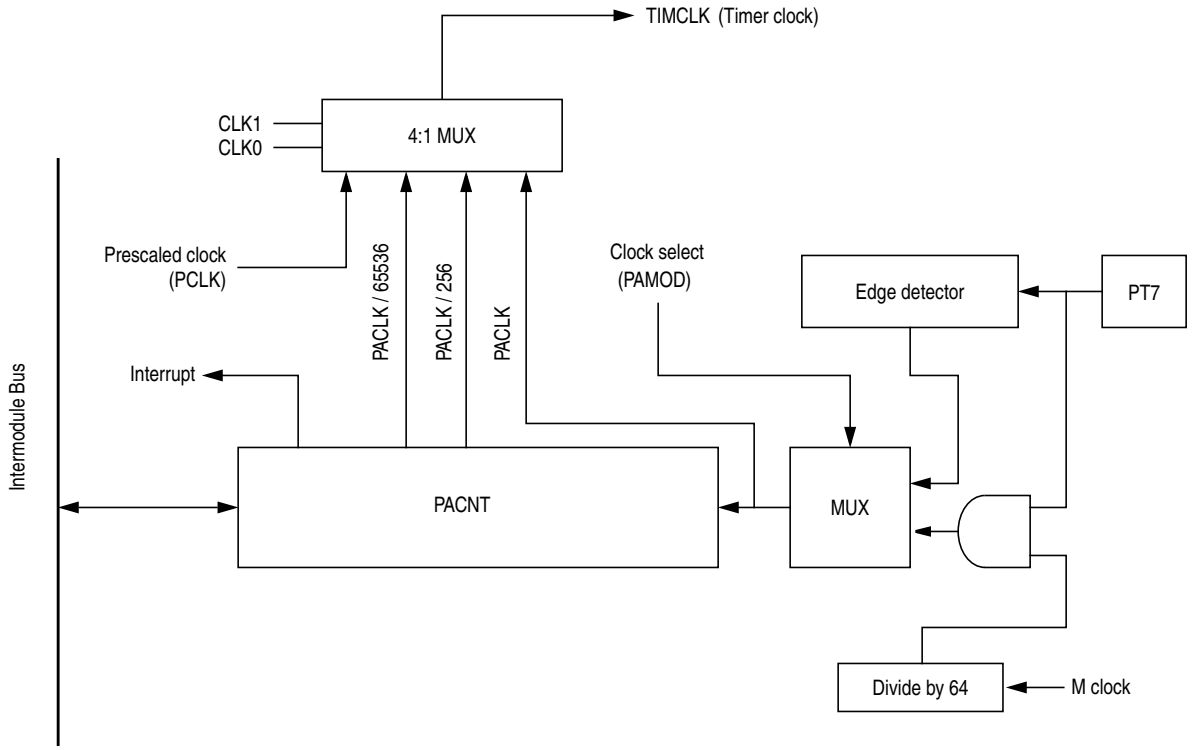

Figure 15-2. 16-Bit Pulse Accumulator Block Diagram

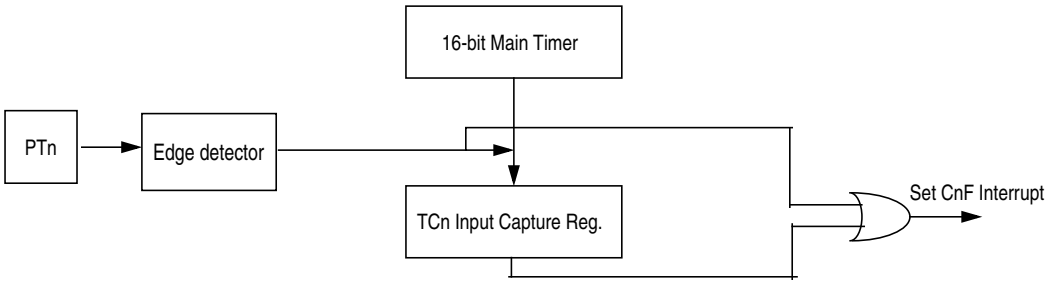

Figure 15-3. Interrupt Flag Setting

15.2.6 IOC2 — Input Capture and Output Compare Channel 2 Pin

This pin serves as input capture or output compare for channel 2.

15.2.7 IOC1 — Input Capture and Output Compare Channel 1 Pin

This pin serves as input capture or output compare for channel 1.

15.2.8 IOC0 — Input Capture and Output Compare Channel 0 Pin

This pin serves as input capture or output compare for channel 0.

NOTE

For the description of interrupts see Section 15.6, “Interrupts”.

15.3 Memory Map and Register Definition

This section provides a detailed description of all memory and registers.

15.3.1 Module Memory Map

The memory map for the TIM16B8CV1 module is given below in Table 15-2. The address listed for each register is the address offset. The total address for each register is the sum of the base address for the TIM16B8CV1 module and the address offset for each register.

15.4.6 Gated Time Accumulation Mode

Setting the PAMOD bit configures the pulse accumulator for gated time accumulation operation. An active level on the PACNT input pin enables a divided-by-64 clock to drive the pulse accumulator. The PEDGE bit selects low levels or high levels to enable the divided-by-64 clock.

The trailing edge of the active level at the IOC7 pin sets the PAIF. The PAI bit enables the PAIF flag to generate interrupt requests.

The pulse accumulator counter register reflect the number of pulses from the divided-by-64 clock since the last reset.

NOTE

The timer prescaler generates the divided-by-64 clock. If the timer is not active, there is no divided-by-64 clock.

15.5 Resets

The reset state of each individual bit is listed within Section 15.3, “Memory Map and Register Definition” which details the registers and their bit fields.

15.6 Interrupts

This section describes interrupts originated by the TIM16B8CV1 block. Table 15-23 lists the interrupts generated by the TIM16B8CV1 to communicate with the MCU.

Table 15-23. TIM16B8CV1 Interrupts

Interrupt	Offset (1)	Vector[1]	Priority[1]	Source	Description
C[7:0]F	—	—	—	Timer Channel 7–0	Active high timer channel interrupts 7–0
PAOVI	—	—	—	Pulse Accumulator Input	Active high pulse accumulator input interrupt
PAOVF	—	—	—	Pulse Accumulator Overflow	Pulse accumulator overflow interrupt
TOF	—	—	—	Timer Overflow	Timer Overflow interrupt

1. Chip Dependent.

The TIM16B8CV1 uses a total of 11 interrupt vectors. The interrupt vector offsets and interrupt numbers are chip dependent.

15.6.1 Channel [7:0] Interrupt (C[7:0]F)

This active high outputs will be asserted by the module to request a timer channel 7 – 0 interrupt to be serviced by the system controller.

19.1.3 Modes of Operation

See Section 19.4.2, “Operating Modes” for a description of the Flash module operating modes. For program and erase operations, refer to Section 19.4.1, “Flash Command Operations”.

19.1.4 Block Diagram

Figure 19-1Figure 19-2 shows a block diagram of the FTS128K1FTS64K module.

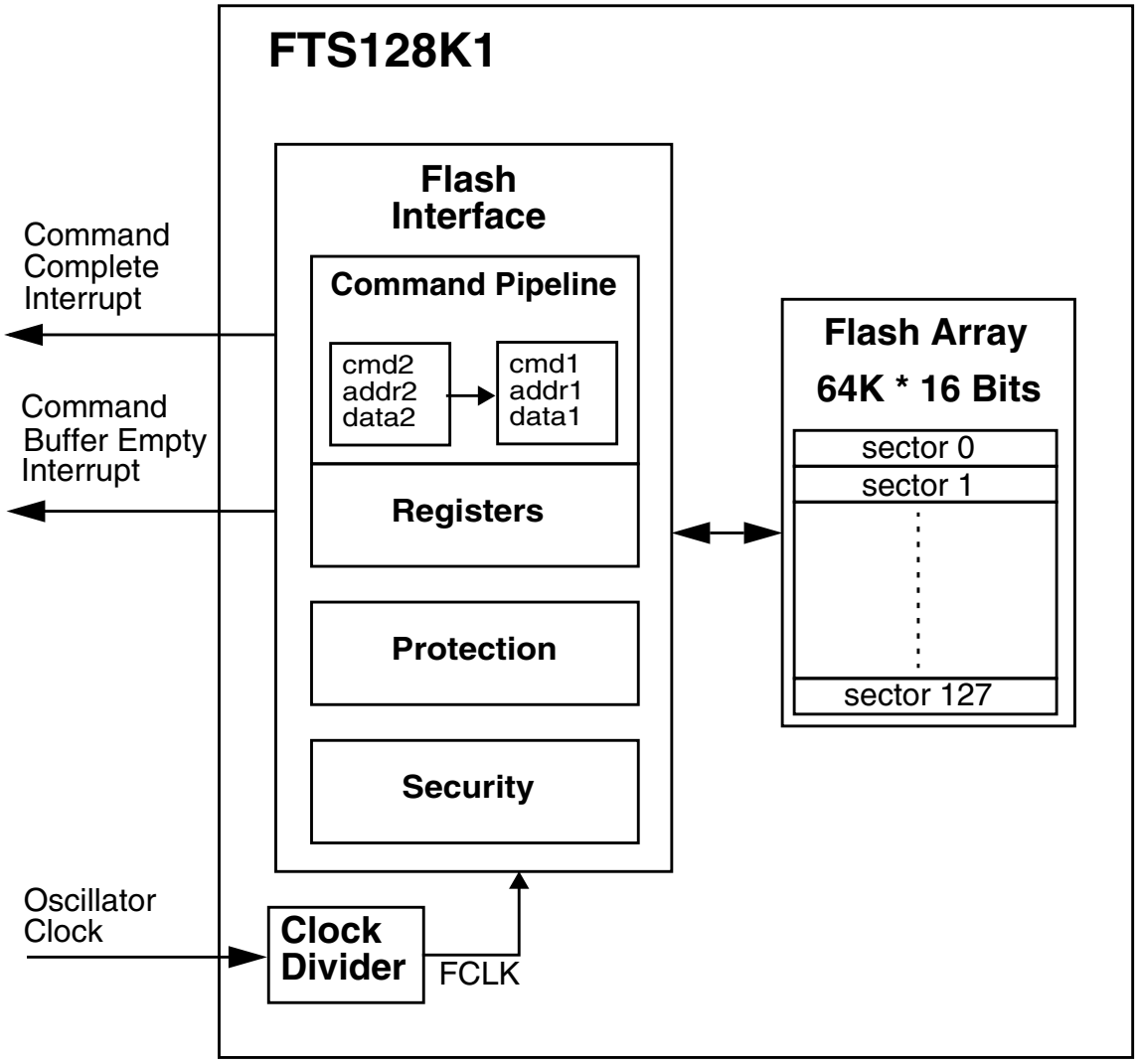

Figure 19-1. FTS128K1 Block Diagram

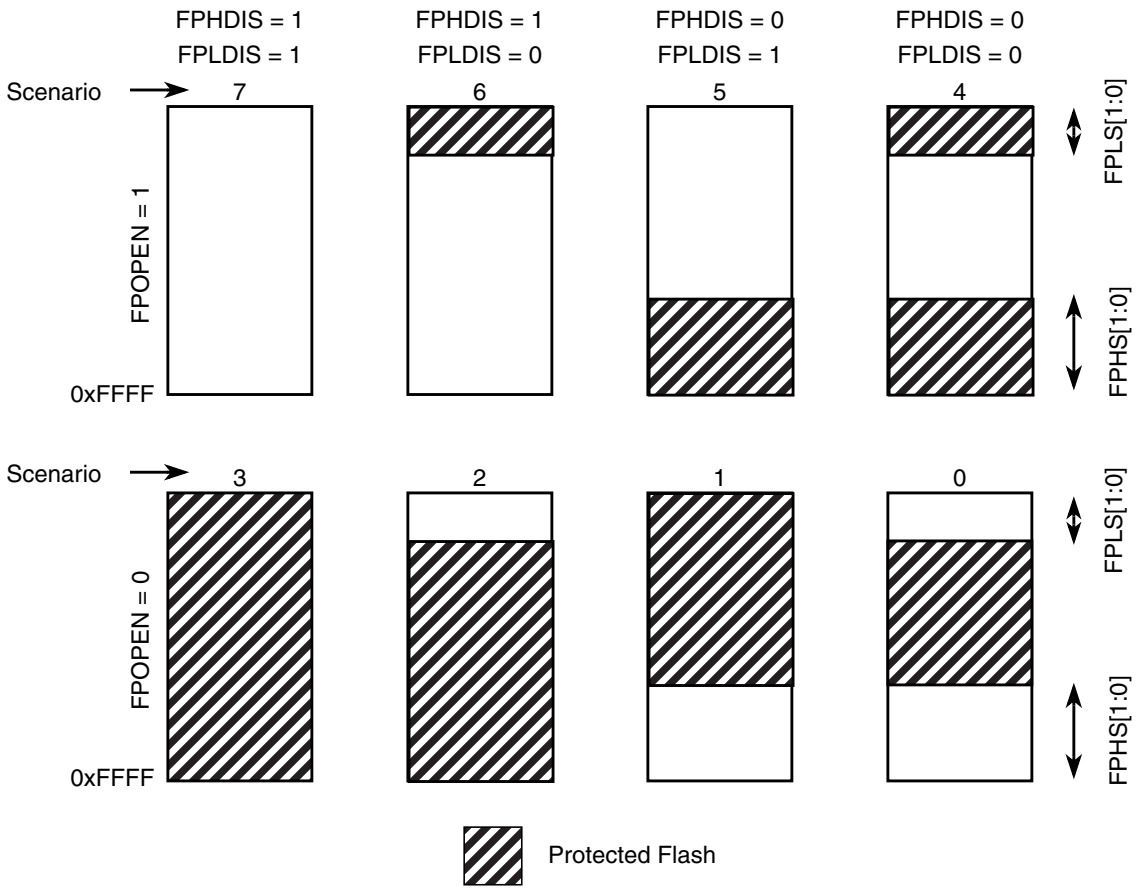

Figure 19-11. Flash Protection Scenarios

19.3.2.5.1 Flash Protection Restrictions

The general guideline is that protection can only be added, not removed. All valid transitions between Flash protection scenarios are specified in Table 19-13. Any attempt to write an invalid scenario to the FPROT register will be ignored and the FPROT register will remain unchanged. The contents of the FPROT register reflect the active protection scenario.

Table 19-13. Flash Protection Scenario Transitions

From Protection Scenario	To Protection Scenario[1]							
	0	1	2	3	4	5	6	7
0	X	X	X	X				
1		X		X				
2			X	X				
3				X				
4				X	X			
5			X	X	X	X		

A.2.2 ATD Operating Characteristics In 3.3V Range

The Table A-11 shows conditions under which the ATD operates.

The following constraints exist to obtain full-scale, full range results: $V_{SSA} \le V_{RL} \le V_{IN} \le V_{RH} \le V_{DDA}$. This constraint exists since the sample buffer amplifier can not drive beyond the power supply levels that it ties to. If the input level goes outside of this range it will effectively be clipped

Table A-11. ATD Operating Characteristics

Conditions are shown in Table A-4 unless otherwise noted; Supply Voltage 3.3V-10% <= V_{DDA} <= 3.3V+10%							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	D	Reference Potential Low High	 V_{RL} V_{RH}	 V_{SSA} $V_{DDA}/2$	 — —	 $V_{DDA}/2$ V_{DDA}	 V V
2	C	Differential Reference Voltage	V_{RH}-V_{RL}	3.0	3.3	3.6	V
3	D	ATD Clock Frequency	f_{ATDCLK}	0.5	—	2.0	MHz
4	D	ATD 10-Bit Conversion Period Clock Cycles(1) Conv, Time at 2.0MHz ATD Clock f_{ATDCLK}	 N_{CONV10} T_{CONV10}	 14 7	 — —	 28 14	 Cycles µs
5	D	ATD 8-Bit Conversion Period Clock Cycles1 Conv, Time at 2.0MHz ATD Clock f_{ATDCLK}	 N_{CONV8} T_{CONV8}	 12 6	 — —	 26 13	 Cycles µs
6	D	Recovery Time (V_{DDA}=3.3 Volts)	t_{REC}	—	—	20	µs
7	P	Reference Supply current	I_{REF}	—	—	0.250	mA

1. The minimum time assumes a final sample period of 2 ATD clocks cycles while the maximum time assumes a final sample period of 16 ATD clocks.

A.2.3 Factors Influencing Accuracy

Three factors — source resistance, source capacitance and current injection — have an influence on the accuracy of the ATD.

A.2.3.1 Source Resistance

Due to the input pin leakage current as specified in Table A-6 in conjunction with the source resistance there will be a voltage drop from the signal source to the ATD input. The maximum source resistance R_S specifies results in an error of less than 1/2 LSB (2.5mV) at the maximum leakage current. If device or operating conditions are less than worst case or leakage-induced error is acceptable, larger values of source resistance is allowable.

A.2.3.2 Source Capacitance

When sampling an additional internal capacitor is switched to the input. This can cause a voltage drop due to charge sharing with the external and the pin capacitance. For a maximum sampling error of the input voltage ≤ 1LSB, then the external filter capacitor, $C_f \ge 1024 * (C_{INS} - C_{INN})$.