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Details

Product Status	Active
Core Processor	HCS12
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, EBI/EMI, SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	35
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	52-LQFP
Supplier Device Package	52-QFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s12c128cpbe

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A full list of family members and options is included in the appendices.

The following revision history table summarizes changes contained in this document.

This document contains information for all constituent modules, with the exception of the S12 CPU. For S12 CPU information please refer to the CPU S12 Reference Manual.

Revision History

Date	Revision Level	Description
June, 2005	01.14	New Book
July, 2005	01.15	Removed 16MHz option for 128K, 96K and 64K versions Minor corrections following review
Oct, 2005	01.16	Added outstanding flash module descriptions Added EPP package options Corrected and Enhanced recommended PCB layouts
Dec, 2005	01.17	Added note to PIM block diagram figure
Dec, 2005	01.18	Added PIM rerouting information to 80-pin package diagram
Jan, 2006	01.19	Modified LVI levels in electrical parameter section Corrected TSCR2 typo in timer register listing
Mar, 2006	01.20	Cleaned up Device Overview Section
May, 2006	01.21	Added 0M66G to PartID table Added units to MSCAN timing parameter table Corrected missing overbars on pin names
Dec, 2006	01.22	Corrected CRGFLG contents in register summary Removed non existing part number options Removed unintended symbol fonts from table A6
May, 2007	01.23	Updated ATD section Corrected typos
May, 2010	01.24	Updated TIM section



when mapping PWM channels to Port T in an 80QFP option, the associated PWM channels are then mapped to both Port P and Port T.



2.3.2.1.4 Port T Reduced Drive Register (RDRT)



Read: Anytime.

Write: Anytime.

Table 2-6. RDRT Field Descriptions

Field	Description
7–0 RDRT[7:0]	 Reduced Drive Port T — This register configures the drive strength of each port T output pin as either full or reduced. If the port is used as input this bit is ignored. Full drive strength at output. Associated pin drives at about 1/3 of the full drive strength.

2.3.2.1.5 Port T Pull Device Enable Register (PERT)

Module Base + 0x0004

	7	6	5	4	3	2	1	0
R W	PERT7	PERT6	PERT5	PERT4	PERT3	PERT2	PERT1	PERT0
Reset	0	0	0	0	0	0	0	0

Figure 2-7. Port T Pull Device Enable Register (PERT)

Read: Anytime.

Write: Anytime.

Table 2-7. PERT Field Descriptions

Field	Description
7–0 PERT[7:0]	 Pull Device Enable — This register configures whether a pull-up or a pull-down device is activated, if the port is used as input. This bit has no effect if the port is used as output. Out of reset no pull device is enabled. 0 Pull-up or pull-down device is disabled. 1 Either a pull-up or pull-down device is enabled.



Pin Name	Pin Functions	Description		
BKGD/MODC/ TAGHI	MODC	At the rising edge on RESET, the state of this pin is registered into the MODC bit to set the mode. (This pin always has an internal pullup.)		
	BKGD	Pseudo open-drain communication pin for the single-wire background debug mode. There is an internal pull-up resistor on this pin.		
	TAGHI	When instruction tagging is on, a 0 at the falling edge of E tags the high half of the instruction word being read into the instruction queue.		
PA7/A15/D15/D7	PA7-PA0	General-purpose I/O pins, see PORTA and DDRA registers.		
thru PA0/A8/D8/D0	A15–A8	High-order address lines multiplexed during ECLK low. Outputs except in special peripheral mode where they are inputs from an external tester system.		
	D15–D8	High-order bidirectional data lines multiplexed during ECLK high in expanded wide modes, special peripheral mode, and visible internal accesses (IVIS = 1) in emulation expanded narrow mode. Direction of data transfer is generally indicated by R/\overline{W} .		
	D15/D7 thru D8/D0	Alternate high-order and low-order bytes of the bidirectional data lines multiplexed during ECLK high in expanded narrow modes and narrow accesses in wide modes. Direction of data transfer is generally indicated by R/W.		
PB7/A7/D7	PB7–PB0	General-purpose I/O pins, see PORTB and DDRB registers.		
PB0/A0/D0	A7–A0	Low-order address lines multiplexed during ECLK low. Outputs except in special peripheral mode where they are inputs from an external tester system.		
	D7–D0	Low-order bidirectional data lines multiplexed during ECLK high in expanded wide modes, special peripheral mode, and visible internal accesses (with $IVIS = 1$) in emulation expanded narrow mode. Direction of data transfer is generally indicated by R/\overline{W} .		
PE7/NOACC	PE7	General-purpose I/O pin, see PORTE and DDRE registers.		
	NOACC	CPU No Access output. Indicates whether the current cycle is a free cycle. Only available in expanded modes.		
PE6/IPIPE1/ MODB/CLKTO	MODB	At the rising edge of $\overline{\text{RESET}}$, the state of this pin is registered into the MODB bit to set the mode.		
	PE6	General-purpose I/O pin, see PORTE and DDRE registers.		
	IPIPE1	Instruction pipe status bit 1, enabled by PIPOE bit in PEAR.		
	СLКТО	System clock test output. Only available in special modes. PIPOE = 1 overrides this function. The enable for this function is in the clock module.		
PE5/IPIPE0/MODA	MODA	At the rising edge on RESET, the state of this pin is registered into the MODA bit to set the mode.		
	PE5	General-purpose I/O pin, see PORTE and DDRE registers.		
	IPIPE0	Instruction pipe status bit 0, enabled by PIPOE bit in PEAR.		



Chapter 6 Background Debug Module (BDMV4) Block Description

6.3.2.1 BDM Status Register (BDMSTS)

0xFF01



Note:

- 1. ENBDM is read as "1" by a debugging environment in Special single-chip mode when the device is not secured or secured but fully erased (Flash and EEPROM). This is because the ENBDM bit is set by the standard firmware before a BDM command can be fully transmitted and executed.
- 2. UNSEC is read as "1" by a debugging environment in Special single-chip mode when the device is secured and fully erased, else it is "0" and can only be read if not secure (see also bit description).

Read: All modes through BDM operation

Write: All modes but subject to the following:

- BDMACT can only be set by BDM hardware upon entry into BDM. It can only be cleared by the standard BDM firmware lookup table upon exit from BDM active mode.
- CLKSW can only be written via BDM hardware or standard BDM firmware write commands.
- All other bits, while writable via BDM hardware or standard BDM firmware write commands, should only be altered by the BDM hardware or standard firmware lookup table as part of BDM command execution.
- ENBDM should only be set via a BDM hardware command if the BDM firmware commands are needed. (This does not apply in special single-chip mode).



If a read command is issued but the data is not retrieved within 512 serial clock cycles, a soft-reset will occur causing the command to be disregarded. The data is not available for retrieval after the time-out has occurred. This is the expected behavior if the handshake protocol is not enabled. However, consider the behavior where the BDC is running in a frequency much greater than the CPU frequency. In this case, the command could time out before the data is ready to be retrieved. In order to allow the data to be retrieved even with a large clock frequency mismatch (between BDC and CPU) when the hardware handshake protocol is enabled, the time out between a read command and the data retrieval is disabled. Therefore, the host could wait for more then 512 serial clock cycles and continue to be able to retrieve the data from an issued read command. However, as soon as the handshake pulse (ACK pulse) is issued, the time-out feature is re-activated, meaning that the target will time out after 512 clock cycles. Therefore, the host needs to retrieve the data within a 512 serial clock cycles time frame after the ACK pulse had been issued. After that period, the read command is discarded and the data is no longer available for retrieval. Any falling edge of the BKGD pin after the time-out period is considered to be a new command or a SYNC request.

Note that whenever a partially issued command, or partially retrieved data, has occurred the time out in the serial communication is active. This means that if a time frame higher than 512 serial clock cycles is observed between two consecutive negative edges and the command being issued or data being retrieved is not complete, a soft-reset will occur causing the partially received command or data retrieved to be disregarded. The next falling edge of the BKGD pin, after a soft-reset has occurred, is considered by the target as the start of a new BDM command, or the start of a SYNC request pulse.

6.4.13 Operation in Wait Mode

The BDM cannot be used in wait mode if the system disables the clocks to the BDM.

There is a clearing mechanism associated with the WAIT instruction when the clocks to the BDM (CPU core platform) are disabled. As the clocks restart from wait mode, the BDM receives a soft reset (clearing any command in progress) and the ACK function will be disabled. This is a change from previous BDM modules.

6.4.14 Operation in Stop Mode

The BDM is completely shutdown in stop mode.

There is a clearing mechanism associated with the STOP instruction. STOP must be enabled and the part must go into stop mode for this to occur. As the clocks restart from stop mode, the BDM receives a soft reset (clearing any command in progress) and the ACK function will be disabled. This is a change from previous BDM modules.



Field	Description
4 TAGAB	 Comparator A/B Tag Select — This bit controls whether the breakpoint will cause a break on the next instruction boundary (force) or on a match that will be an executable opcode (tagged). Non-executed opcodes cannot cause a tagged breakpoint. On match, break at the next instruction boundary (force) On match, break if/when the instruction is about to be executed (tagged)
3 BKCEN	 Breakpoint Comparator C Enable Bit — This bit enables the breakpoint capability using comparator C. 0 Comparator C disabled for breakpoint 1 Comparator C enabled for breakpoint Note: This bit will be cleared automatically when the DBG module is armed in loop1 mode.
2 TAGC	 Comparator C Tag Select — This bit controls whether the breakpoint will cause a break on the next instruction boundary (force) or on a match that will be an executable opcode (tagged). Non-executed opcodes cannot cause a tagged breakpoint. On match, break at the next instruction boundary (force) On match, break if/when the instruction is about to be executed (tagged)
1 RWCEN	 Read/Write Comparator C Enable Bit — The RWCEN bit controls whether read or write comparison is enabled for comparator C. RWCEN is not useful for tagged breakpoints. Read/Write is not used in comparison Read/Write is used in comparison
0 RWC	 Read/Write Comparator C Value Bit — The RWC bit controls whether read or write is used in compare for comparator C. The RWC bit is not used if RWCEN = 0. 0 Write cycle will be matched 1 Read cycle will be matched

7.3.2.8 Debug Control Register 3 (DBGC3)

Module Base + 0x0029

Starting address location affected by INITRG register setting.

	7	6	5	4	3	2	1	0
R W	BKAMBH ⁽¹⁾	BKAMBL ¹	BKBMBH ⁽²⁾	BKBMBL ²	RWAEN	RWA	RWBEN	RWB
Reset	0	0	0	0	0	0	0	0

1. In DBG mode, BKAMBH:BKAMBL has no meaning and are forced to 0's.

2. In DBG mode, BKBMBH:BKBMBL are used in full mode to qualify data.

Figure 7-14. Debug Control Register 3 (DBGC3)



8.2 Signal Description

The ATD10B8C has a total of 12 external pins.

8.2.1 AN7 / ETRIG / PAD7

This pin serves as the analog input channel 7. It can be configured to provide an external trigger for the ATD conversion. It can be configured as general-purpose digital I/O.

8.2.2 AN6 / PAD6

This pin serves as the analog input channel 6. It can be configured as general-purpose digital I/O.

8.2.3 AN5 / PAD5

This pin serves as the analog input channel 5. It can be configured as general-purpose digital I/O.

8.2.4 AN4 / PAD4

This pin serves as the analog input channel 4. It can be configured as general-purpose digital I/O.

8.2.5 AN3 / PAD3

This pin serves as the analog input channel 3. It can be configured as general-purpose digital I/O.

8.2.6 AN2 / PAD2

This pin serves as the analog input channel 2. It can be configured as general-purpose digital I/O.

8.2.7 AN1 / PAD1

This pin serves as the analog input channel 1. It can be configured as general-purpose digital I/O.

8.2.8 AN0 / PAD0

This pin serves as the analog input channel 0. It can be configured as general-purpose digital I/O.

8.2.9 V_{RH}, V_{RL}

 V_{RH} is the high reference voltage and V_{RL} is the low reference voltage for ATD conversion.

8.2.10 V_{DDA}, V_{SSA}

These pins are the power supplies for the analog circuitry of the ATD10B8C block.



8.4 Functional Description

The ATD10B8C is structured in an analog and a digital sub-block.

8.4.1 Analog Sub-block

The analog sub-block contains all analog electronics required to perform a single conversion. Separate power supplies V_{DDA} and V_{SSA} allow to isolate noise of other MCU circuitry from the analog sub-block.

8.4.1.1 Sample and Hold Machine

The sample and hold (S/H) machine accepts analog signals from the external surroundings and stores them as capacitor charge on a storage node.

The sample process uses a two stage approach. During the first stage, the sample amplifier is used to quickly charge the storage node. The second stage connects the input directly to the storage node to complete the sample for high accuracy.

When not sampling, the sample and hold machine disables its own clocks. The analog electronics still draw their quiescent current. The power down (ADPU) bit must be set to disable both the digital clocks and the analog power consumption.

The input analog signals are unipolar and must fall within the potential range of V_{SSA} to V_{DDA}.

8.4.1.2 Analog Input Multiplexer

The analog input multiplexer connects one of the 8 external analog input channels to the sample and hold machine.

8.4.1.3 Sample Buffer Amplifier

The sample amplifier is used to buffer the input analog signal so that the storage node can be quickly charged to the sample potential.

8.4.1.4 Analog-to-Digital (A/D) Machine

The A/D machine performs analog-to-digital conversions. The resolution is program selectable at either 8 or 10 bits. The A/D machine uses a successive approximation architecture. It functions by comparing the stored analog sample potential with a series of digitally generated analog potentials. By following a binary search algorithm, the A/D machine locates the approximating potential that is nearest to the sampled potential.

When not converting the A/D machine disables its own clocks. The analog electronics still draws quiescent current. The power down (ADPU) bit must be set to disable both the digital clocks and the analog power consumption.

Only analog input signals within the potential range of V_{RL} to V_{RH} (A/D reference potentials) will result in a non-railed digital output codes.



Module Base +	0x001C (CAN 0x001D (CAN 0x001E (CAN 0x001F (CAN	IIDMR4) IIDMR5) IIDMR6) IIDMR7)						
_	7	6	5	4	3	2	1	0
R W	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
Reset	0	0	0	0	0	0	0	0
F	7	6	5	4	3	2	1	0
R W	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
Reset	0	0	0	0	0	0	0	0
_	7	6	5	4	3	2	1	0
R W	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
Reset	0	0	0	0	0	0	0	0
- Г	7	6	5	4	3	2	1	0
R W	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
Reset	0	0	0	0	0	0	0	0

Figure 10-22. MSCAN Identifier Mask Registers (Second Bank) — CANIDMR4–CANIDMR7

Read: Anytime

Write: Anytime in initialization mode (INITRQ = 1 and INITAK = 1)

Table 10-22. CANIDMR4–CANIDMR7 Register Field Descriptions

Field	Description
7:0 AM[7:0]	 Acceptance Mask Bits — If a particular bit in this register is cleared, this indicates that the corresponding bit in the identifier acceptance register must be the same as its identifier bit before a match is detected. The message is accepted if all such bits match. If a bit is set, it indicates that the state of the corresponding bit in the identifier acceptance register does not affect whether or not the message is accepted. 0 Match corresponding acceptance code register and identifier bits 1 Ignore corresponding acceptance code register bit



10.4.3.1 Protocol Violation Protection

The MSCAN protects the user from accidentally violating the CAN protocol through programming errors. The protection logic implements the following features:

- The receive and transmit error counters cannot be written or otherwise manipulated.
- All registers which control the configuration of the MSCAN cannot be modified while the MSCAN is on-line. The MSCAN has to be in Initialization Mode. The corresponding INITRQ/INITAK handshake bits in the CANCTL0/CANCTL1 registers (see Section 10.3.2.1, "MSCAN Control Register 0 (CANCTL0)") serve as a lock to protect the following registers:
 - MSCAN control 1 register (CANCTL1)
 - MSCAN bus timing registers 0 and 1 (CANBTR0, CANBTR1)
 - MSCAN identifier acceptance control register (CANIDAC)
 - MSCAN identifier acceptance registers (CANIDAR0–CANIDAR7)
 - MSCAN identifier mask registers (CANIDMR0–CANIDMR7)
- The TXCAN pin is immediately forced to a recessive state when the MSCAN goes into the power down mode or initialization mode (see Section 10.4.5.6, "MSCAN Power Down Mode," and Section 10.4.5.5, "MSCAN Initialization Mode").
- The MSCAN enable bit (CANE) is writable only once in normal system operation modes, which provides further protection against inadvertently disabling the MSCAN.

10.4.3.2 Clock System

Figure 10-42 shows the structure of the MSCAN clock generation circuitry.



Figure 10-42. MSCAN Clocking Scheme

The clock source bit (CLKSRC) in the CANCTL1 register (10.3.2.2/10-294) defines whether the internal CANCLK is connected to the output of a crystal oscillator (oscillator clock) or to the bus clock.

The clock source has to be chosen such that the tight oscillator tolerance requirements (up to 0.4%) of the CAN protocol are met. Additionally, for high CAN bus rates (1 Mbps), a 45% to 55% duty cycle of the clock is required.



Chapter 11 Oscillator (OSCV2) Block Description

11.3 Memory Map and Register Definition

The CRG contains the registers and associated bits for controlling and monitoring the OSCV2 module.

11.4 Functional Description

The OSCV2 block has two external pins, EXTAL and XTAL. The oscillator input pin, EXTAL, is intended to be connected to either a crystal or an external clock source. The selection of Colpitts oscillator or Pierce oscillator/external clock depends on the XCLKS signal which is sampled during reset. The XTAL pin is an output signal that provides crystal circuit feedback.

A buffered EXTAL signal, OSCCLK, becomes the internal reference clock. To improve noise immunity, the oscillator is powered by the V_{DDPLL} and V_{SSPLL} power supply pins.

The Pierce oscillator can be used for higher frequencies compared to the low power Colpitts oscillator.

11.4.1 Amplitude Limitation Control (ALC)

The Colpitts oscillator is equipped with a feedback system which does not waste current by generating harmonics. Its configuration is "Colpitts oscillator with translated ground." The transconductor used is driven by a current source under the control of a peak detector which will measure the amplitude of the AC signal appearing on EXTAL node in order to implement an amplitude limitation control (ALC) loop. The ALC loop is in charge of reducing the quiescent current in the transconductor as a result of an increase in the oscillation amplitude. The oscillation amplitude can be limited to two values. The normal amplitude which is intended for non power saving modes and a small amplitude which is intended for low power operation modes. Please refer to the CRG block description chapter for the control and assignment of the amplitude value to operation modes.

11.4.2 Clock Monitor (CM)

The clock monitor circuit is based on an internal resistor-capacitor (RC) time delay so that it can operate without any MCU clocks. If no OSCCLK edges are detected within this RC time delay, the clock monitor indicates a failure which asserts self clock mode or generates a system reset depending on the state of SCME bit. If the clock monitor is disabled or the presence of clocks is detected no failure is indicated. The clock monitor function is enabled/disabled by the CME control bit, described in the CRG block description chapter.

11.5 Interrupts

OSCV2 contains a clock monitor, which can trigger an interrupt or reset. The control bits and status bits for the clock monitor are described in the CRG block description chapter.



Chapter 12 Pulse-Width Modulator (PWM8B6CV1) Block Description

• The channel is disabled

In this way, the output of the PWM will always be either the old waveform or the new waveform, not some variation in between. If the channel is not enabled, then writes to the period register will go directly to the latches as well as the buffer.

NOTE

Reads of this register return the most recent value written. Reads do not necessarily return the value of the currently active period due to the double buffering scheme.

Reference Section 12.4.2.3, "PWM Period and Duty," for more information.

To calculate the output period, take the selected clock source period for the channel of interest (A, B, SA, or SB) and multiply it by the value in the period register for that channel:

- Left aligned output (CAEx = 0)
- PWMx period = channel clock period * PWMPERx center aligned output (CAEx = 1)
- PWMx period = channel clock period * (2 * PWMPERx)

For boundary case programming values, please refer to Section 12.4.2.8, "PWM Boundary Cases."

Module Base + 0x0012





Chapter 13 Serial Communications Interface (S12SCIV2) Block Description

13.3.2.2 SCI Control Register 1 (SCICR1)



Read: Anytime

Write: Anytime

Table 13-2. SCICR1 Field De	scriptions
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Field	Description
7 LOOPS	 Loop Select Bit — LOOPS enables loop operation. In loop operation, the RXD pin is disconnected from the SCI and the transmitter output is internally connected to the receiver input. Both the transmitter and the receiver must be enabled to use the loop function.See Table 13-3. 0 Normal operation enabled 1 Loop operation enabled Note: The receiver input is determined by the RSRC bit.
6 SCISWAI	 SCI Stop in Wait Mode Bit — SCISWAI disables the SCI in wait mode. SCI enabled in wait mode SCI disabled in wait mode
5 RSRC	 Receiver Source Bit — When LOOPS = 1, the RSRC bit determines the source for the receiver shift register input. 0 Receiver input internally connected to transmitter output 1 Receiver input connected externally to transmitter
4 M	 Data Format Mode Bit — MODE determines whether data characters are eight or nine bits long. One start bit, eight data bits, one stop bit One start bit, nine data bits, one stop bit
3 WAKE	 Wakeup Condition Bit — WAKE determines which condition wakes up the SCI: a logic 1 (address mark) in the most significant bit position of a received data character or an idle condition on the RXD. 0 Idle line wakeup 1 Address mark wakeup
2 ILT	Idle Line Type Bit — ILT determines when the receiver starts counting logic 1s as idle character bits. The counting begins either after the start bit or after the stop bit. If the count begins after the start bit, then a string of logic 1s preceding the stop bit may cause false recognition of an idle character. Beginning the count after the stop bit avoids false idle character recognition, but requires properly synchronized transmissions. 0 Idle character bit count begins after start bit 1 Idle character bit count begins after stop bit
1 PE	 Parity Enable Bit — PE enables the parity function. When enabled, the parity function inserts a parity bit in the most significant bit position. 0 Parity function disabled 1 Parity function enabled
0 PT	Parity Type Bit — PT determines whether the SCI generates and checks for even parity or odd parity. With even parity, an even number of 1s clears the parity bit and an odd number of 1s sets the parity bit. With odd parity, an odd number of 1s clears the parity bit and an even number of 1s sets the parity bit. 0 Even parity 1 Odd parity



PAMOD	PEDGE	Pin Action
0	0	Falling edge
0	1	Rising edge
1	0	Div. by 64 clock enabled with pin high level
1	1	Div. by 64 clock enabled with pin low level

Table 15-20. Pin Action

NOTE

If the timer is not active (TEN = 0 in TSCR), there is no divide-by-64 because the \div 64 clock is generated by the timer prescaler.

Table 15-21.	. Timer	Clock	Selection
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CLK1	CLK0	Timer Clock
0	0	Use timer prescaler clock as timer counter clock
0	1	Use PACLK as input to timer counter clock
1	0	Use PACLK/256 as timer counter clock frequency
1	1	Use PACLK/65536 as timer counter clock frequency

For the description of PACLK please refer Figure 15-24.

If the pulse accumulator is disabled (PAEN = 0), the prescaler clock from the timer is always used as an input clock to the timer counter. The change from one selected clock to the other happens immediately after these bits are written.

15.3.2.16 Pulse Accumulator Flag Register (PAFLG)



Read: Anytime

Write: Anytime

When the TFFCA bit in the TSCR register is set, any access to the PACNT register will clear all the flags in the PAFLG register. Timer module must stay enabled (TEN =1) while clearing the bits.



Chapter 15 Timer Module (TIM16B8CV1) Block Description

Field	Description
1 PAOVF	Pulse Accumulator Overflow Flag — Set when the 16-bit pulse accumulator overflows from 0xFFFF to 0x0000. Clearing this bit requires wirting a one to this bit in the PAFLG register while TEN bit of TSCR1 register is set to one.
0 PAIF	Pulse Accumulator Input edge Flag — Set when the selected edge is detected at the IOC7 input pin. In event mode the event edge triggers PAIF and in gated time accumulation mode the trailing edge of the gate signal at the IOC7 input pin triggers PAIF.
	Clearing this bit requires writing a one to this bit in the PAFLG register while TEN bit of TSCR1 register is set to one. Any access to the PACNT register will clear all the flags in this register when TFFCA bit in register TSCR(0x0006) is set.

Table 15-22. PAFLG Field Descriptions



19.4.1.4 Illegal Flash Operations

19.4.1.4.1 Access Error

The ACCERR flag in the FSTAT register will be set during the command write sequence if any of the following illegal Flash operations are performed causing the command write sequence to immediately abort:

- 1. Writing to the Flash address space before initializing the FCLKDIV register
- 2. Writing a misaligned word or a byte to the valid Flash address space
- 3. Writing to the Flash address space while CBEIF is not set
- 4. Writing a second word to the Flash address space before executing a program or erase command on the previously written word
- 5. Writing to any Flash register other than FCMD after writing a word to the Flash address space
- 6. Writing a second command to the FCMD register before executing the previously written command
- 7. Writing an invalid command to the FCMD register
- 8. Writing to any Flash register other than FSTAT (to clear CBEIF) after writing to the FCMD register
- 9. The part enters stop mode and a program or erase command is in progress. The command is aborted and any pending command is killed
- 10. When security is enabled, a command other than mass erase originating from a non-secure memory or from the background debug mode is written to the FCMD register
- 11. A 0 is written to the CBEIF bit in the FSTAT register to abort a command write sequence.

The ACCERR flag will not be set if any Flash register is read during the command write sequence. If the Flash array is read during execution of an algorithm (CCIF=0), the Flash module will return invalid data and the ACCERR flag will not be set. If an ACCERR flag is set in the FSTAT register, the Flash command controller is locked. It is not possible to launch another command until the ACCERR flag is cleared.

19.4.1.4.2 Protection Violation

The PVIOL flag in the FSTAT register will be set during the command write sequence after the word write to the Flash address space if any of the following illegal Flash operations are performed, causing the command write sequence to immediately abort:

- 1. Writing a Flash address to program in a protected area of the Flash array (see Section 19.3.2.5).
- 2. Writing a Flash address to erase in a protected area of the Flash array.
- 3. Writing the mass erase command to the FCMD register while any protection is enabled.

If the PVIOL flag is set, the Flash command controller is locked. It is not possible to launch another command until the PVIOL flag is cleared.



Chapter 20 96 Kbyte Flash Module (S12FTS96KV1)



Note: 0x3A–0x3F correspond to the PPAGE register content Figure 20-4. Flash Memory Map



Chapter 21 128 Kbyte Flash Module (S12FTS128K1V1)







21.4.1.3.3 Sector Erase Command

The sector erase operation will erase all addresses in a 1024 byte sector of the Flash array using an embedded algorithm.

An example flow to execute the sector erase operation is shown in Figure 21-24. The sector erase command write sequence is as follows:

- 1. Write to a Flash array address to start the command write sequence for the sector erase command. The Flash address written determines the sector to be erased while MCU address bits [9:0] and the data written are ignored.
- 2. Write the sector erase command, 0x40, to the FCMD register.
- 3. Clear the CBEIF flag in the FSTAT register by writing a 1 to CBEIF to launch the sector erase command.

If a Flash sector to be erased is in a protected area of the Flash array, the PVIOL flag in the FSTAT register will set and the sector erase command will not launch. Once the sector erase command has successfully launched, the CCIF flag in the FSTAT register will set after the sector erase operation has completed unless a new command write sequence has been buffered.