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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	HCS12
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, EBI/EMI, SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	35
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	52-LQFP
Supplier Device Package	52-TQFP (10x10)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s12c128vpbe">https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s12c128vpbe</a>

## Chapter 14

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## Chapter 15

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### 1.3.4.6 PA[7:0] / ADDR[15:8] / DATA[15:8] — Port A I/O Pins

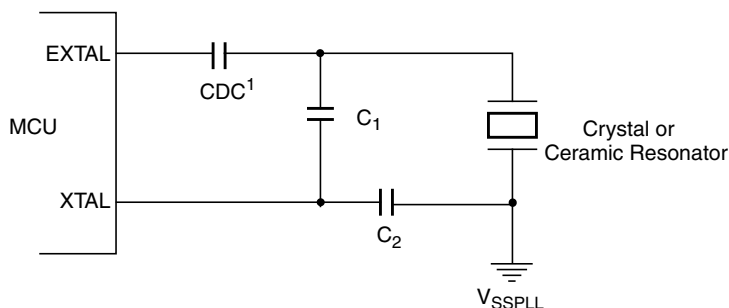
PA7–PA0 are general purpose input or output pins,. In MCU expanded modes of operation, these pins are used for the multiplexed external address and data bus. PA[7:1] pins are not available in the 48-pin package version. PA[7:3] are not available in the 52-pin package version.

### 1.3.4.7 PB[7:0] / ADDR[7:0] / DATA[7:0] — Port B I/O Pins

PB7–PB0 are general purpose input or output pins. In MCU expanded modes of operation, these pins are used for the multiplexed external address and data bus. PB[7:5] and PB[3:0] pins are not available in the 48-pin nor 52-pin package version.

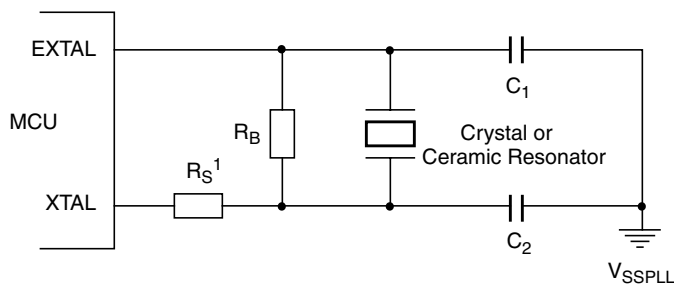
### 1.3.4.8 PE7 / NOACC / $\overline{\text{XCLKS}}$ — Port E I/O Pin 7

PE7 is a general purpose input or output pin. During MCU expanded modes of operation, the NOACC signal, when enabled, is used to indicate that the current bus cycle is an unused or “free” cycle. This signal will assert when the CPU is not using the bus. The  $\overline{\text{XCLKS}}$  is an input signal which controls whether a crystal in combination with the internal Colpitts (low power) oscillator is used or whether Pierce oscillator/external clock circuitry is used. The state of this pin is latched at the rising edge of  $\overline{\text{RESET}}$ . If the input is a logic low the EXTAL pin is configured for an external clock drive or a Pierce oscillator. If input is a logic high a Colpitts oscillator circuit is configured on EXTAL and XTAL. Since this pin is an input with a pull-up device during reset, if the pin is left floating, the default configuration is a Colpitts oscillator circuit on EXTAL and XTAL.



1. Due to the nature of a translated ground Colpitts oscillator a DC voltage bias is applied to the crystal. Please contact the crystal manufacturer for crystal DC.

**Figure 1-11. Colpitts Oscillator Connections (PE7 = 1)**



1. RS can be zero (shorted) when used with higher frequency crystals, refer to manufacturer's data.

**Figure 1-12. Pierce Oscillator Connections (PE7 = 0)**

## 1.4 System Clock Description

The clock and reset generator provides the internal clock signals for the core and all peripheral modules. Figure 1-14 shows the clock connections from the CRG to all modules. Consult the CRG Block User Guide for details on clock generation.

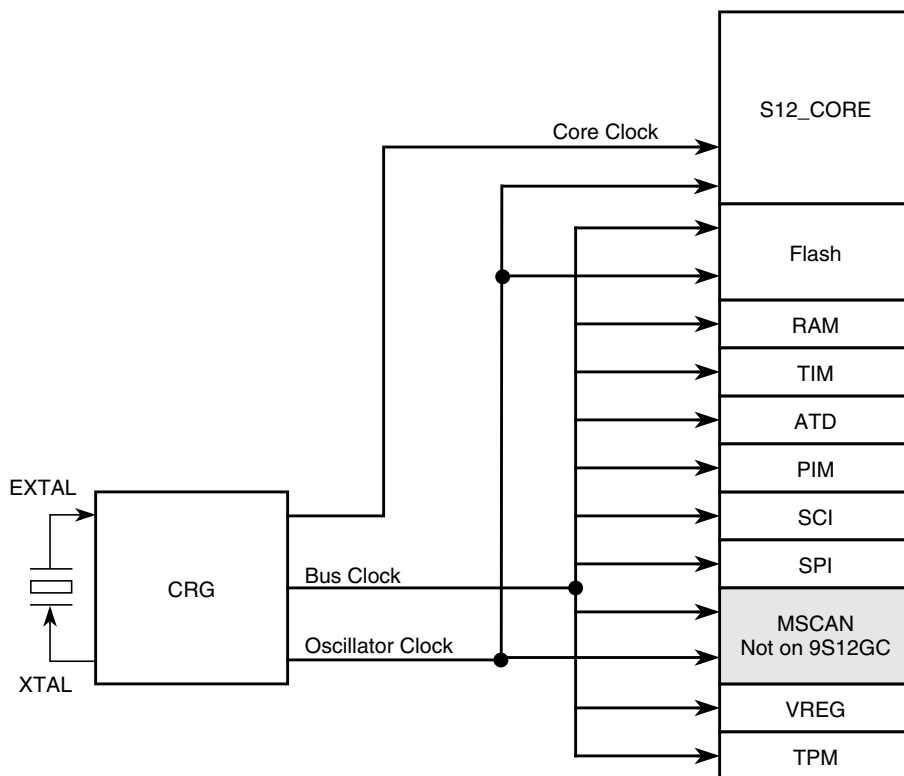


Figure 1-14. Clock Connections

## 1.5 Modes of Operation

Eight possible modes determine the device operating configuration. Each mode has an associated default memory map and external bus configuration controlled by a further pin.

Three low power modes exist for the device.

### 1.5.1 Chip Configuration Summary

The operating mode out of reset is determined by the states of the MODC, MODB, and MODA pins during reset. The MODC, MODB, and MODA bits in the MODE register show the current operating mode and provide limited mode switching during operation. The states of the MODC, MODB, and MODA pins are latched into these bits on the rising edge of the reset signal. The ROMCTL signal allows the setting of the ROMON bit in the MISC register thus controlling whether the internal Flash is visible in the memory map. ROMON = 1 mean the Flash is visible in the memory map. The state of the ROMCTL pin is latched into the ROMON bit in the MISC register on the rising edge of the reset signal.

This register is not in the on-chip memory map in expanded and special peripheral modes. Therefore, these accesses will be echoed externally.

### NOTE

These bits have no effect when the associated pin(s) are outputs. (The pull resistors are inactive.)

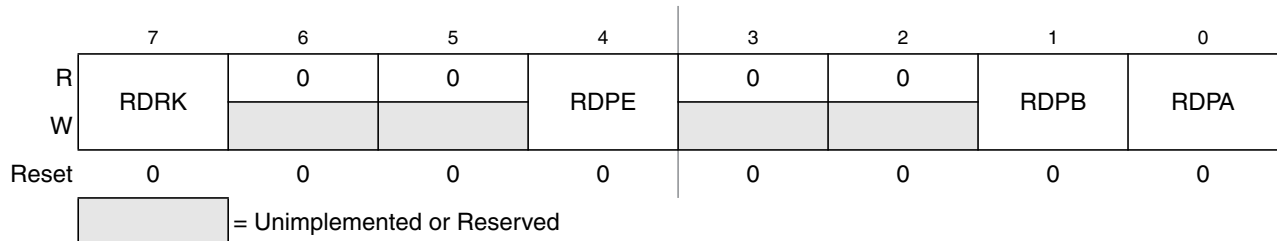
**Table 4-9. PUCR Field Descriptions**

Field	Description
7 PUPKE	<b>Pull resistors Port K Enable</b> 0 Port K pull resistors are disabled. 1 Enable pull resistors for port K input pins.
4 PUPEE	<b>Pull resistors Port E Enable</b> 0 Port E pull resistors on bits 7, 4:0 are disabled. 1 Enable pull resistors for port E input pins bits 7, 4:0. <b>Note:</b> Pins 5 and 6 of port E have pull resistors which are only enabled during reset. This bit has no effect on these pins.
1 PUPBE	<b>Pull resistors Port B Enable</b> 0 Port B pull resistors are disabled. 1 Enable pull resistors for all port B input pins.
0 PUPAE	<b>Pull resistors Port A Enable</b> 0 Port A pull resistors are disabled. 1 Enable pull resistors for all port A input pins.

### 4.3.2.11 Reduced Drive Register (RDRIV)

Module Base + 0x000D

Starting address location affected by INITRG register setting.



**Figure 4-15. Reduced Drive Register (RDRIV)**

Read: Anytime (provided this register is in the map)

Write: Anytime (provided this register is in the map)

This register is used to select reduced drive for the pins associated with the core ports. This gives reduced power consumption and reduced RFI with a slight increase in transition time (depending on loading). This feature would be used on ports which have a light loading. The reduced drive function is independent of which function is being used on a particular port.

This register is not in the on-chip memory map in expanded and special peripheral modes. Therefore, these accesses will be echoed externally.

### 7.4.2.5.8 Inside Range ( $A \leq \text{address} \leq B$ )

In the inside range trigger mode, if the match condition for A and B happen on the same bus cycle, both the A and B flags in DBGSC are set and a trigger occurs. If a match condition on only A or only B occurs no flags are set. If TRGSEL = 1, the inside range is accurate only to word boundaries. If TRGSEL = 0, an aligned word access which straddles the range boundary will cause a trigger only if the aligned address is within the range.

### 7.4.2.5.9 Outside Range ( $\text{address} < A$ or $\text{address} > B$ )

In the outside range trigger mode, if the match condition for A or B is met, the corresponding flag in DBGSC is set and a trigger occurs. If TRGSEL = 1, the outside range is accurate only to word boundaries. If TRGSEL = 0, an aligned word access which straddles the range boundary will cause a trigger only if the aligned address is outside the range.

### 7.4.2.5.10 Control Bit Priorities

The definitions of some of the control bits are incompatible with each other. Table 7-25 and the notes associated with it summarize how these incompatibilities are managed:

- Read/write comparisons are not compatible with TRGSEL = 1. Therefore, RWAEN and RWBEN are ignored.
- Event-only trigger modes are always considered a begin-type trigger. See Section 7.4.2.8.1, “Storing with Begin-Trigger,” and Section 7.4.2.8.2, “Storing with End-Trigger.”
- Detail capture mode has priority over the event-only trigger/capture modes. Therefore, event-only modes have no meaning in detail mode and their functions default to similar trigger modes.

**Table 7-25. Resolution of Mode Conflicts**

Mode	Normal / Loop1		Detail	
	Tag	Force	Tag	Force
A only				
A or B				
A then B				
Event-only B	1		1, 3	3
A then event-only B	2		4	4
A and B (full mode)	5		5	
A and not B (full mode)	5		5	
Inside range	6		6	
Outside range	6		6	

1 — Ignored — same as force

2 — Ignored for comparator B

3 — Reduces to effectively “B only”

4 — Works same as A then B

5 — Reduces to effectively “A only” — B not compared

6 — Only accurate to word boundaries

# Chapter 10

## Freescalé's Scalable Controller Area Network (S12MSCANV2)

### 10.1 Introduction

Freescalé's scalable controller area network (S12MSCANV2) definition is based on the MSCAN12 definition, which is the specific implementation of the MSCAN concept targeted for the M68HC12 microcontroller family.

The module is a communication controller implementing the CAN 2.0A/B protocol as defined in the Bosch specification dated September 1991. For users to fully understand the MSCAN specification, it is recommended that the Bosch specification be read first to familiarize the reader with the terms and concepts contained within this document.

Though not exclusively intended for automotive applications, CAN protocol is designed to meet the specific requirements of a vehicle serial data bus: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness, and required bandwidth.

MSCAN uses an advanced buffer arrangement resulting in predictable real-time behavior and simplified application software.

#### 10.1.1 Glossary

ACK: Acknowledge of CAN message

CAN: Controller Area Network

CRC: Cyclic Redundancy Code

EOF: End of Frame

FIFO: First-In-First-Out Memory

IFS: Inter-Frame Sequence

SOF: Start of Frame

CPU bus: CPU related read/write data bus

CAN bus: CAN protocol related serial bus

oscillator clock: Direct clock from external oscillator

bus clock: CPU bus realated clock

CAN clock: CAN protocol related clock

### NOTE

Reading this register when in any other mode other than sleep or initialization mode may return an incorrect value. For MCUs with dual CPUs, this may result in a CPU fault condition.

Writing to this register when in special modes can alter the MSCAN functionality.

#### 10.3.2.15 MSCAN Transmit Error Counter (CANTXERR)

This register reflects the status of the MSCAN transmit error counter.

Module Base + 0x000F

	7	6	5	4	3	2	1	0
R	TXERR7	TXERR6	TXERR5	TXERR4	TXERR3	TXERR2	TXERR1	TXERR0
W								
Reset:	0	0	0	0	0	0	0	0
	= Unimplemented							

**Figure 10-18. MSCAN Transmit Error Counter (CANTXERR)**

Read: Only when in sleep mode (SLPRQ = 1 and SLPK = 1) or initialization mode (INITRQ = 1 and INITAK = 1)

Write: Unimplemented

### NOTE

Reading this register when in any other mode other than sleep or initialization mode, may return an incorrect value. For MCUs with dual CPUs, this may result in a CPU fault condition.

Writing to this register when in special modes can alter the MSCAN functionality.



Each PWM channel has the capability of selecting one of two clocks. For channels 0, 1, 4, and 5 the clock choices are clock A or clock SA. For channels 2 and 3 the choices are clock B or clock SB. The clock selection is done with the PCLKx control bits in the PWMCLK register.

Changing clock control bits while channels are operating can cause irregularities in the PWM outputs.

The main part of the PWM module are the actual timers. Each of the timer channels has a counter, a period register and a duty register (each are 8 bit). The waveform output period is controlled by a match between the period register and the value in the counter. The duty is controlled by a match between the duty register and the counter value and causes the state of the output to change during the period. The starting polarity of the output is also selectable on a per channel basis. [Figure 12-35](#) shows a block diagram for PWM timer.



- Transmission complete
- Receiver full
- Idle receiver input
- Receiver overrun
- Noise error
- Framing error
- Parity error
- Receiver framing error detection
- Hardware parity checking
- 1/16 bit-time noise detection

### 13.1.3 Modes of Operation

The SCI operation is the same independent of device resource mapping and bus interface mode. Different power modes are available to facilitate power saving.

#### 13.1.3.1 Run Mode

Normal mode of operation.

#### 13.1.3.2 Wait Mode

SCI operation in wait mode depends on the state of the SCISWAI bit in the SCI control register 1 (SCICR1).

- If SCISWAI is clear, the SCI operates normally when the CPU is in wait mode.
- If SCISWAI is set, SCI clock generation ceases and the SCI module enters a power-conservation state when the CPU is in wait mode. Setting SCISWAI does not affect the state of the receiver enable bit, RE, or the transmitter enable bit, TE.
- If SCISWAI is set, any transmission or reception in progress stops at wait mode entry. The transmission or reception resumes when either an internal or external interrupt brings the CPU out of wait mode. Exiting wait mode by reset aborts any transmission or reception in progress and resets the SCI.

#### 13.1.3.3 Stop Mode

The SCI is inactive during stop mode for reduced power consumption. The STOP instruction does not affect the SCI register states, but the SCI module clock will be disabled. The SCI operation resumes from where it left off after an external interrupt brings the CPU out of stop mode. Exiting stop mode by reset aborts any transmission or reception in progress and resets the SCI.

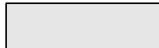
### 13.3.2.6 SCI Data Registers (SCIDRH and SCIDRL)

Module Base + 0x\_0006

	7	6	5	4	3	2	1	0
R	R8	T8	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

Module Base + 0x\_0007

	7	6	5	4	3	2	1	0
R	R7	R6	R5	R4	R3	R2	R1	R0
W	T7	T6	T5	T4	T3	T2	T1	T0
Reset	0	0	0	0	0	0	0	0

 = Unimplemented or Reserved

**Figure 13-8. SCI Data Registers (SCIDRH and SCIDRL)**

Read: Anytime; reading accesses SCI receive data register

Write: Anytime; writing accesses SCI transmit data register; writing to R8 has no effect

**Table 13-7. SCIDRH AND SCIDRL Field Descriptions**

Field	Description
7 R8	<b>Received Bit 8</b> — R8 is the ninth data bit received when the SCI is configured for 9-bit data format (M = 1).
6 T8	<b>Transmit Bit 8</b> — T8 is the ninth data bit transmitted when the SCI is configured for 9-bit data format (M = 1).
7–0 R[7:0] T[7:0]	<b>Received Bits</b> — Received bits seven through zero for 9-bit or 8-bit data formats <b>Transmit Bits</b> — Transmit bits seven through zero for 9-bit or 8-bit formats

#### NOTE

If the value of T8 is the same as in the previous transmission, T8 does not have to be rewritten. The same value is transmitted until T8 is rewritten.

In 8-bit data format, only SCI data register low (SCIDRL) needs to be accessed.

When transmitting in 9-bit data format and using 8-bit write instructions, write first to SCI data register high (SCIDRH), then SCIDRL.

### NOTE

When queueing an idle character, return the TE bit to logic 1 before the stop bit of the current frame shifts out through the **Tx output** signal. Setting TE after the stop bit appears on **Tx output signal** causes data previously written to the SCI data register to be lost. Toggle the TE bit for a queued idle character while the TDRE flag is set and immediately before writing the next byte to the SCI data register.

### NOTE

If the TE bit is clear and the transmission is complete, the SCI is not the master of the TXD pin

## 13.4.4 Receiver

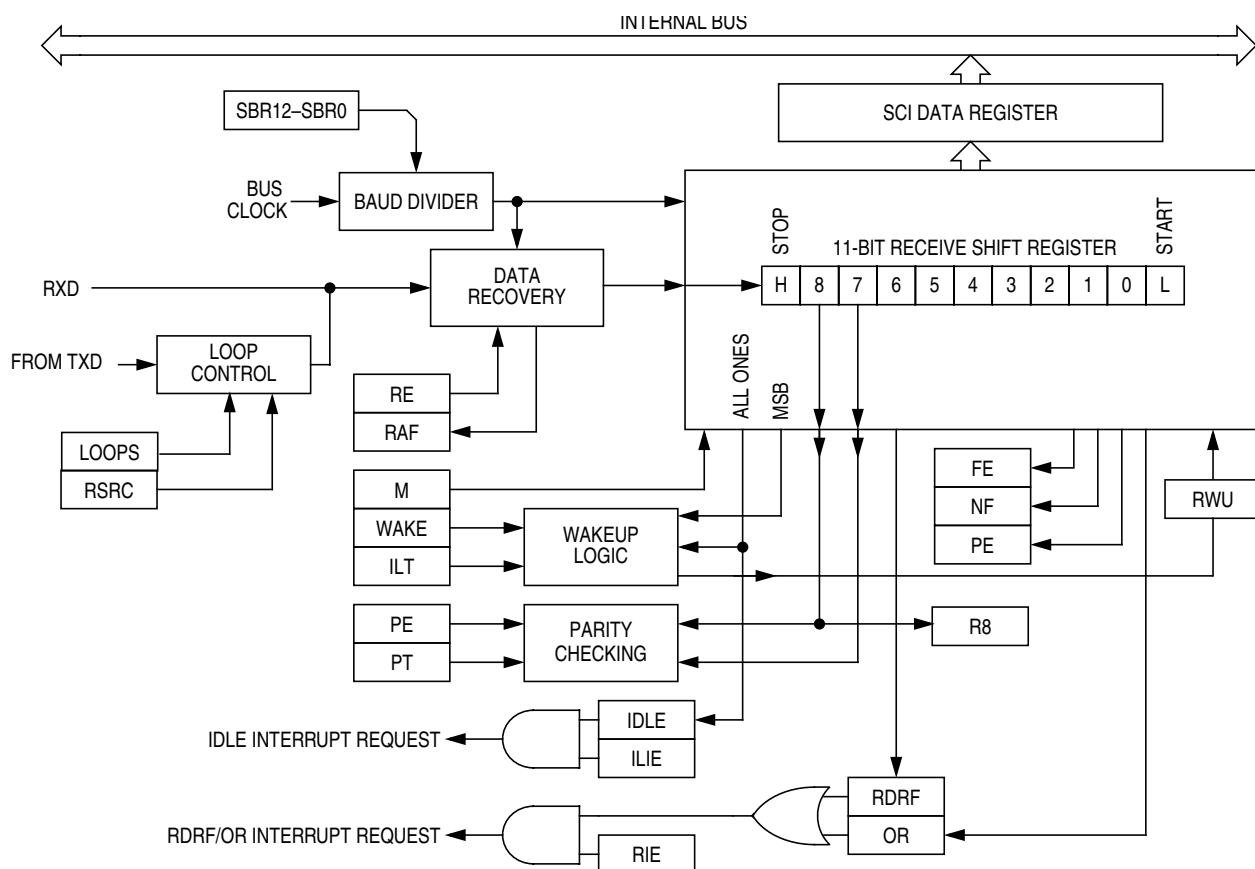


Figure 13-12. SCI Receiver Block Diagram

### 13.4.4.1 Receiver Character Length

The SCI receiver can accommodate either 8-bit or 9-bit data characters. The state of the M bit in SCI control register 1 (SCICR1) determines the length of data characters. When receiving 9-bit data, bit R8 in SCI data register high (SCIDRH) is the ninth bit (bit 8).

In master mode, with slave select output enabled the  $\overline{SS}$  line is always deasserted and reasserted between successive transfers for at least minimum idle time.

## 14.4.3.3 CPHA = 1 Transfer Format

Some peripherals require the first SCK edge before the first data bit becomes available at the data out pin, the second edge clocks data into the system. In this format, the first SCK edge is issued by setting the CPHA bit at the beginning of the 8-cycle transfer operation.

The first edge of SCK occurs immediately after the half SCK clock cycle synchronization delay. This first edge commands the slave to transfer its first data bit to the serial data input pin of the master.

A half SCK cycle later, the second edge appears on the SCK pin. This is the latching edge for both the master and slave.

When the third edge occurs, the value previously latched from the serial data input pin is shifted into the LSB or MSB of the SPI shift register, depending on LSBFE bit. After this edge, the next bit of the master data is coupled out of the serial data output pin of the master to the serial input pin on the slave.

This process continues for a total of 16 edges on the SCK line with data being latched on even numbered edges and shifting taking place on odd numbered edges.

Data reception is double buffered, data is serially shifted into the SPI shift register during the transfer and is transferred to the parallel SPI Data Register after the last bit is shifted in.

After the 16th SCK edge:

- Data that was previously in the SPI Data Register of the master is now in the data register of the slave, and data that was in the data register of the slave is in the master.
- The SPIF flag bit in SPISR is set indicating that the transfer is complete.

Figure 14-10 shows two clocking variations for CPHA = 1. The diagram may be interpreted as a master or slave timing diagram because the SCK, MISO, and MOSI pins are connected directly between the master and the slave. The MISO signal is the output from the slave, and the MOSI signal is the output from the master. The  $\overline{SS}$  line is the slave select input to the slave. The  $\overline{SS}$  pin of the master must be either high or reconfigured as a general-purpose output not affecting the SPI.

The  $\overline{SS}$  line can remain active low between successive transfers (can be tied low at all times). This format is sometimes preferred in systems having a single fixed master and a single slave that drive the MISO data line.

- Back-to-back transfers in master mode

In master mode, if a transmission has completed and a new data byte is available in the SPI Data Register, this byte is send out immediately without a trailing and minimum idle time.

The SPI interrupt request flag (SPIF) is common to both the master and slave modes. SPIF gets set one half SCK cycle after the last SCK edge.

## 16.2 External Signal Description

Due to the nature of VREG3V3V2 being a voltage regulator providing the chip internal power supply voltages most signals are power supply signals connected to pads.

Table 16-1 shows all signals of VREG3V3V2 associated with pins.

**Table 16-1. VREG3V3V2 — Signal Properties**

Name	Port	Function	Reset State	Pull Up
$V_{DDR}$	—	VREG3V3V2 power input (positive supply)	—	—
$V_{DDA}$	—	VREG3V3V2 quiet input (positive supply)	—	—
$V_{SSA}$	—	VREG3V3V2 quiet input (ground)	—	—
$V_{DD}$	—	VREG3V3V2 primary output (positive supply)	—	—
$V_{SS}$	—	VREG3V3V2 primary output (ground)	—	—
$V_{DDPLL}$	—	VREG3V3V2 secondary output (positive supply)	—	—
$V_{SSPLL}$	—	VREG3V3V2 secondary output (ground)	—	—
$V_{REGEN}$ (optional)	—	VREG3V3V2 (Optional) Regulator Enable	—	—

### NOTE

Check device overview chapter for connectivity of the signals.

### 16.2.1 $V_{DDR}$ — Regulator Power Input

Signal  $V_{DDR}$  is the power input of VREG3V3V2. All currents sourced into the regulator loads flow through this pin. A chip external decoupling capacitor (100 nF...220 nF, X7R ceramic) between  $V_{DDR}$  and  $V_{SSR}$  can smoothen ripple on  $V_{DDR}$ .

For entering Shutdown Mode, pin  $V_{DDR}$  should also be tied to ground on devices without a  $V_{REGEN}$  pin.

### 16.2.2 $V_{DDA}$ , $V_{SSA}$ — Regulator Reference Supply

Signals  $V_{DDA}/V_{SSA}$  which are supposed to be relatively quiet are used to supply the analog parts of the regulator. Internal precision reference circuits are supplied from these signals. A chip external decoupling capacitor (100 nF...220 nF, X7R ceramic) between  $V_{DDA}$  and  $V_{SSA}$  can further improve the quality of this supply.

## 16.5 Resets

This subsection describes how VREG3V3V2 controls the reset of the MCU. The reset values of registers and signals are provided in [Section 16.3, “Memory Map and Register Definition”](#). Possible reset sources are listed in [Table 16-4](#).

**Table 16-4. VREG3V3V2 — Reset Sources**

Reset Source	Local Enable
Power-on reset	Always active
Low-voltage reset	Available only in Full Performance Mode

### 16.5.1 Power-On Reset

During chip power-up the digital core may not work if its supply voltage  $V_{DD}$  is below the POR deassertion level ( $V_{POR\overline{D}}$ ). Therefore, signal POR which forces the other blocks of the device into reset is kept high until  $V_{DD}$  exceeds  $V_{POR\overline{D}}$ . Then POR becomes low and the reset generator of the device continues the start-up sequence. The power-on reset is active in all operation modes of VREG3V3V2.

### 16.5.2 Low-Voltage Reset

For details on low-voltage reset see [Section 16.4.6, “LVR — Low-Voltage Reset”](#).

## 16.6 Interrupts

This subsection describes all interrupts originated by VREG3V3V2.

The interrupt vectors requested by VREG3V3V2 are listed in [Table 16-5](#). Vector addresses and interrupt priorities are defined at MCU level.

**Table 16-5. VREG3V3V2 — Interrupt Vectors**

Interrupt Source	Local Enable
Low Voltage Interrupt (LVI)	LVIE = 1; Available only in Full Performance Mode

### 16.6.1 LVI — Low-Voltage Interrupt

In FPM VREG3V3V2 monitors the input voltage  $V_{DDA}$ . Whenever  $V_{DDA}$  drops below level  $V_{LVIA}$  the status bit LVDS is set to 1. Vice versa, LVDS is reset to 0 when  $V_{DDA}$  rises above level  $V_{LVID}$ . An interrupt, indicated by flag LVIF = 1, is triggered by any change of the status bit LVDS if interrupt enable bit LVIE = 1.

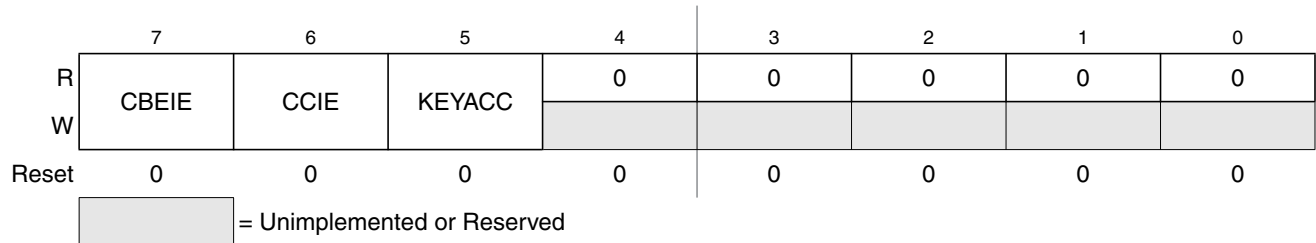
#### NOTE

On entering the Reduced Power Mode, the LVIF is not cleared by the VREG3V3V2.

### 17.3.2.4 Flash Configuration Register (FCNFG)

The FCNFG register enables the Flash interrupts and gates the security backdoor key writes.

Module Base + 0x0003



**Figure 17-7. Flash Configuration Register (FCNFG)**

CBEIE, CCIE, and KEYACC are readable and writable while remaining bits read 0 and are not writable. KEYACC is only writable if the KEYEN bit in the FSEC register is set to the enabled state (see [Section 17.3.2.2](#)).

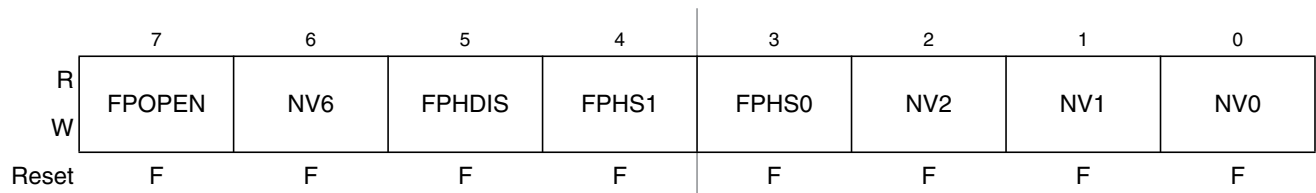
**Table 17-7. FCNFG Field Descriptions**

Field	Description
7 CBEIE	<b>Command Buffer Empty Interrupt Enable</b> — The CBEIE bit enables the interrupts in case of an empty command buffer in the Flash module. 0 Command Buffer Empty interrupts disabled 1 An interrupt will be requested whenever the CBEIF flag is set (see <a href="#">Section 17.3.2.6</a> )
6 CCIE	<b>Command Complete Interrupt Enable</b> — The CCIE bit enables the interrupts in case of all commands being completed in the Flash module. 0 Command Complete interrupts disabled 1 An interrupt will be requested whenever the CCIF flag is set (see <a href="#">Section 17.3.2.6</a> )
5 KEYACC	<b>Enable Security Key Writing.</b> 0 Flash writes are interpreted as the start of a command write sequence 1 Writes to the Flash array are interpreted as a backdoor key while reads of the Flash array return invalid data

### 17.3.2.5 Flash Protection Register (FPROT)

The FPROT register defines which Flash sectors are protected against program or erase.

Module Base + 0x0004



**Figure 17-8. Flash Protection Register (FPROT)**

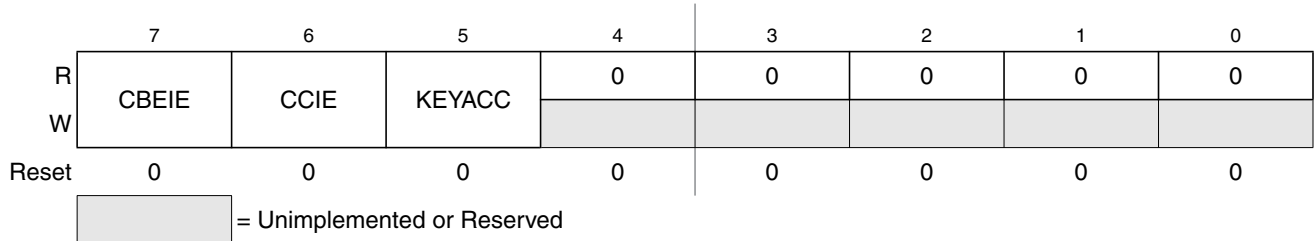
The FPROT register is readable in normal and special modes. FPOPEN can only be written from a 1 to a 0. FPHS[1:0] can be written anytime until FPHDIS is cleared. The FPROT register is loaded from Flash address 0xFF0D during the reset sequence, indicated by F in [Figure 17-8](#).



### 18.3.2.4 Flash Configuration Register (FCNFG)

The FCNFG register enables the Flash interrupts and gates the security backdoor key writes.

Module Base + 0x0003



**Figure 18-7. Flash Configuration Register (FCNFG)**

CBEIE, CCIE, and KEYACC are readable and writable while remaining bits read 0 and are not writable. KEYACC is only writable if the KEYEN bit in the FSEC register is set to the enabled state (see [Section 18.3.2.2](#)).

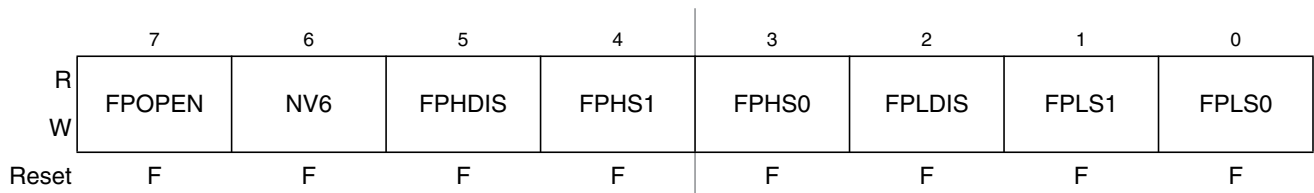
**Table 18-7. FCNFG Field Descriptions**

Field	Description
7 CBEIE	<b>Command Buffer Empty Interrupt Enable</b> — The CBEIE bit enables the interrupts in case of an empty command buffer in the Flash module. 0 Command Buffer Empty interrupts disabled 1 An interrupt will be requested whenever the CBEIF flag is set (see <a href="#">Section 18.3.2.6</a> )
6 CCIE	<b>Command Complete Interrupt Enable</b> — The CCIE bit enables the interrupts in case of all commands being completed in the Flash module. 0 Command Complete interrupts disabled 1 An interrupt will be requested whenever the CCIF flag is set (see <a href="#">Section 18.3.2.6</a> )
5 KEYACC	<b>Enable Security Key Writing.</b> 0 Flash writes are interpreted as the start of a command write sequence 1 Writes to the Flash array are interpreted as a backdoor key while reads of the Flash array return invalid data

### 18.3.2.5 Flash Protection Register (FPROT)

The FPROT register defines which Flash sectors are protected against program or erase.

Module Base + 0x0004



**Figure 18-8. Flash Protection Register (FPROT)**

The FPROT register is readable in normal and special modes. FPOPEN can only be written from a 1 to a 0. [FPLS\[1:0\]](#) can be written anytime until [FPLDIS](#) is cleared. [FPHS\[1:0\]](#) can be written anytime until

Table 19-14. FSTAT Field Descriptions

Field	Description
5 PVIOL	<b>Protection Violation</b> — The PVIOL flag indicates an attempt was made to program or erase an address in a protected Flash array memory area. The PVIOL flag is cleared by writing a 1 to PVIOL. Writing a 0 to the PVIOL flag has no effect on PVIOL. While PVIOL is set, it is not possible to launch another command. 0 No protection violation detected 1 Protection violation has occurred
4 ACCERR	<b>Access Error</b> — The ACCERR flag indicates an illegal access to the Flash array caused by either a violation of the command write sequence, issuing an illegal command (illegal combination of the CMDDBx bits in the FCMD register) or the execution of a CPU STOP instruction while a command is executing (CCIF=0). The ACCERR flag is cleared by writing a 1 to ACCERR. Writing a 0 to the ACCERR flag has no effect on ACCERR. While ACCERR is set, it is not possible to launch another command. 0 No access error detected 1 Access error has occurred
2 BLANK	<b>Flash Array Has Been Verified as Erased</b> — The BLANK flag indicates that an erase verify command has checked the Flash array and found it to be erased. The BLANK flag is cleared by hardware when CBEIF is cleared as part of a new valid command write sequence. Writing to the BLANK flag has no effect on BLANK. 0 If an erase verify command has been requested, and the CCIF flag is set, then a 0 in BLANK indicates the array is not erased 1 Flash array verifies as erased
1 FAIL	<b>Flag Indicating a Failed Flash Operation</b> — In special modes, the FAIL flag will set if the erase verify operation fails (Flash array verified as not erased). Writing a 0 to the FAIL flag has no effect on FAIL. The FAIL flag is cleared by writing a 1 to FAIL. While FAIL is set, it is not possible to launch another command. 0 Flash operation completed without error 1 Flash operation failed
0 DONE	<b>Flag Indicating a Failed Operation is not Active</b> — In special modes, the DONE flag will clear if a program, erase, or erase verify operation is active. 0 Flash operation is active 1 Flash operation is not active

### 19.3.2.7 Flash Command Register (FCMD)

The FCMD register defines the Flash commands.

Module Base + 0x0006

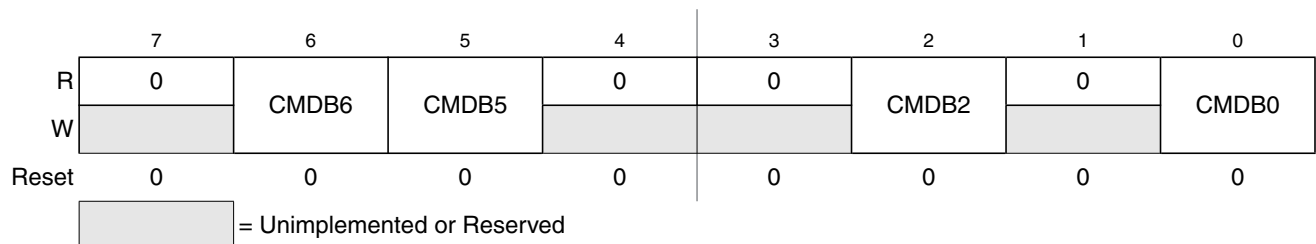


Figure 19-13. Flash Command Register (FCMD)

Bits CMDB6, CMDB5, CMDB2, and CMDB0 are readable and writable during a command write sequence while bits 7, 4, 3, and 1 read 0 and are not writable.

### 19.4.1.3 Valid Flash Commands

Table 19-17 summarizes the valid Flash commands along with the effects of the commands on the Flash array.

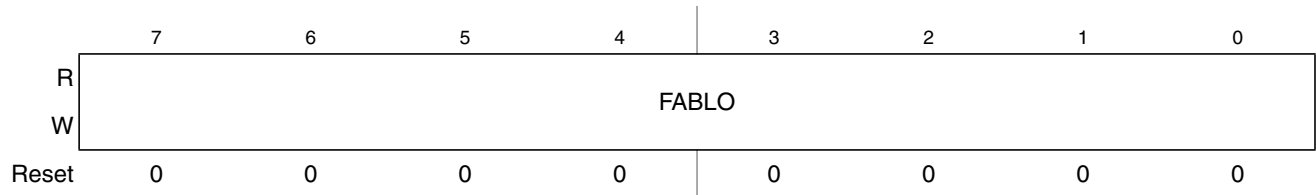
**Table 19-17. Valid Flash Commands**

FCMD	Meaning	Function on Flash Array
0x05	Erase Verify	Verify all bytes in the Flash array are erased. If the Flash array is erased, the BLANK bit will set in the FSTAT register upon command completion.
0x20	Program	Program a word (2 bytes) in the Flash array.
0x40	Sector Erase	Erase all 1024 bytes in a sector of the Flash array.
0x41	Mass Erase	Erase all bytes in the Flash array. A mass erase of the full Flash array is only possible when FPLDIS, FPHDIS, and FPOPEN bits in the FPROT register are set prior to launching the command.

#### CAUTION

A Flash word must be in the erased state before being programmed.  
Cumulative programming of bits within a Flash word is not allowed.

Module Base + 0x0009



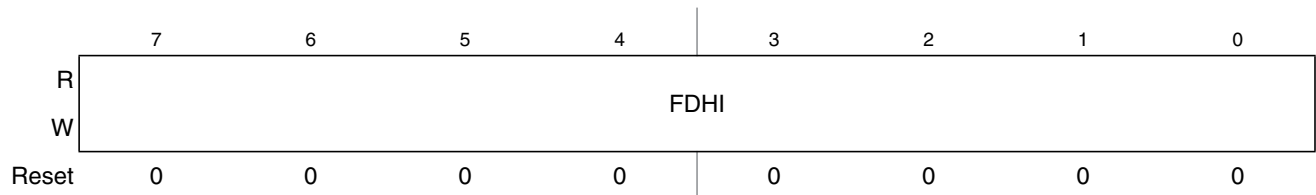
**Figure 21-14. Flash Address Low Register (FADDRLO)**

In normal modes, all FABHI and FABLO bits read 0 and are not writable. In special modes, the FABHI and FABLO bits are readable and writable. For sector erase, the MCU address bits [9:0] are ignored. For mass erase, any address within the Flash array is valid to start the command.

### 21.3.2.10 Flash Data Register (FDATA)

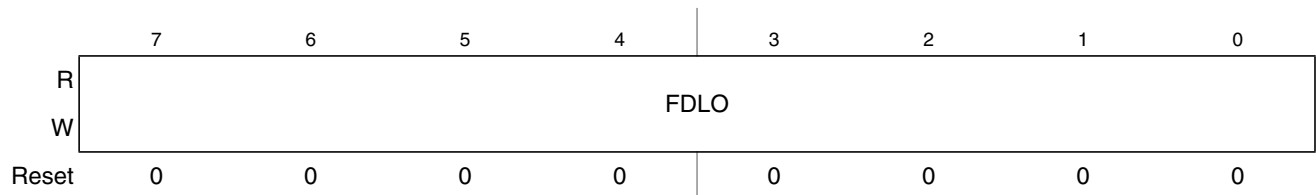
FDATAHI and FDATALO are the Flash data registers.

Module Base + 0x000A



**Figure 21-15. Flash Data High Register (FDATAHI)**

Module Base + 0x000B



**Figure 21-16. Flash Data Low Register (FDATALO)**

In normal modes, all FDATAHI and FDATALO bits read 0 and are not writable. In special modes, all FDATAHI and FDATALO bits are readable and writable when writing to an address within the Flash address range.

### 21.3.2.11 RESERVED3

This register is reserved for factory testing and is not accessible to the user.

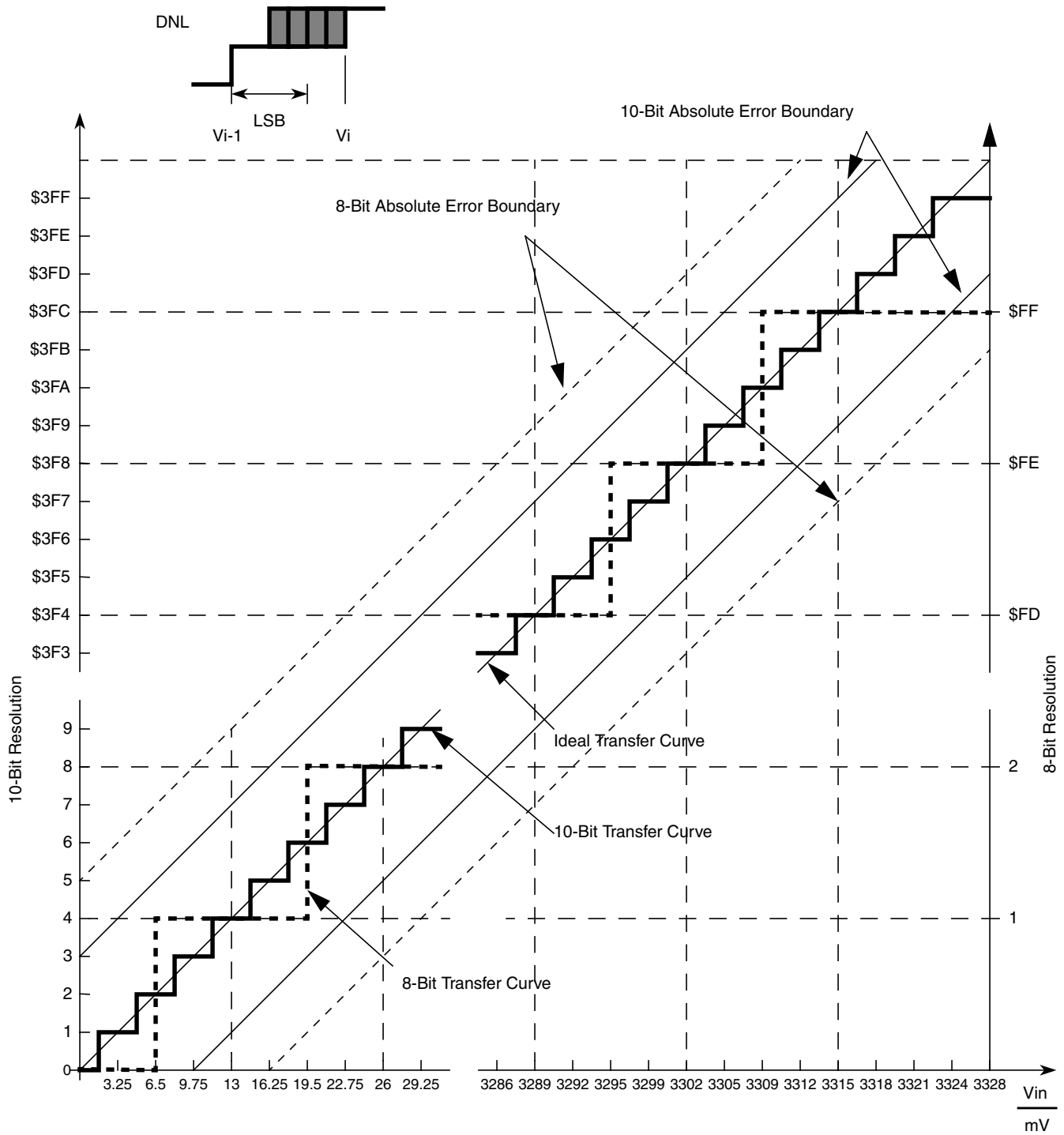


Figure A-1. ATD Accuracy Definitions

**NOTE**

Figure A-1 shows only definitions, for specification values refer to [Table A-12](#).