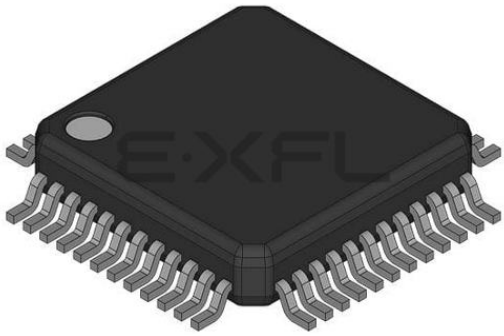

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	HCS12
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, EBI/EMI, SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	31
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9s12c32mfae16

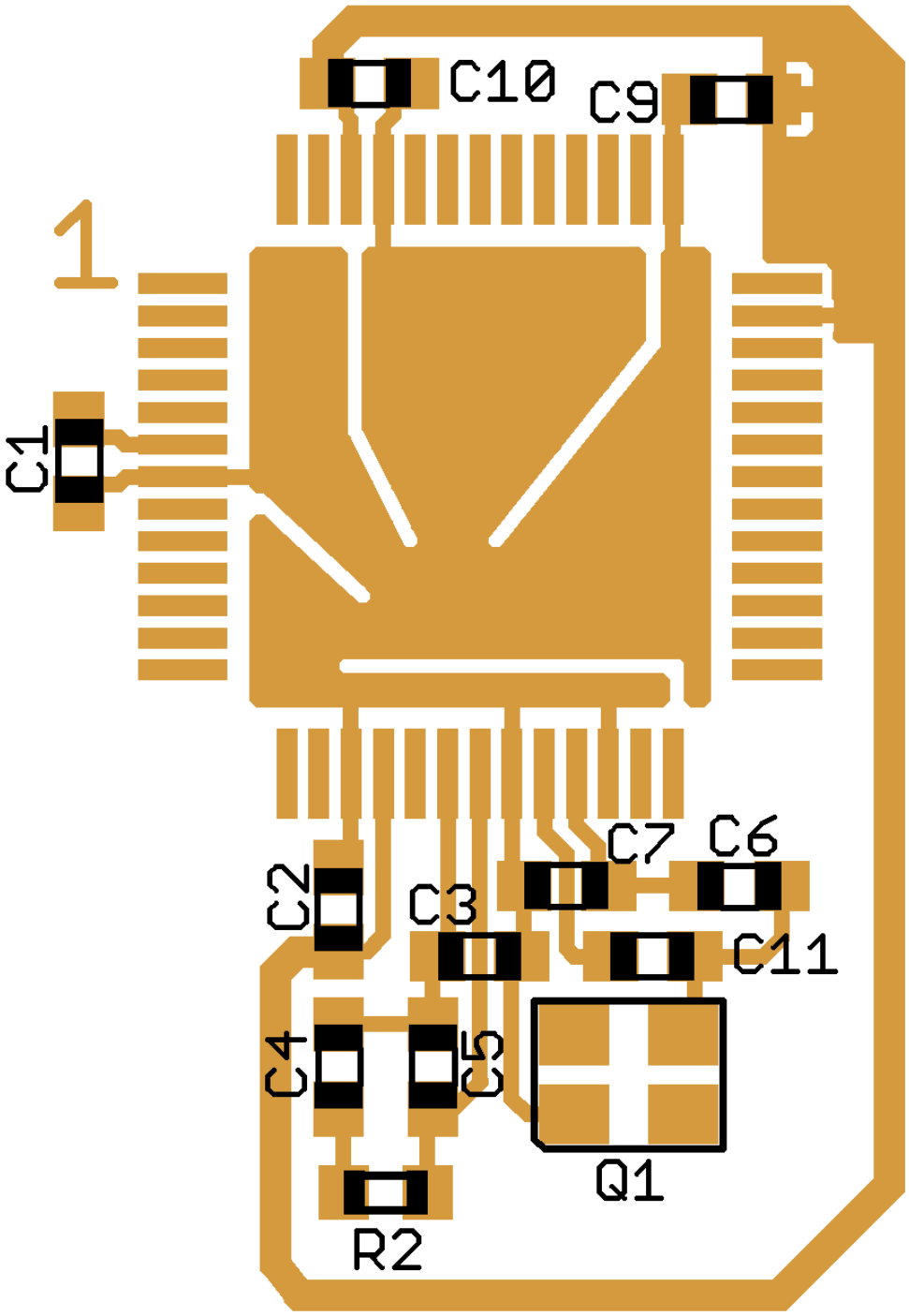

Figure 1-16. Recommended PCB Layout (52 LQFP) Colpitts Oscillator

2.3.2 Register Descriptions

Table 2-2 summarizes the effect on the various configuration bits — data direction (DDR), input/output level (I/O), reduced drive (RDR), pull enable (PE), pull select (PS), and interrupt enable (IE) for the ports. The configuration bit PS is used for two purposes:

1. Configure the sensitive interrupt edge (rising or falling), if interrupt is enabled.
2. Select either a pull-up or pull-down device if PE is active.

Table 2-2. Pin Configuration Summary

DDR	IO	RDR	PE	PS	IE[1]	Function	Pull Device	Interrupt
0	X	X	0	X	0	Input	Disabled	Disabled
0	X	X	1	0	0	Input	Pull up	Disabled
0	X	X	1	1	0	Input	Pull down	Disabled
0	X	X	0	0	1	Input	Disabled	Falling edge
0	X	X	0	1	1	Input	Disabled	Rising edge
0	X	X	1	0	1	Input	Pull up	Falling edge
0	X	X	1	1	1	Input	Pull down	rising edge
1	0	0	X	X	0	Output, full drive to 0	Disabled	Disabled
1	1	0	X	X	0	Output, full drive to 1	Disabled	Disabled
1	0	1	X	X	0	Output, reduced drive to 0	Disabled	Disabled
1	1	1	X	X	0	Output, reduced drive to 1	Disabled	Disabled
1	0	0	X	0	1	Output, full drive to 0	Disabled	Falling edge
1	1	0	X	1	1	Output, full drive to 1	Disabled	Rising edge
1	0	1	X	0	1	Output, reduced drive to 0	Disabled	Falling edge
1	1	1	X	1	1	Output, reduced drive to 1	Disabled	Rising edge

1. Applicable only on ports P and J.

NOTE

All bits of all registers in this module are completely synchronous to internal clocks during a register read.

2.3.2.3.4 Port M Reduced Drive Register (RDRM)

Module Base + 0x0013

	7	6	5	4	3	2	1	0
R	0	0	RDRM5	RDRM4	RDRM3	RDRM2	RDRM1	RDRM0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 2-20. Port M Reduced Drive Register (RDRM)

Read: Anytime.

Write: Anytime.

Table 2-18. RDRM Field Descriptions

Field	Description
5–0 RDRM[5:0]	**Reduced Drive Port M** — This register configures the drive strength of each port M output pin as either full or reduced. If the port is used as input this bit is ignored. 0 Full drive strength at output. 1 Associated pin drives at about 1/3 of the full drive strength.

2.3.2.3.5 Port M Pull Device Enable Register (PERM)

Module Base + 0x0014

	7	6	5	4	3	2	1	0
R	0	0	PERM5	PERM4	PERM3	PERM2	PERM1	PERM0
W								
Reset	0	0	1	1	1	1	1	1

= Unimplemented or Reserved

Figure 2-21. Port M Pull Device Enable Register (PERM)

Read: Anytime.

Write: Anytime.

Table 2-19. PERM Field Descriptions

Field	Description
5–0 PERM[5:0]	**Pull Device Enable Port M** — This register configures whether a pull-up or a pull-down device is activated, if the port is used as input or as output in wired-or (open drain) mode. This bit has no effect if the port is used as push-pull output. Out of reset a pull-up device is enabled. 0 Pull-up or pull-down device is disabled. 1 Either a pull-up or pull-down device is enabled.

Table 3-9. Allocated RAM Memory Space (continued)

ram_sw2:ram_sw0	Allocated RAM Space	RAM Mappable Region	INITRM Bits Used	RAM Reset Base Address(1)
011	8K bytes	8K bytes	RAM[15:13]	0x0000
100	10K bytes	16K bytes [2]	RAM[15:14]	0x1800
101	12K bytes	16K bytes [2]	RAM[15:14]	0x1000
110	14K bytes	16K bytes [2]	RAM[15:14]	0x0800
111	16K bytes	16K bytes	RAM[15:14]	0x0000

1. The RAM Reset BASE Address is based on the reset value of the INITRM register, 0x0009.
2. Alignment of the Allocated RAM space within the RAM mappable region is dependent on the value of RAMHAL.

NOTE

As stated, the bits in this register provide read visibility to the system physical memory space allocations defined at system integration. The actual array size for any given type of memory block may differ from the allocated size. Please refer to the device overview chapter for actual sizes.

3.3.2.8 Memory Size Register 1 (MEMSIZ1)

Module Base + 0x001D
Starting address location affected by INITRG register setting.

	7	6	5	4	3	2	1	0
R	ROM_SW1	ROM_SW0	0	0	0	0	PAG_SW1	PAG_SW0
W								
Reset	—	—	—	—	—	—	—	—

= Unimplemented or Reserved

Figure 3-10. Memory Size Register 1 (MEMSIZ1)

Read: Anytime

Write: Writes have no effect

Reset: Defined at chip integration, see device overview section.

The MEMSIZ1 register reflects the state of the FLASH or ROM physical memory space and paging switches at the core boundary which are configured at system integration. This register allows read visibility to the state of these switches.

4.3.1 Module Memory Map

Table 4-2. MEBI Memory Map

Address Offset	Use	Access
0x0000	Port A Data Register (PORTA)	R/W
0x0001	Port B Data Register (PORTB)	R/W
0x0002	Data Direction Register A (DDRA)	R/W
0x0003	Data Direction Register B (DDRB)	R/W
0x0004	Reserved	R
0x0005	Reserved	R
0x0006	Reserved	R
0x0007	Reserved	R
0x0008	Port E Data Register (PORTE)	R/W
0x0009	Data Direction Register E (DDRE)	R/W
0x000A	Port E Assignment Register (PEAR)	R/W
0x000B	Mode Register (MODE)	R/W
0x000C	Pull Control Register (PUCR)	R/W
0x000D	Reduced Drive Register (RDRIV)	R/W
0x000E	External Bus Interface Control Register (EBICTL)	R/W
0x000F	Reserved	R
0x001E	IRQ Control Register (IRQCR)	R/W
0x00032	Port K Data Register (PORTK)	R/W
0x00033	Data Direction Register K (DDRK)	R/W

4.3.2 Register Descriptions

4.3.2.1 Port A Data Register (PORTA)

Module Base + 0x0000
Starting address location affected by INITRG register setting.

	7	6	5	4	3	2	1	0
R W	Bit 7	6	5	4	3	2	1	Bit 0
Reset	0	0	0	0	0	0	0	0
Single Chip	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Expanded Wide, Emulation Narrow with IVIS, and Peripheral	AB/DB15	AB/DB14	AB/DB13	AB/DB12	AB/DB11	AB/DB10	AB/DB9	AB/DB8
Expanded Narrow	AB15 and DB15/DB7	AB14 and DB14/DB6	AB13 and DB13/DB5	AB12 and DB12/DB4	AB11 and DB11/DB3	AB10 and DB10/DB2	AB9 and DB9/DB1	AB8 and DB8/DB0

Figure 4-2. Port A Data Register (PORTA)

5.2 External Signal Description

Most interfacing with the interrupt sub-block is done within the core. However, the interrupt does receive direct input from the multiplexed external bus interface (MEBI) sub-block of the core for the $\overline{IRQ}$ and $\overline{XIRQ}$ pin data.

5.3 Memory Map and Register Definition

Detailed descriptions of the registers and associated bits are given in the subsections that follow.

5.3.1 Module Memory Map

Table 5-1. INT Memory Map

Address Offset	Use	Access
0x0015	Interrupt Test Control Register (ITCR)	R/W
0x0016	Interrupt Test Registers (ITEST)	R/W
0x001F	Highest Priority Interrupt (Optional) (HPRIO)	R/W

5.3.2 Register Descriptions

5.3.2.1 Interrupt Test Control Register

Module Base + 0x0015
Starting address location affected by INITRG register setting.

	7	6	5	4	3	2	1	0
R	0	0	0	WRTINT	ADR3	ADR2	ADR1	ADR0
W								
Reset	0	0	0	0	1	1	1	1

= Unimplemented or Reserved

Figure 5-2. Interrupt Test Control Register (ITCR)

Read: See individual bit descriptions

Write: See individual bit descriptions

8.1.2.2 MCU Operating Modes

- **Stop Mode**

  Entering stop mode causes all clocks to halt and thus the system is placed in a minimum power standby mode. This aborts any conversion sequence in progress. During recovery from stop mode, there must be a minimum delay for the stop recovery time, t_{SR}, before initiating a new ATD conversion sequence.

- **Wait Mode**

  Entering wait mode the ATD conversion either continues or aborts for low power depending on the logical value of the AWAIT bit.

- **Freeze Mode**

  In freeze mode the ATD10B8C will behave according to the logical values of the FRZ1 and FRZ0 bits. This is useful for debugging and emulation.

8.1.3 Block Diagram

Figure 8-1 is a block diagram of the ATD.

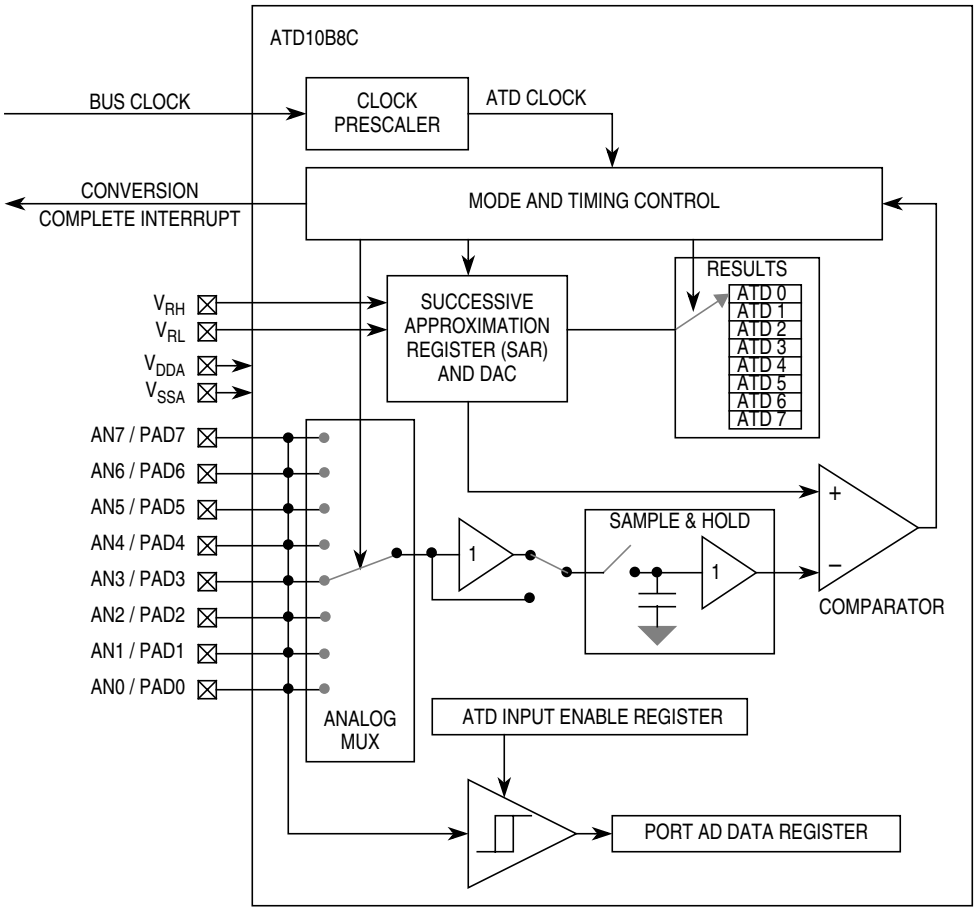

Figure 8-1. ATD10B8C Block Diagram

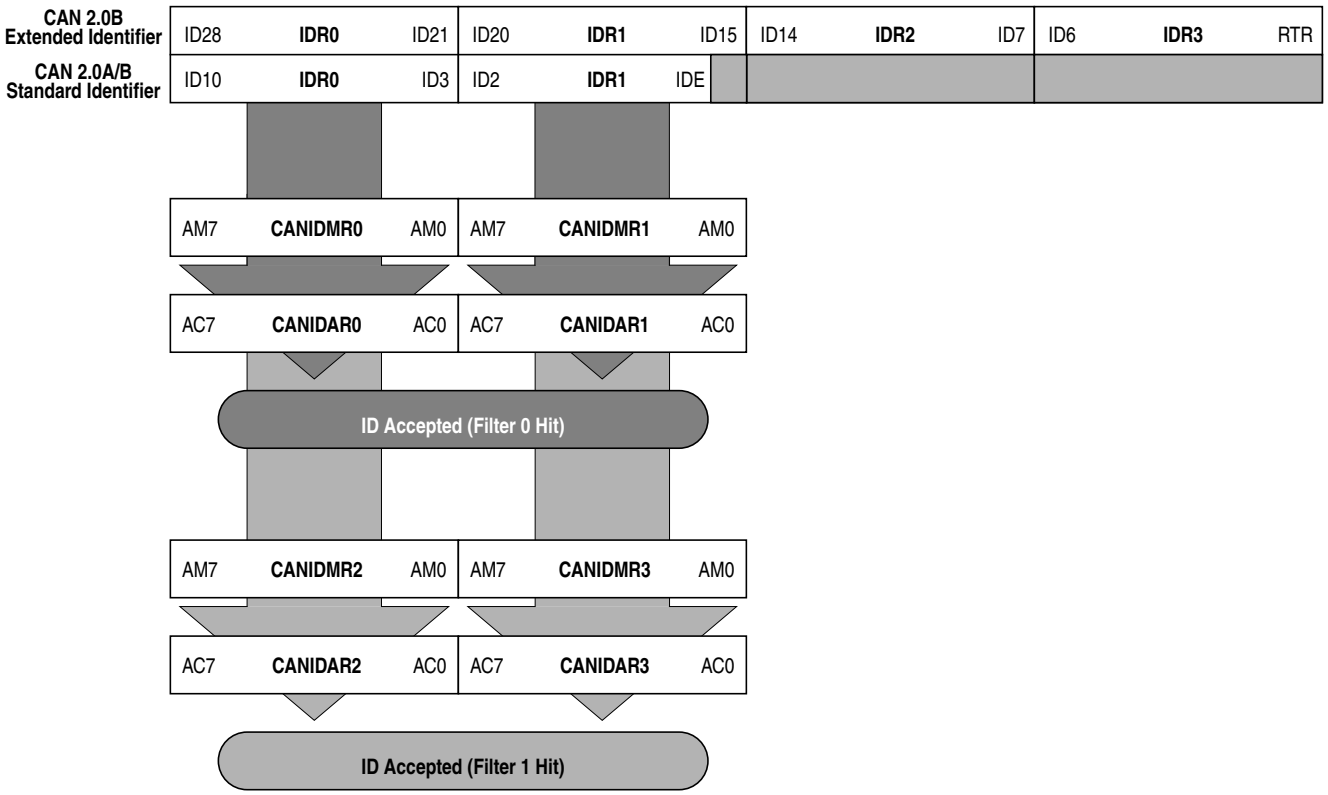

Figure 10-40. 16-bit Maskable Identifier Acceptance Filters

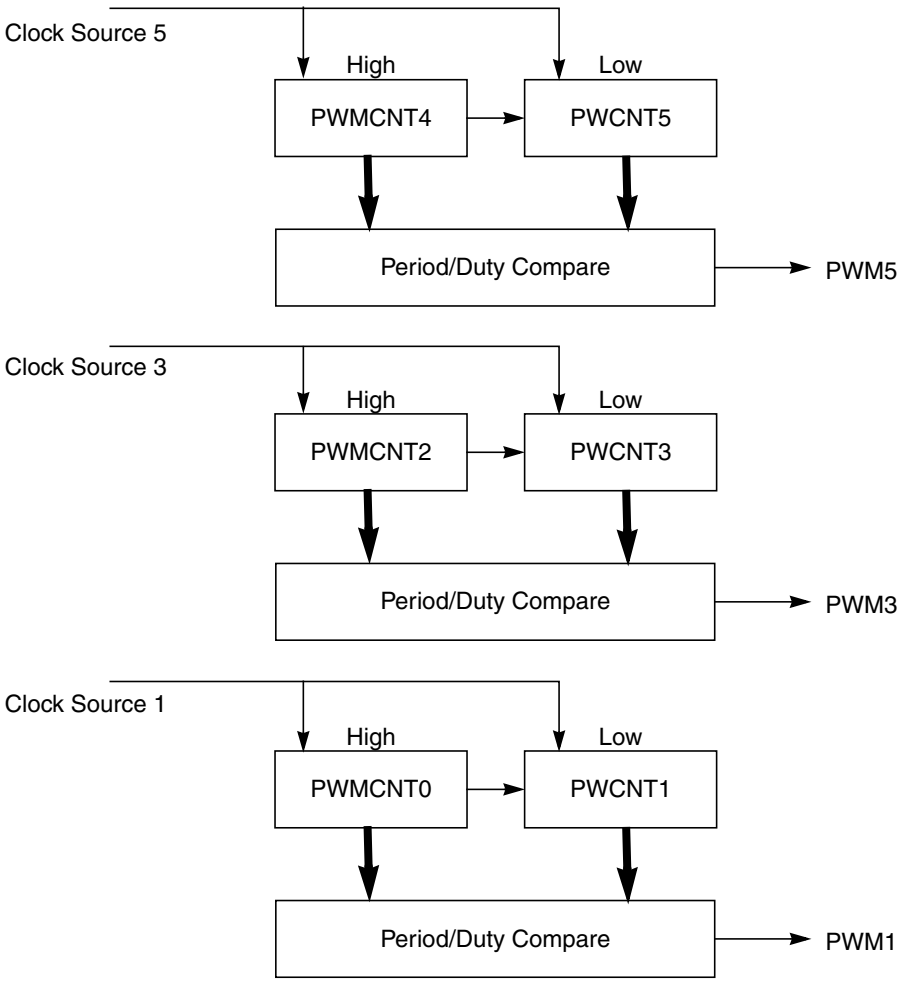

Figure 12-40. PWM 16-Bit Mode

When using the 16-bit concatenated mode, the clock source is determined by the low-order 8-bit channel clock select control bits. That is channel 5 when channels 4 and 5 are concatenated, channel 3 when channels 2 and 3 are concatenated, and channel 1 when channels 0 and 1 are concatenated. The resulting PWM is output to the pins of the corresponding low-order 8-bit channel as also shown in Figure 12-40. The polarity of the resulting PWM output is controlled by the PPOLx bit of the corresponding low-order 8-bit channel as well.

After concatenated mode is enabled (CONxx bits set in PWMCTL register), enabling/disabling the corresponding 16-bit PWM channel is controlled by the low-order PWMEx bit. In this case, the high-order bytes PWMEx bits have no effect and their corresponding PWM output is disabled.

In concatenated mode, writes to the 16-bit counter by using a 16-bit access or writes to either the low or high-order byte of the counter will reset the 16-bit counter. Reads of the 16-bit counter must be made by 16-bit access to maintain data coherency.

Either left aligned or center aligned output mode can be used in concatenated mode and is controlled by the low-order CAEx bit. The high-order CAEx bit has no effect.

13.4.4.2 Character Reception

During an SCI reception, the receive shift register shifts a frame in from the **Rx input** signal. The SCI data register is the read-only buffer between the internal data bus and the receive shift register.

After a complete frame shifts into the receive shift register, the data portion of the frame transfers to the SCI data register. The receive data register full flag, RDRF, in SCI status register 1 (SCISR1) becomes set, indicating that the received byte can be read. If the receive interrupt enable bit, RIE, in SCI control register 2 (SCICR2) is also set, the RDRF flag generates an RDRF interrupt request.

13.4.4.3 Data Sampling

The receiver samples the **Rx input** signal at the RT clock rate. The RT clock is an internal signal with a frequency 16 times the baud rate. To adjust for baud rate mismatch, the RT clock (see Figure 13-13) is re-synchronized:

- After every start bit
- After the receiver detects a data bit change from logic 1 to logic 0 (after the majority of data bit samples at RT8, RT9, and RT10 returns a valid logic 1 and the majority of the next RT8, RT9, and RT10 samples returns a valid logic 0)

To locate the start bit, data recovery logic does an asynchronous search for a logic 0 preceded by three logic 1s.When the falling edge of a possible start bit occurs, the RT clock begins to count to 16.

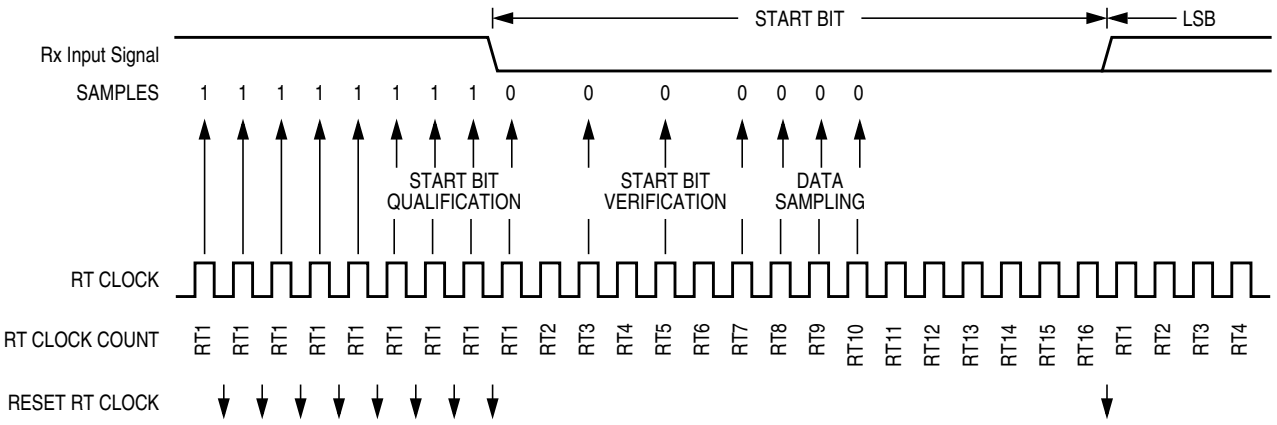

Figure 13-13. Receiver Data Sampling

To verify the start bit and to detect noise, data recovery logic takes samples at RT3, RT5, and RT7. Table 13-11 summarizes the results of the start bit verification samples.

Table 13-11. Start Bit Verification

RT3, RT5, and RT7 Samples	Start Bit Verification	Noise Flag
000	Yes	0
001	Yes	1
010	Yes	1
011	No	0

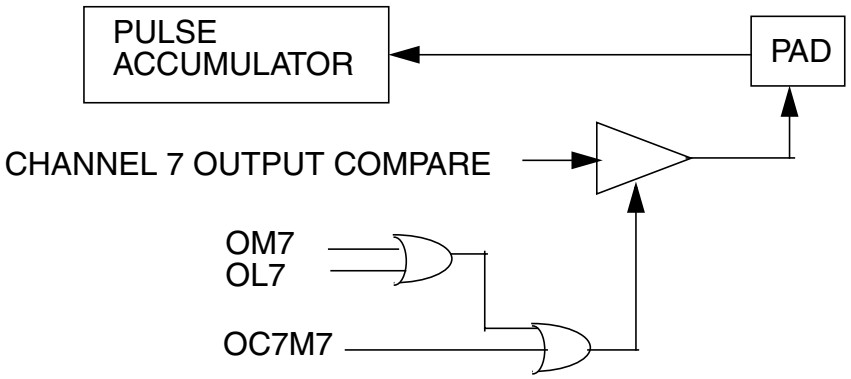

Figure 15-4. Channel 7 Output Compare/Pulse Accumulator Logic

NOTE

For more information see the respective functional descriptions in Section 15.4, "Functional Description," of this document.

15.2 External Signal Description

The TIM16B8CV1 module has a total of eight external pins.

15.2.1 IOC7 — Input Capture and Output Compare Channel 7 Pin

This pin serves as input capture or output compare for channel 7. This can also be configured as pulse accumulator input.

15.2.2 IOC6 — Input Capture and Output Compare Channel 6 Pin

This pin serves as input capture or output compare for channel 6.

15.2.3 IOC5 — Input Capture and Output Compare Channel 5 Pin

This pin serves as input capture or output compare for channel 5.

15.2.4 IOC4 — Input Capture and Output Compare Channel 4 Pin

This pin serves as input capture or output compare for channel 4. Pin

15.2.5 IOC3 — Input Capture and Output Compare Channel 3 Pin

This pin serves as input capture or output compare for channel 3.

16.2 External Signal Description

Due to the nature of VREG3V3V2 being a voltage regulator providing the chip internal power supply voltages most signals are power supply signals connected to pads.

Table 16-1 shows all signals of VREG3V3V2 associated with pins.

Table 16-1. VREG3V3V2 — Signal Properties

Name	Port	Function	Reset State	Pull Up
V_{DDR}	—	VREG3V3V2 power input (positive supply)	—	—
V_{DDA}	—	VREG3V3V2 quiet input (positive supply)	—	—
V_{SSA}	—	VREG3V3V2 quiet input (ground)	—	—
V_{DD}	—	VREG3V3V2 primary output (positive supply)	—	—
V_{SS}	—	VREG3V3V2 primary output (ground)	—	—
V_{DDPLL}	—	VREG3V3V2 secondary output (positive supply)	—	—
V_{SSPLL}	—	VREG3V3V2 secondary output (ground)	—	—
V_{REGEN} (optional)	—	VREG3V3V2 (Optional) Regulator Enable	—	—

NOTE

Check device overview chapter for connectivity of the signals.

16.2.1 V_{DDR} — Regulator Power Input

Signal V_{DDR} is the power input of VREG3V3V2. All currents sourced into the regulator loads flow through this pin. A chip external decoupling capacitor (100 nF...220 nF, X7R ceramic) between V_{DDR} and V_{SSR} can smoothen ripple on V_{DDR}.

For entering Shutdown Mode, pin V_{DDR} should also be tied to ground on devices without a V_{REGEN} pin.

16.2.2 V_{DDA}, V_{SSA} — Regulator Reference Supply

Signals V_{DDA}/V_{SSA} which are supposed to be relatively quiet are used to supply the analog parts of the regulator. Internal precision reference circuits are supplied from these signals. A chip external decoupling capacitor (100 nF...220 nF, X7R ceramic) between V_{DDA} and V_{SSA} can further improve the quality of this supply.

Module Base + 0x000F

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 17-20. RESERVED6

All bits read 0 and are not writable.

17.4 Functional Description

17.4.1 Flash Command Operations

Write operations are used for the program, erase, and erase verify algorithms described in this section. The program and erase algorithms are controlled by a state machine whose timebase FCLK is derived from the oscillator clock via a programmable divider. The FCMD register as well as the associated FADDR and FDATA registers operate as a buffer and a register (2-stage FIFO) so that a new command along with the necessary data and address can be stored to the buffer while the previous command is still in progress. This pipelined operation allows a time optimization when programming more than one word on a specific row, as the high voltage generation can be kept active in between two programming commands. The pipelined operation also allows a simplification of command launching. Buffer empty as well as command completion are signalled by flags in the FSTAT register with corresponding interrupts generated, if enabled.

The next sections describe:

- How to write the FCLKDIV register
- Command write sequence used to program, erase or erase verify the Flash array
- Valid Flash commands
- Errors resulting from illegal Flash operations

17.4.1.1 Writing the FCLKDIV Register

Prior to issuing any Flash command after a reset, it is first necessary to write the FCLKDIV register to divide the oscillator clock down to within the 150-kHz to 200-kHz range. Since the program and erase timings are also a function of the bus clock, the FCLKDIV determination must take this information into account.

If we define:

- FCLK as the clock of the Flash timing control block
- Tbus as the period of the bus clock
- INT(x) as taking the integer part of x (e.g., INT(4.323) = 4),

Table 18-12. Flash Protection Scenario Transitions

From Protection Scenario	To Protection Scenario[1]							
	0	1	2	3	4	5	6	7
6		X		X	X		X	
7	X	X	X	X	X	X	X	X

1. Allowed transitions marked with X.

18.3.2.6 Flash Status Register (FSTAT)

The FSTAT register defines the status of the Flash command controller and the results of command execution.

Module Base + 0x0005

	7	6	5	4	3	2	1	0
R	CBEIF	CCIF	PVIOL	ACCERR	0	BLANK	FAIL	DONE
W								
Reset	1	1	0	0	0	0	0	1

= Unimplemented or Reserved

Figure 18-10. Flash Status Register (FSTAT)

In normal modes, bits CBEIF, PVIOL, and ACCERR are readable and writable, bits CCIF and BLANK are readable and not writable, remaining bits, including FAIL and DONE, read 0 and are not writable. In special modes, FAIL is readable and writable while DONE is readable but not writable. FAIL must be clear in special modes when starting a command write sequence.

Table 18-13. FSTAT Field Descriptions

Field	Description
7 CBEIF	**Command Buffer Empty Interrupt Flag** — The CBEIF flag indicates that the address, data and command buffers are empty so that a new command write sequence can be started. The CBEIF flag is cleared by writing a 1 to CBEIF. Writing a 0 to the CBEIF flag has no effect on CBEIF. Writing a 0 to CBEIF after writing an aligned word to the Flash address space but before CBEIF is cleared will abort a command write sequence and cause the ACCERR flag in the FSTAT register to be set. Writing a 0 to CBEIF outside of a command write sequence will not set the ACCERR flag. The CBEIF flag is used together with the CBEIE bit in the FCNFG register to generate an interrupt request (see Figure 18-26). 0 Buffers are full 1 Buffers are ready to accept a new command
6 CCIF	**Command Complete Interrupt Flag** — The CCIF flag indicates that there are no more commands pending. The CCIF flag is cleared when CBEIF is clear and sets automatically upon completion of all active and pending commands. The CCIF flag does not set when an active commands completes and a pending command is fetched from the command buffer. Writing to the CCIF flag has no effect. The CCIF flag is used together with the CCIE bit in the FCNFG register to generate an interrupt request (see Figure 18-26). 0 Command in progress 1 All commands are completed

Chapter 19
64 Kbyte Flash Module (S12FTS64KV4)

19.1 Introduction

The FTS128K1FTS64K module implements a 12864 Kbyte Flash (nonvolatile) memory. The Flash memory contains one array of 12864 Kbytes organized as 1024512 rows of 128128 bytes with an erase sector size of eight rows (10241024 bytes). The Flash array may be read as either bytes, aligned words, or misaligned words. Read access time is one bus cycle for byte and aligned word, and two bus cycles for misaligned words.

The Flash array is ideal for program and data storage for single-supply applications allowing for field reprogramming without requiring external voltage sources for program or erase. Program and erase functions are controlled by a command driven interface. The Flash module supports both mass erase and sector erase. An erased bit reads 1 and a programmed bit reads 0. The high voltage required to program and erase is generated internally. It is not possible to read from a Flash array while it is being erased or programmed.

CAUTION

A Flash word must be in the erased state before being programmed. Cumulative programming of bits within a Flash word is not allowed.

19.1.1 Glossary

Command Write Sequence — A three-step MCU instruction sequence to program, erase, or erase verify the Flash array memory.

19.1.2 Features

- 12864 Kbytes of Flash memory comprised of one 12864 Kbyte array divided into 12864 sectors of 10241024 bytes
- Automated program and erase algorithm
- Interrupts on Flash command completion and command buffer empty
- Fast sector erase and word program operation
- 2-stage command pipeline for faster multi-word program times
- Flexible protection scheme to prevent accidental program or erase
- Single power supply for Flash program and erase operations
- Security feature to prevent unauthorized access to the Flash array memory

Table A-9. Supply Current Characteristics for Other Family Members

Conditions are shown in Table A-4 with internal regulator enabled unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Run Supply Current Single Chip,	I_{DD5}	—	—	45	mA
2		Wait Supply current	I_{DDW}				mA
	P	All modules enabled		—	—	33	
	P	VDDR<4.9V, only RTI enabled[2]		—	2.5	8	
	C	VDDR>4.9V, only RTI enabled		—	3.5	—	
6		Pseudo Stop Current (RTI and COP disabled)[23]	I_{DDPS}[(1)]				µA
	C	–40°C		—	190	—	
	P	27°C		—	200	250	
	C	85°C		—	300	—	
	P	"C" Temp Option 100˚C		—	400	1400	
	C	105°C		—	450	—	
	P	"V" Temp Option 120˚C		—	600	1900	
	C	125°C		—	650	—	
	P	"M" Temp Option 140°C		—	1000	4800	
4		Pseudo Stop Current (RTI and COP enabled)[(2) (3)]	I_{DDPS}[1]				µA
	C	–40°C		—	370	—	
	C	27°C		—	500	—	
	C	85°C		—	590	—	
	C	105°C		—	780	—	
	C	125°C		—	1200	—	
5		Stop Current [3]	I_{DDS}[1]				µA
	C	–40°C		—	12	—	
	P	27°C		—	25	100	
	C	85°C		—	130	—	
	P	"C" Temp Option 100˚C		—	160	1200	
	C	105°C		—	200	—	
	P	"V" Temp Option 120˚C		—	350	1700	
	C	125°C		—	400	—	
	P	"M" Temp Option 140°C		—	600	4500	

1. STOP current measured in production test at increased junction temperature, hence for Temp Option "C" the test is carried out at 100˚C although the Temperature specification is 85˚C. Similarly for "v" and "M" options the temperature used in test lies 15˚C above the temperature option specification.
2. PLL off
3. At those low power dissipation levels $T_J = T_A$ can be assumed

A.3 MSCAN

Table A-14. MSCAN Wake-up Pulse Characteristics

Conditions are shown in Table A-4 unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	MSCAN Wake-up dominant pulse filtered	t_{WUP}	—	—	2	us
2	P	MSCAN Wake-up dominant pulse pass	t_{WUP}	5	—	—	us

A.4 Reset, Oscillator and PLL

This section summarizes the electrical characteristics of the various startup scenarios for Oscillator and Phase-Locked-Loop (PLL).

A.4.1 Startup

Table A-15 summarizes several startup characteristics explained in this section. Detailed description of the startup behavior can be found in the Clock and Reset Generator (CRG) Block User Guide.

Table A-15. Startup Characteristics

Conditions are shown in Table A-4 unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	T	POR release level	V_{PORR}	—	—	2.07	V
2	T	POR assert level	V_{PORA}	0.97	—	—	V
3	D	Reset input pulse width, minimum input time	PW_{RSTL}	2	—	—	t_{osc}
4	D	Startup from Reset	n_{RST}	192	—	196	n_{osc}
5	D	Interrupt pulse width, $\overline{IRQ}$ edge-sensitive mode	PW_{IRQ}	20	—	—	ns
6	D	Wait recovery startup time	t_{WRS}	—	—	14	t_{cyc}

A.4.1.1 POR

The release level V_{PORR} and the assert level V_{PORA} are derived from the V_{DD} supply. They are also valid if the device is powered externally. After releasing the POR reset the oscillator and the clock quality check are started. If after a time t_{CQOUT} no valid oscillation is detected, the MCU will start using the internal self clock. The fastest startup time possible is given by n_{uposc}.

A.4.1.2 LVR

The release level V_{LVRR} and the assert level V_{LVRA} are derived from the V_{DD} supply. They are also valid if the device is powered externally. After releasing the LVR reset the oscillator and the clock quality check are started. If after a time t_{CQOUT} no valid oscillation is detected, the MCU will start using the internal self clock. The fastest startup time possible is given by n_{uposc}.

Appendix E
Ordering Information

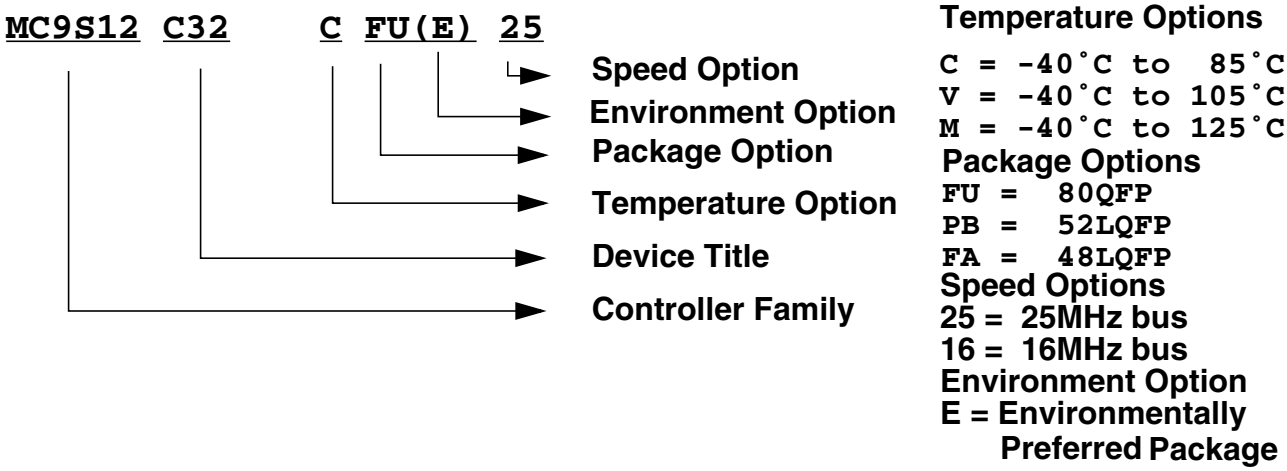

Figure E-1. Order Part number Coding

Table E-1. lists C-family part number coding based on package, speed and temperature and die options.

Table E-2. lists CG-family part number coding based on package, speed and temperature and die options.

Table E-1. MC9S12C-Family / MC9S12GC-Family Part Number Coding

Part Number	Mask[1] set	Temp.	Package	Speed	Die Type	Flash	RAM	I/O[2], [3]
MC9S12C128CFA	XL09S/0M66G	-40˚C, 85˚C	48LQFP	25MHz	C128 die	128K	4K	31
MC9S12C128CPB	XL09S/0M66G	-40˚C, 85˚C	52LQFP	25MHz	C128 die	128K	4K	35
MC9S12C128CFU	XL09S/0M66G	-40˚C, 85˚C	80QFP	25MHz	C128 die	128K	4K	60
MC9S12C128VFA	XL09S/0M66G	-40˚C,105˚C	48LQFP	25MHz	C128 die	128K	4K	31
MC9S12C128VPB	XL09S/0M66G	-40˚C,105˚C	52LQFP	25MHz	C128 die	128K	4K	35
MC9S12C128VFU	XL09S/0M66G	-40˚C, 105˚C	80QFP	25MHz	C128 die	128K	4K	60
MC9S12C128MFA	XL09S/0M66G	-40˚C,125˚C	48LQFP	25MHz	C128 die	128K	4K	31
MC9S12C128MPB	XL09S/0M66G	-40˚C,125˚C	52LQFP	25MHz	C128 die	128K	4K	35
MC9S12C128MFU	XL09S/0M66G	-40˚C, 125˚C	80QFP	25MHz	C128 die	128K	4K	60
MC9S12C96CFA	XL09S/0M66G	-40˚C, 85˚C	48LQFP	25MHz	C128 die	96K	4K	31
MC9S12C96CPB	XL09S/0M66G	-40˚C, 85˚C	52LQFP	25MHz	C128 die	96K	4K	35
MC9S12C96CFU	XL09S/0M66G	-40˚C, 85˚C	80QFP	25MHz	C128 die	96K	4K	60
MC9S12C96VFA	XL09S/0M66G	-40˚C,105˚C	48LQFP	25MHz	C128 die	96K	4K	31
MC9S12C96VPB	XL09S/0M66G	-40˚C,105˚C	52LQFP	25MHz	C128 die	96K	4K	35
MC9S12C96VFU	XL09S/0M66G	-40˚C, 105˚C	80QFP	25MHz	C128 die	96K	4K	60
MC9S12C96MFA	XL09S/0M66G	-40˚C,125˚C	48LQFP	25MHz	C128 die	96K	4K	31
MC9S12C96MPB	XL09S/0M66G	-40˚C,125˚C	52LQFP	25MHz	C128 die	96K	4K	35
MC9S12C96MFU	XL09S/0M66G	-40˚C, 125˚C	80QFP	25MHz	C128 die	96K	4K	60
MC9S12C64CFA	XL09S/0M66G	-40˚C, 85˚C	48LQFP	25MHz	C128 die	64K	4K	31
MC9S12C64CPB	XL09S/0M66G	-40˚C, 85˚C	52LQFP	25MHz	C128 die	64K	4K	35