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Details

Product Status	Active
Core Processor	HCS12
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, EBI/EMI, SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	31
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s12c32mfae25

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x005F	TC7 (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:	Bit 7	6	5	4	3	2	1	Bit 0
0x0060	PACTL	Read:	0	PAEN	PAMOD	PEDGE	CLK1	CLK0	PAOVI	PAI
		Write:	0	PAEN	PAMOD	PEDGE	CLK1	CLK0	PAOVI	PAI
0x0061	PAFLG	Read:	0	0	0	0	0	0	PAOVF	PAIF
		Write:	0	0	0	0	0	0	PAOVF	PAIF
0x0062	PACNT (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:	Bit 15	14	13	12	11	10	9	Bit 8
0x0063	PACNT (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:	Bit 7	6	5	4	3	2	1	Bit 0
0x0064	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:	0	0	0	0	0	0	0	0
0x0065	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:	0	0	0	0	0	0	0	0
0x0066	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:	0	0	0	0	0	0	0	0
0x0067	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:	0	0	0	0	0	0	0	0
0x0068	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:	0	0	0	0	0	0	0	0
0x0069	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:	0	0	0	0	0	0	0	0
0x006A	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:	0	0	0	0	0	0	0	0
0x006B	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:	0	0	0	0	0	0	0	0
0x006C	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:	0	0	0	0	0	0	0	0
0x006D	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:	0	0	0	0	0	0	0	0
0x006E	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:	0	0	0	0	0	0	0	0
0x006F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:	0	0	0	0	0	0	0	0

0x0070–0x007F Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0070–0x007F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:	0	0	0	0	0	0	0	0

1.3.2 Signal Properties Summary

Table 1-5. Signal Properties

Pin Name Function 1	Pin Name Function 2	Pin Name Function 3	Power Domain	Internal Pull Resistor		Description
				CTRL	Reset State	
EXTAL	—	—	V _{DDPLL}	NA	NA	Oscillator pins
XTAL	—	—	V _{DDPLL}	NA	NA	
RESET	—	—	V _{DDX}	None	None	External reset pin
XFC	—	—	V _{DDPLL}	NA	NA	PLL loop filter pin
TEST	V _{PP}	—	V _{SSX}	NA	NA	Test pin only
BKGD	MODC	TAGHI	V _{DDX}	Up	Up	Background debug, mode pin, tag signal high
PE7	NOACC	XCLKS	V _{DDX}	PUCR	Up	Port E I/O pin, access, clock select
PE6	IPIPE1	MODB	V _{DDX}	While RESET pin is low: Down		Port E I/O pin and pipe status
PE5	IPIPE0	MODA	V _{DDX}	While RESET pin is low: Down		Port E I/O pin and pipe status
PE4	ECLK	—	V _{DDX}	PUCR	Mode Dep ⁽¹⁾	Port E I/O pin, bus clock output
PE3	LSTRB	TAGLO	V _{DDX}	PUCR	Mode Dep ¹	Port E I/O pin, low strobe, tag signal low
PE2	R/W	—	V _{DDX}	PUCR	Mode Dep ¹	Port E I/O pin, R/W in expanded modes
PE1	IRQ	—	V _{DDX}	PUCR	Up	Port E input, external interrupt pin
PE0	XIRQ	—	V _{DDX}	PUCR	Up	Port E input, non-maskable interrupt pin
PA[7:3]	ADDR[15:1/ DATA[15:1]	—	V _{DDX}	PUCR	Disabled	Port A I/O pin and multiplexed address/data
PA[2:1]	ADDR[10:9/ DATA[10:9]	—	V _{DDX}	PUCR	Disabled	Port A I/O pin and multiplexed address/data
PA[0]	ADDR[8]/ DATA[8]	—	V _{DDX}	PUCR	Disabled	Port A I/O pin and multiplexed address/data
PB[7:5]	ADDR[7:5]/ DATA[7:5]	—	V _{DDX}	PUCR	Disabled	Port B I/O pin and multiplexed address/data
PB[4]	ADDR[4]/ DATA[4]	—	V _{DDX}	PUCR	Disabled	Port B I/O pin and multiplexed address/data
PB[3:0]	ADDR[3:0]/ DATA[3:0]	—	V _{DDX}	PUCR	Disabled	Port B I/O pin and multiplexed address/data
PAD[7:0]	AN[7:0]	—	V _{DDA}	PERAD/P PSAD	Disabled	Port AD I/O pins and ATD inputs
PP[7]	KWP[7]	—	V _{DDX}	PERP/ PPSP	Disabled	Port P I/O pins and keypad wake-up
PP[6]	KWP[6]	ROMCTL	V _{DDX}	PERP/ PPSP	Disabled	Port P I/O pins, keypad wake-up, and ROMON enable.
PP[5]	KWP[5]	PW5	V _{DDX}	PERP/ PPSP	Disabled	Port P I/O pin, keypad wake-up, PW5 output
PP[4:3]	KWP[4:3]	PW[4:3]	V _{DDX}	PERP/ PPSP	Disabled	Port P I/O pin, keypad wake-up, PWM output

the Flash EEPROM memory in the memory map (ROMCTL). At the rising edge of $\overline{\text{RESET}}$, the state of this pin is latched to the ROMON bit.

- PP6 = 1 in emulation modes equates to ROMON = 0 (ROM space externally mapped)
- PP6 = 0 in expanded modes equates to ROMON = 0 (ROM space externally mapped)

1.3.4.19 PP[5:0] / KWP[5:0] / PW[5:0] — Port P I/O Pins [5:0]

PP[5:0] are general purpose input or output pins, shared with the keypad interrupt function. When configured as inputs, they can generate interrupts causing the MCU to exit stop or wait mode.

PP[5:0] are also shared with the PWM output signals, PW[5:0]. Pins PP[2:0] are only available in the 80-pin package version. Pins PP[4:3] are not available in the 48-pin package version.

1.3.4.20 PJ[7:6] / KWJ[7:6] — Port J I/O Pins [7:6]

PJ[7:6] are general purpose input or output pins, shared with the keypad interrupt function. When configured as inputs, they can generate interrupts causing the MCU to exit stop or wait mode. These pins are not available in the 48-pin package version nor in the 52-pin package version.

1.3.4.21 PM5 / SCK — Port M I/O Pin 5

PM5 is a general purpose input or output pin and also the serial clock pin SCK for the serial peripheral interface (SPI).

1.3.4.22 PM4 / MOSI — Port M I/O Pin 4

PM4 is a general purpose input or output pin and also the master output (during master mode) or slave input (during slave mode) pin for the serial peripheral interface (SPI).

1.3.4.23 PM3 / $\overline{\text{SS}}$ — Port M I/O Pin 3

PM3 is a general purpose input or output pin and also the slave select pin $\overline{\text{SS}}$ for the serial peripheral interface (SPI).

1.3.4.24 PM2 / MISO — Port M I/O Pin 2

PM2 is a general purpose input or output pin and also the master input (during master mode) or slave output (during slave mode) pin for the serial peripheral interface (SPI).

1.3.4.25 PM1 / TXCAN — Port M I/O Pin 1

PM1 is a general purpose input or output pin and the transmit pin, TXCAN, of the CAN module if available.

1.3.4.26 PM0 / RXCAN — Port M I/O Pin 0

PM0 is a general purpose input or output pin and the receive pin, RXCAN, of the CAN module if available.

4.3.2.9 Mode Register (MODE)

Module Base + 0x000B

Starting address location affected by INITRG register setting.

	7	6	5	4	3	2	1	0
R	MODC	MODB	MODA	0	IVIS	0	EMK	EME
W								
Reset								
Special Single Chip	0	0	0	0	0	0	0	0
Emulation Expanded Narrow	0	0	1	0	1	0	1	1
Special Test	0	1	0	0	1	0	0	0
Emulation Expanded Wide	0	1	1	0	1	0	1	1
Normal Single Chip	1	0	0	0	0	0	0	0
Normal Expanded Narrow	1	0	1	0	0	0	0	0
Peripheral	1	1	0	0	0	0	0	0
Normal Expanded Wide	1	1	1	0	0	0	0	0

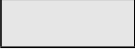
 = Unimplemented or Reserved

Figure 4-13. Mode Register (MODE)

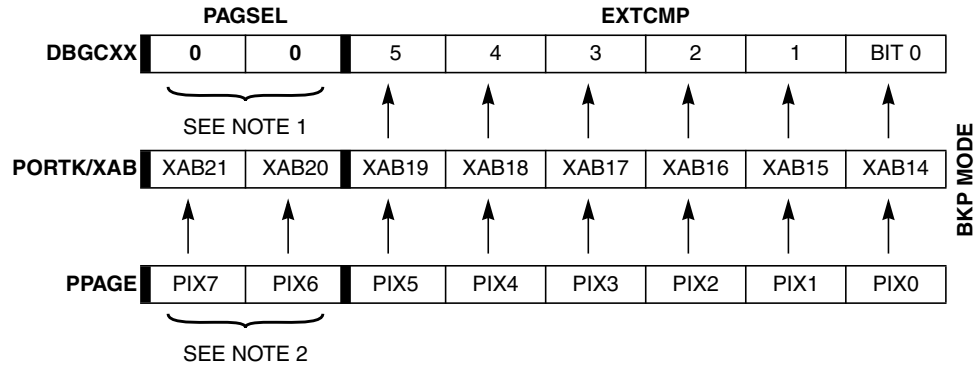
Read: Anytime (provided this register is in the map).

Write: Each bit has specific write conditions. Please refer to the descriptions of each bit on the following pages.

The MODE register is used to establish the operating mode and other miscellaneous functions (i.e., internal visibility and emulation of port E and K).

In special peripheral mode, this register is not accessible but it is reset as shown to system configuration features. Changes to bits in the MODE register are delayed one cycle after the write.

This register is not in the on-chip memory map in expanded and special peripheral modes. Therefore, these accesses will be echoed externally.



NOTES:

1. In BKP mode, PAGSEL has no functionality. Therefore, set PAGSEL to 00 (reset state).
2. Current HCS12 implementations are limited to six PPAGE bits, PIX[5:0].

Figure 7-16. Comparators A and B Extended Comparison in BKP Mode

7.3.2.10 Debug Comparator A Register (DBGCA)

Module Base + 0x002B

Starting address location affected by INITRG register setting.

	15	14	13	12	11	10	9	8
R	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W								
Reset	0	0	0	0	0	0	0	0

Figure 7-17. Debug Comparator A Register High (DBGCAH)

Module Base + 0x002C

Starting address location affected by INITRG register setting.

	7	6	5	4	3	2	1	0
R	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W								
Reset	0	0	0	0	0	0	0	0

Figure 7-18. Debug Comparator A Register Low (DBGCAL)

Table 7-21. DBGCA Field Descriptions

Field	Description
15:0	Comparator A Compare Bits — The comparator A compare bits control whether comparator A compares the address bus bits [15:0] to a logic 1 or logic 0. See Table 7-20 .
15:0	0 Compare corresponding address bit to a logic 0
	1 Compare corresponding address bit to a logic 1

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x000B ARMCOP	R	0	0	0	0	0	0	0	0
	W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

= Unimplemented or Reserved

Figure 9-3. CRG Register Summary (continued)

9.3.2.1 CRG Synthesizer Register (SYNR)

The SYNR register controls the multiplication factor of the PLL. If the PLL is on, the count in the loop divider (SYNR) register effectively multiplies up the PLL clock (PLLCLK) from the reference frequency by 2 x (SYNR+1). PLLCLK will not be below the minimum VCO frequency (f_{SCM}).

$$PLLCLK = 2 \times OSCCLK \times \frac{(SYNR + 1)}{(REFDV + 1)}$$

NOTE

If PLL is selected (PLLSEL=1), Bus Clock = PLLCLK / 2
 Bus Clock must not exceed the maximum operating system frequency.

Module Base + 0x0000

	7	6	5	4	3	2	1	0
R	0	0	SYN5	SYNR	SYN3	SYN2	SYN1	SYN0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 9-4. CRG Synthesizer Register (SYNR)

Read: anytime

Write: anytime except if PLLSEL = 1

NOTE

Write to this register initializes the lock detector bit and the track detector bit.

Table 9-4. CLKSEL Field Descriptions (continued)

Field	Description
2 CWA1	Core Stops in Wait Mode Bit — Write: anytime 0 Core clock keeps running in wait mode. 1 Core clock stops in wait mode.
1 RT1WA1	RT1 Stops in Wait Mode Bit — Write: anytime 0 RT1 keeps running in wait mode. 1 RT1 stops and initializes the RT1 dividers whenever the part goes into wait mode.
0 COPWA1	COP Stops in Wait Mode Bit — Normal modes: Write once —Special modes: Write anytime 0 COP keeps running in wait mode. 1 COP stops and initializes the COP dividers whenever the part goes into wait mode.

9.3.2.7 CRG PLL Control Register (PLLCTL)

This register controls the PLL functionality.

Module Base + 0x0006

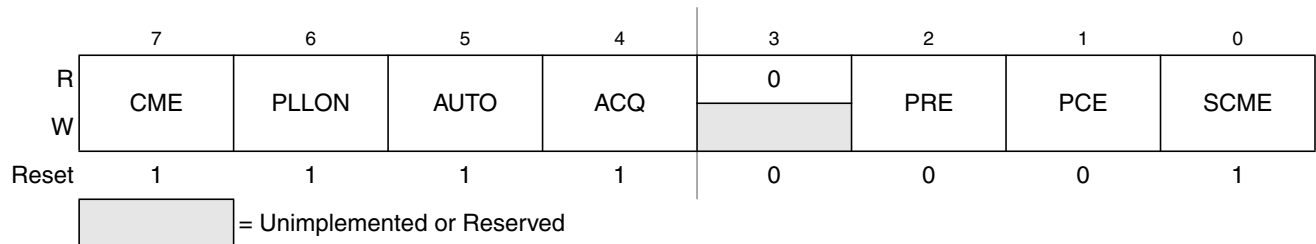


Figure 9-10. CRG PLL Control Register (PLLCTL)

Read: anytime

Write: refer to each bit for individual write conditions

Table 9-5. PLLCTL Field Descriptions

Field	Description
7 CME	Clock Monitor Enable Bit — CME enables the clock monitor. Write anytime except when SCM = 1. 0 Clock monitor is disabled. 1 Clock monitor is enabled. Slow or stopped clocks will cause a clock monitor reset sequence or self-clock mode. Note: Operating with CME = 0 will not detect any loss of clock. In case of poor clock quality this could cause unpredictable operation of the MCU. Note: In Stop Mode (PSTP = 0) the clock monitor is disabled independently of the CME bit setting and any loss of clock will not be detected.
6 PLLON	Phase Lock Loop On Bit — PLLON turns on the PLL circuitry. In self-clock mode, the PLL is turned on, but the PLLON bit reads the last latched value. Write anytime except when PLLSEL = 1. 0 PLL is turned off. 1 PLL is turned on. If AUTO bit is set, the PLL will lock automatically.

Module Base + 0x0018 (CANIDAR4)
 0x0019 (CANIDAR5)
 0x001A (CANIDAR6)
 0x001B (CANIDAR7)

	7	6	5	4	3	2	1	0
R	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
W								
Reset	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
R	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
W								
Reset	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
R	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
W								
Reset	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
R	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
W								
Reset	0	0	0	0	0	0	0	0

Figure 10-20. MSCAN Identifier Acceptance Registers (Second Bank) — CANIDAR4–CANIDAR7

Read: Anytime

Write: Anytime in initialization mode (INITRQ = 1 and INITAK = 1)

Table 10-20. CANIDAR4–CANIDAR7 Register Field Descriptions

Field	Description
7:0 AC[7:0]	Acceptance Code Bits — AC[7:0] comprise a user-defined sequence of bits with which the corresponding bits of the related identifier register (IDRn) of the receive message buffer are compared. The result of this comparison is then masked with the corresponding identifier mask register.

11.3 Memory Map and Register Definition

The CRG contains the registers and associated bits for controlling and monitoring the OSCV2 module.

11.4 Functional Description

The OSCV2 block has two external pins, EXTAL and XTAL. The oscillator input pin, EXTAL, is intended to be connected to either a crystal or an external clock source. The selection of Colpitts oscillator or Pierce oscillator/external clock depends on the XCLKS signal which is sampled during reset. The XTAL pin is an output signal that provides crystal circuit feedback.

A buffered EXTAL signal, OSCCLK, becomes the internal reference clock. To improve noise immunity, the oscillator is powered by the V_{DDPLL} and V_{SSPLL} power supply pins.

The Pierce oscillator can be used for higher frequencies compared to the low power Colpitts oscillator.

11.4.1 Amplitude Limitation Control (ALC)

The Colpitts oscillator is equipped with a feedback system which does not waste current by generating harmonics. Its configuration is “Colpitts oscillator with translated ground.” The transconductor used is driven by a current source under the control of a peak detector which will measure the amplitude of the AC signal appearing on EXTAL node in order to implement an amplitude limitation control (ALC) loop. The ALC loop is in charge of reducing the quiescent current in the transconductor as a result of an increase in the oscillation amplitude. The oscillation amplitude can be limited to two values. The normal amplitude which is intended for non power saving modes and a small amplitude which is intended for low power operation modes. Please refer to the CRG block description chapter for the control and assignment of the amplitude value to operation modes.

11.4.2 Clock Monitor (CM)

The clock monitor circuit is based on an internal resistor-capacitor (RC) time delay so that it can operate without any MCU clocks. If no OSCCLK edges are detected within this RC time delay, the clock monitor indicates a failure which asserts self clock mode or generates a system reset depending on the state of SCME bit. If the clock monitor is disabled or the presence of clocks is detected no failure is indicated. The clock monitor function is enabled/disabled by the CME control bit, described in the CRG block description chapter.

11.5 Interrupts

OSCV2 contains a clock monitor, which can trigger an interrupt or reset. The control bits and status bits for the clock monitor are described in the CRG block description chapter.

Chapter 12

Pulse-Width Modulator (PWM8B6CV1) Block Description

12.1 Introduction

The pulse width modulation (PWM) definition is based on the HC12 PWM definitions. The PWM8B6CV1 module contains the basic features from the HC11 with some of the enhancements incorporated on the HC12, that is center aligned output mode and four available clock sources. The PWM8B6CV1 module has six channels with independent control of left and center aligned outputs on each channel.

Each of the six PWM channels has a programmable period and duty cycle as well as a dedicated counter. A flexible clock select scheme allows a total of four different clock sources to be used with the counters. Each of the modulators can create independent continuous waveforms with software-selectable duty rates from 0% to 100%. The PWM outputs can be programmed as left aligned outputs or center aligned outputs

12.1.1 Features

- Six independent PWM channels with programmable period and duty cycle
- Dedicated counter for each PWM channel
- Programmable PWM enable/disable for each channel
- Software selection of PWM duty pulse polarity for each channel
- Period and duty cycle are double buffered. Change takes effect when the end of the effective period is reached (PWM counter reaches 0) or when the channel is disabled.
- Programmable center or left aligned outputs on individual channels
- Six 8-bit channel or three 16-bit channel PWM resolution
- Four clock sources (A, B, SA, and SB) provide for a wide range of frequencies.
- Programmable clock select logic
- Emergency shutdown

12.1.2 Modes of Operation

There is a software programmable option for low power consumption in wait mode that disables the input clock to the prescaler.

In freeze mode there is a software programmable option to disable the input clock to the prescaler. This is useful for emulation.

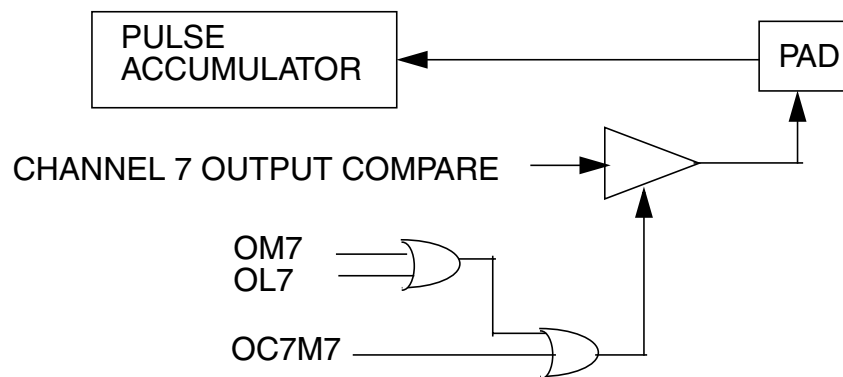


Figure 15-4. Channel 7 Output Compare/Pulse Accumulator Logic

NOTE

For more information see the respective functional descriptions in [Section 15.4, “Functional Description,”](#) of this document.

15.2 External Signal Description

The TIM16B8CV1 module has a total of eight external pins.

15.2.1 IOC7 — Input Capture and Output Compare Channel 7 Pin

This pin serves as input capture or output compare for channel 7. This can also be configured as pulse accumulator input.

15.2.2 IOC6 — Input Capture and Output Compare Channel 6 Pin

This pin serves as input capture or output compare for channel 6.

15.2.3 IOC5 — Input Capture and Output Compare Channel 5 Pin

This pin serves as input capture or output compare for channel 5.

15.2.4 IOC4 — Input Capture and Output Compare Channel 4 Pin

This pin serves as input capture or output compare for channel 4. Pin

15.2.5 IOC3 — Input Capture and Output Compare Channel 3 Pin

This pin serves as input capture or output compare for channel 3.

Table 15-5. OC7M Field Descriptions

Field	Description
7:0 OC7M[7:0]	Output Compare 7 Mask — Setting the OC7Mx (x ranges from 0 to 6) will set the corresponding port to be an output port when the corresponding TIOSx (x ranges from 0 to 6) bit is set to be an output compare. Note: A successful channel 7 output compare overrides any channel 6:0 compares. For each OC7M bit that is set, the output compare action reflects the corresponding OC7D bit.

15.3.2.4 Output Compare 7 Data Register (OC7D)

Module Base + 0x0003

	7	6	5	4	3	2	1	0
R	OC7D7	OC7D6	OC7D5	OC7D4	OC7D3	OC7D2	OC7D1	OC7D0
W								
Reset	0	0	0	0	0	0	0	0

Figure 15-9. Output Compare 7 Data Register (OC7D)

Read: Anytime

Write: Anytime

Table 15-6. OC7D Field Descriptions

Field	Description
7:0 OC7D[7:0]	Output Compare 7 Data — A channel 7 output compare can cause bits in the output compare 7 data register to transfer to the timer port data register depending on the output compare 7 mask register.

15.3.2.5 Timer Count Register (TCNT)

Module Base + 0x0004

	15	14	13	12	11	10	9	9
R	TCNT15	TCNT14	TCNT13	TCNT12	TCNT11	TCNT10	TCNT9	TCNT8
W								
Reset	0	0	0	0	0	0	0	0

Figure 15-10. Timer Count Register High (TCNTH)

Module Base + 0x0005

	7	6	5	4	3	2	1	0
R	TCNT7	TCNT6	TCNT5	TCNT4	TCNT3	TCNT2	TCNT1	TCNT0
W								
Reset	0	0	0	0	0	0	0	0

Figure 15-11. Timer Count Register Low (TCNTL)

17.4.4 Flash Reset Sequence

On each reset, the Flash module executes a reset sequence to hold CPU activity while loading the following registers from the Flash array memory according to [Table 17-1](#):

- FPROT — Flash Protection Register (see [Section 17.3.2.5](#))
- FSEC — Flash Security Register (see [Section 17.3.2.2](#))

17.4.4.1 Reset While Flash Command Active

If a reset occurs while any Flash command is in progress, that command will be immediately aborted. The state of the word being programmed or the sector/array being erased is not guaranteed.

17.4.5 Interrupts

The Flash module can generate an interrupt when all Flash commands have completed execution or the Flash address, data, and command buffers are empty.

Table 17-16. Flash Interrupt Sources

Interrupt Source	Interrupt Flag	Local Enable	Global (CCR) Mask
Flash Address, Data, and Command Buffers are empty	CBEIF (FSTAT register)	CBEIE	I Bit
All Flash commands have completed execution	CCIF (FSTAT register)	CCIE	I Bit

NOTE

Vector addresses and their relative interrupt priority are determined at the MCU level.

17.4.5.1 Description of Interrupt Operation

[Figure 17-26](#) shows the logic used for generating interrupts.

The Flash module uses the CBEIF and CCIF flags in combination with the enable bits CBIE and CCIE to discriminate for the generation of interrupts.

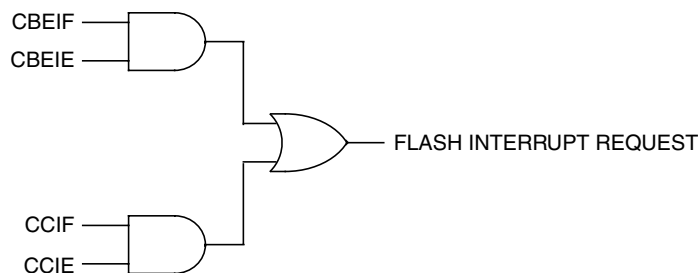


Figure 17-26. Flash Interrupt Implementation

For a detailed description of these register bits, refer to [Section 17.3.2.4](#), “Flash Configuration Register (FCNFG)” and [Section 17.3.2.6](#), “Flash Status Register (FSTAT)”.

FPHDIS is cleared. The FPROT register is loaded from Flash address 0xFF0D during the reset sequence, indicated by F in [Figure 18-8](#).

To change the Flash protection that will be loaded on reset, the upper sector of the Flash array must be unprotected, then the Flash protection byte located at Flash address 0xFF0D must be written to.

A protected Flash sector is disabled by FPHDIS and [FPLDIS](#) while the size of the protected sector is defined by FPHS[1:0] and [FPLS\[1:0\]](#) in the FPROT register.

Trying to alter any of the protected areas will result in a protect violation error and the PVIOL flag will be set in the FSTAT register (see [Section 18.3.2.6](#)). A mass erase of the whole Flash array is only possible when protection is fully disabled by setting the FPOPEN, [FPLDIS](#), and FPHDIS bits. An attempt to mass erase a Flash array while protection is enabled will set the PVIOL flag in the FSTAT register.

Table 18-8. FPROT Field Descriptions

Field	Description
7 FPOPEN	Protection Function for Program or Erase — It is possible using the FPOPEN bit to either select address ranges to be protected using FPHDIS, FPLDIS, FPHS[1:0] and FPLS[1:0] or to select the same ranges to be unprotected. When FPOPEN is set, FPxDIS enables the ranges to be protected, whereby clearing FPxDIS enables protection for the range specified by the corresponding FPxS[1:0] bits. When FPOPEN is cleared, FPxDIS defines unprotected ranges as specified by the corresponding FPxS[1:0] bits. In this case, setting FPxDIS enables protection. Thus the effective polarity of the FPxDIS bits is swapped by the FPOPEN bit as shown in Table 18-9 . This function allows the main part of the Flash array to be protected while a small range can remain unprotected for EEPROM emulation. 0 The FPHDIS and FPLDIS bits define Flash address ranges to be unprotected 1 The FPHDIS and FPLDIS bits define Flash address ranges to be protected
6 NV6	Nonvolatile Flag Bit — The NV6 bit should remain in the erased state for future enhancements.
5 FPHDIS	Flash Protection Higher Address Range Disable — The FPHDIS bit determines whether there is a protected/unprotected area in the higher space of the Flash address map. 0 Protection/unprotection enabled 1 Protection/unprotection disabled
4–3 FPHS[1:0]	Flash Protection Higher Address Size — The FPHS[1:0] bits determine the size of the protected/unprotected sector as shown in Table 18-10 . The FPHS[1:0] bits can only be written to while the FPHDIS bit is set.
2 FPLDIS	Flash Protection Lower Address Range Disable — The FPLDIS bit determines whether there is a protected/unprotected sector in the lower space of the Flash address map. 0 Protection/unprotection enabled 1 Protection/unprotection disabled
1–0 FPLS[1:0]	Flash Protection Lower Address Size — The FPLS[1:0] bits determine the size of the protected/unprotected sector as shown in Table 18-11 . The FPLS[1:0] bits can only be written to while the FPLDIS bit is set.

then FCLKDIV register bits PRDIV8 and FDIV[5:0] are to be set as described in [Figure 18-21](#).

For example, if the oscillator clock frequency is 950 kHz and the bus clock is 10 MHz, FCLKDIV bits FDIV[5:0] should be set to 4 (000100) and bit PRDIV8 set to 0. The resulting FCLK is then 190 kHz. As a result, the Flash algorithm timings are increased over optimum target by:

$$(200 - 190) / 200 \times 100 = 5\%$$

Command execution time will increase proportionally with the period of FCLK.

CAUTION

Because of the impact of clock synchronization on the accuracy of the functional timings, programming or erasing the Flash array cannot be performed if the bus clock runs at less than 1 MHz. Programming or erasing the Flash array with an input clock < 150 kHz should be avoided. Setting FCLKDIV to a value such that FCLK < 150 kHz can destroy the Flash array due to overstress. Setting FCLKDIV to a value such that $(1/\text{FCLK} + T_{\text{bus}}) < 5\mu\text{s}$ can result in incomplete programming or erasure of the Flash array cells.

If the FCLKDIV register is written, the bit FDIVLD is set automatically. If the FDIVLD bit is 0, the FCLKDIV register has not been written since the last reset. If the FCLKDIV register has not been written to, the Flash command loaded during a command write sequence will not execute and the ACCERR flag in the FSTAT register will set.

Table 19-13. Flash Protection Scenario Transitions

From Protection Scenario	To Protection Scenario ⁽¹⁾							
	0	1	2	3	4	5	6	7
6		X		X	X		X	
7	X	X	X	X	X	X	X	X

1. Allowed transitions marked with X.

19.3.2.6 Flash Status Register (FSTAT)

The FSTAT register defines the status of the Flash command controller and the results of command execution.

Module Base + 0x0005

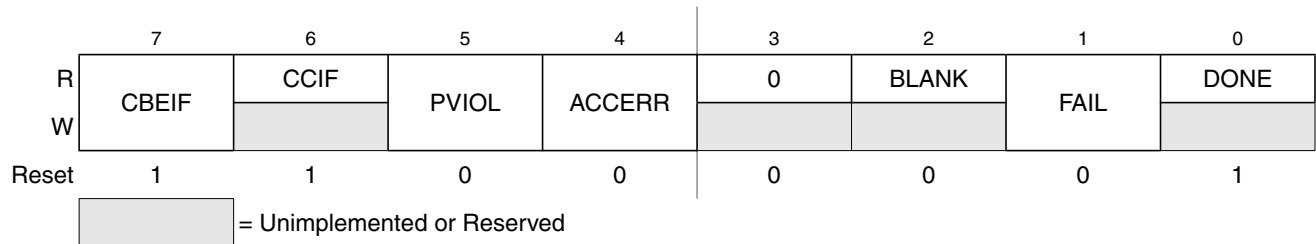


Figure 19-12. Flash Status Register (FSTAT)

In normal modes, bits CBEIF, PVIOL, and ACCERR are readable and writable, bits CCIF and BLANK are readable and not writable, remaining bits, including FAIL and DONE, read 0 and are not writable. In special modes, FAIL is readable and writable while DONE is readable but not writable. FAIL must be clear in special modes when starting a command write sequence.

Table 19-14. FSTAT Field Descriptions

Field	Description
7 CBEIF	Command Buffer Empty Interrupt Flag — The CBEIF flag indicates that the address, data and command buffers are empty so that a new command write sequence can be started. The CBEIF flag is cleared by writing a 1 to CBEIF. Writing a 0 to the CBEIF flag has no effect on CBEIF. Writing a 0 to CBEIF after writing an aligned word to the Flash address space but before CBEIF is cleared will abort a command write sequence and cause the ACCERR flag in the FSTAT register to be set. Writing a 0 to CBEIF outside of a command write sequence will not set the ACCERR flag. The CBEIF flag is used together with the CBEIE bit in the FCNFG register to generate an interrupt request (see Figure 19-29). 0 Buffers are full 1 Buffers are ready to accept a new command
6 CCIF	Command Complete Interrupt Flag — The CCIF flag indicates that there are no more commands pending. The CCIF flag is cleared when CBEIF is clear and sets automatically upon completion of all active and pending commands. The CCIF flag does not set when an active commands completes and a pending command is fetched from the command buffer. Writing to the CCIF flag has no effect. The CCIF flag is used together with the CCIE bit in the FCNFG register to generate an interrupt request (see Figure 19-29). 0 Command in progress 1 All commands are completed

19.4.1.3.2 Program Command

The program operation will program a previously erased word in the Flash array using an embedded algorithm.

An example flow to execute the program operation is shown in [Figure 19-26](#). The program command write sequence is as follows:

1. Write to a Flash array address to start the command write sequence for the program command. The data written will be programmed to the Flash array address written.
2. Write the program command, 0x20, to the FCMD register.
3. Clear the CBEIF flag in the FSTAT register by writing a 1 to CBEIF to launch the program command.

If a word to be programmed is in a protected area of the Flash array, the PVIOL flag in the FSTAT register will set and the program command will not launch. Once the program command has successfully launched, the CCIF flag in the FSTAT register will set after the program operation has completed unless a new command write sequence has been buffered. By executing a new program command write sequence on sequential words after the CBEIF flag in the FSTAT register has been set, up to 55% faster programming time per word can be effectively achieved than by waiting for the CCIF flag to set after each program operation.

21.4.2 Operating Modes

21.4.2.1 Wait Mode

If the MCU enters wait mode while a Flash command is active ($CCIF = 0$), that command and any buffered command will be completed.

The Flash module can recover the MCU from wait mode if the interrupts are enabled (see [Section 21.4.5](#)).

21.4.2.2 Stop Mode

If the MCU enters stop mode while a Flash command is active ($CCIF = 0$), that command will be aborted and the data being programmed or erased is lost. The high voltage circuitry to the Flash array will be switched off when entering stop mode. $CCIF$ and $ACCERR$ flags will be set. Upon exit from stop mode, the $CBEIF$ flag will be set and any buffered command will not be executed. The $ACCERR$ flag must be cleared before returning to normal operation.

NOTE

As active Flash commands are immediately aborted when the MCU enters stop mode, it is strongly recommended that the user does not use the STOP instruction during program and erase execution.

21.4.2.3 Background Debug Mode

In background debug mode (BDM), the $FPROT$ register is writable. If the MCU is unsecured, then all Flash commands listed in [Table 21-16](#) can be executed. If the MCU is secured and is in special single chip mode, the only possible command to execute is mass erase.

21.4.3 Flash Module Security

The Flash module provides the necessary security information to the MCU. After each reset, the Flash module determines the security state of the MCU as defined in [Section 21.3.2.2, “Flash Security Register \(FSEC\)”](#).

The contents of the Flash security/options byte at address $0xFF0F$ in the Flash configuration field must be changed directly by programming address $0xFF0F$ when the device is unsecured and the higher address sector is unprotected. If the Flash security/options byte is left in the secure state, any reset will cause the MCU to return to the secure operating mode.

21.4.3.1 Unsecuring the MCU using Backdoor Key Access

The MCU may only be unsecured by using the backdoor key access feature which requires knowledge of the contents of the backdoor key (four 16-bit words programmed at addresses $0xFF00$ – $0xFF07$). If $KEYEN[1:0] = 1:0$ and the $KEYACC$ bit is set, a write to a backdoor key address in the Flash array triggers a comparison between the written data and the backdoor key data stored in the Flash array. If all four words of data are written to the correct addresses in the correct order and the data matches the backdoor key stored in the Flash array, the MCU will be unsecured. The data must be written to the backdoor key

A.1.7 Operating Conditions

This chapter describes the operating conditions of the devices. Unless otherwise noted those conditions apply to all the following data.

NOTE

Instead of specifying ambient temperature all parameters are specified for the more meaningful silicon junction temperature. For power dissipation calculations refer to [Section A.1.8, “Power Dissipation and Thermal Characteristics”](#)

Table A-4. Operating Conditions

Rating	Symbol	Min	Typ	Max	Unit
I/O, Regulator and Analog Supply Voltage	V_{DD5}	2.97	5	5.5	V
Digital Logic Supply Voltage ⁽¹⁾	V_{DD}	2.35	2.5	2.75	V
PLL Supply Voltage ¹	V_{DDPLL}	2.35	2.5	2.75	V
Voltage Difference V_{DDX} to V_{DDA}	ΔV_{DDX}	−0.1	0	0.1	V
Voltage Difference V_{SSX} to V_{SSR} and V_{SSA}	ΔV_{SSX}	−0.1	0	0.1	V
Bus Frequency	$f_{bus}^{(2)}$	0.25	—	25	MHz
Bus Frequency	$f_{bus}^{(3)}$	0.25	—	16	MHz
Operating Junction Temperature Range	T_J	−40	—	140	°C

1. The device contains an internal voltage regulator to generate the logic and PLL supply out of the I/O supply. The operating conditions apply when this regulator is disabled and the device is powered from an external source.

Using an external regulator, with the internal voltage regulator disabled, an external LVR must be provided.

2. Some blocks e.g. ATD (conversion) and NVMs (program/erase) require higher bus frequencies for proper operation.

3. Some blocks e.g. ATD (conversion) and NVMs (program/erase) require higher bus frequencies for proper operation.

A.1.8 Power Dissipation and Thermal Characteristics

Power dissipation and thermal characteristics are closely related. The user must assure that the maximum operating junction temperature is not exceeded. The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \cdot \Theta_{JA})$$

T_J = Junction Temperature, [°C]

T_A = Ambient Temperature, [°C]

P_D = Total Chip Power Dissipation, [W]

Θ_{JA} = Package Thermal Resistance, [°C/W]

The total power dissipation can be calculated from:

$$P_D = P_{INT} + P_{IO}$$

P_{INT} = Chip Internal Power Dissipation, [W]

Two cases with internal voltage regulator enabled and disabled must be considered:

1. Internal Voltage Regulator disabled

$$P_{INT} = I_{DD} \cdot V_{DD} + I_{DDPLL} \cdot V_{DDPLL} + I_{DDA} \cdot V_{DDA}$$

$$P_{IO} = \sum_i R_{DS(on)} \cdot I_{IO_i}^2$$

Which is the sum of all output currents on I/O ports associated with V_{DDX} and V_{DDM} .

For $R_{DS(on)}$ is valid:

$$R_{DS(on)} = \frac{V_{OL}}{I_{OL}}; \text{for outputs driven low}$$

respectively

$$R_{DS(on)} = \frac{V_{DD5} - V_{OH}}{I_{OH}}; \text{for outputs driven high}$$

2. Internal voltage regulator enabled

$$P_{INT} = I_{DDR} \cdot V_{DDR} + I_{DDA} \cdot V_{DDA}$$

I_{DDR} is the current shown in [Table A-8](#) and not the overall current flowing into V_{DDR} , which additionally contains the current flowing into the external loads with output high.

$$P_{IO} = \sum_i R_{DS(on)} \cdot I_{IO_i}^2$$

Which is the sum of all output currents on I/O ports associated with V_{DDX} and V_{DDR} .