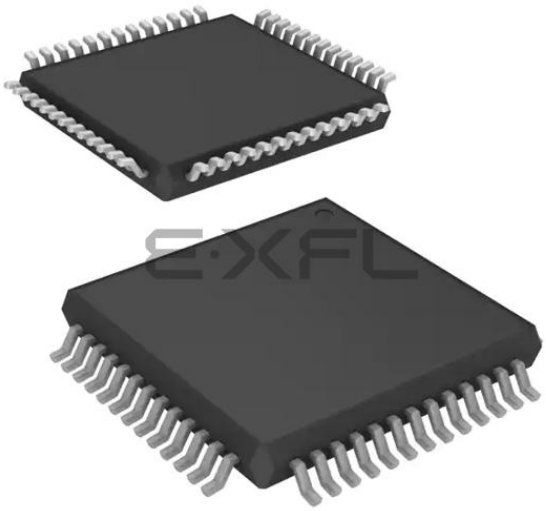

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Number of I/O	35
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Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
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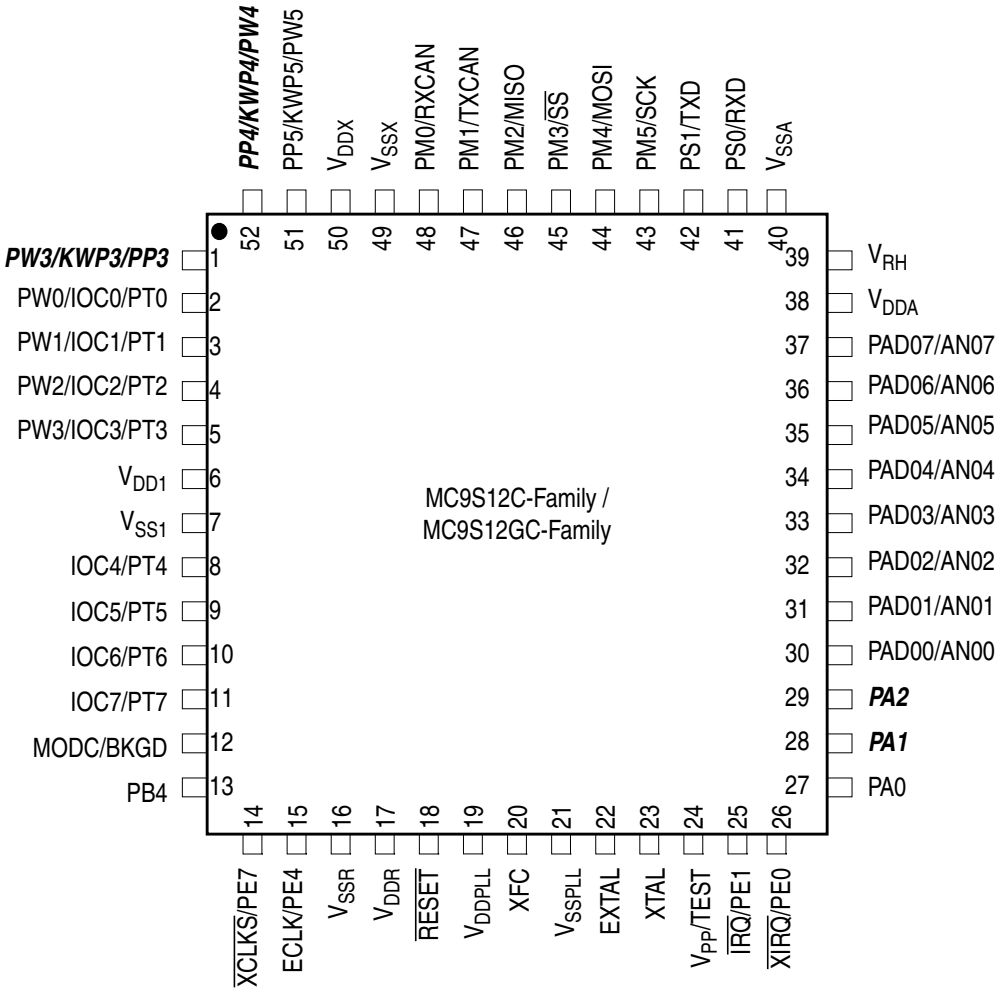
Table 1-2. Detailed MSCAN Foreground Receive and Transmit Buffer Layout (continued)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0xXXX2	Extended ID	Read:	ID14	ID13	ID12	ID11	ID10	ID9	ID8	ID7
	Standard ID	Read:								
	CANxRIDR2	Write:								
0xXXX3	Extended ID	Read:	ID6	ID5	ID4	ID3	ID2	ID1	ID0	RTR
	Standard ID	Read:								
	CANxRIDR3	Write:								
0xXXX4–0xXXXB	CANxRDSR0–CANxRDSR7	Read:	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
		Write:								
0xXXXC	CANRxDLR	Read:					DLC3	DLC2	DLC1	DLC0
		Write:								
0xXXXD	Reserved	Read:								
		Write:								
0xXXXE	CANxRTSRH	Read:	TSR15	TSR14	TSR13	TSR12	TSR11	TSR10	TSR9	TSR8
		Write:								
0xXXXF	CANxRTSRL	Read:	TSR7	TSR6	TSR5	TSR4	TSR3	TSR2	TSR1	TSR0
		Write:								
0xxx10	Extended ID CANxTIDR0	Read:	ID28	ID27	ID26	ID25	ID24	ID23	ID22	ID21
		Write:								
	Standard ID	Read:	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3
		Write:								
0xxx11	Extended ID CANxTIDR1	Read:	ID20	ID19	ID18	SRR=1	IDE=1	ID17	ID16	ID15
		Write:								
	Standard ID	Read:	ID2	ID1	ID0	RTR	IDE=0			
		Write:								
0xxx12	Extended ID CANxTIDR2	Read:	ID14	ID13	ID12	ID11	ID10	ID9	ID8	ID7
		Write:								
	Standard ID	Read:								
		Write:								
0xxx13	Extended ID CANxTIDR3	Read:	ID6	ID5	ID4	ID3	ID2	ID1	ID0	RTR
		Write:								
	Standard ID	Read:								
		Write:								
0xxx14–0xxx1B	CANxTDSR0–CANxTDSR7	Read:	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
		Write:								
0xxx1C	CANxTDLR	Read:					DLC3	DLC2	DLC1	DLC0
		Write:								
0xxx1D	CONxTTBPR	Read:	PRIO7	PRIO6	PRIO5	PRIO4	PRIO3	PRIO2	PRIO1	PRIO0
		Write:								
0xxx1E	CANxTTSRH	Read:	TSR15	TSR14	TSR13	TSR12	TSR11	TSR10	TSR9	TSR8
		Write:								
0xxx1F	CANxTTSRL	Read:	TSR7	TSR6	TSR5	TSR4	TSR3	TSR2	TSR1	TSR0
		Write:								



* Signals shown in ***Bold italic*** are not available on the 48-pin package

Figure 1-8. Pin Assignments in 52-Pin LQFP

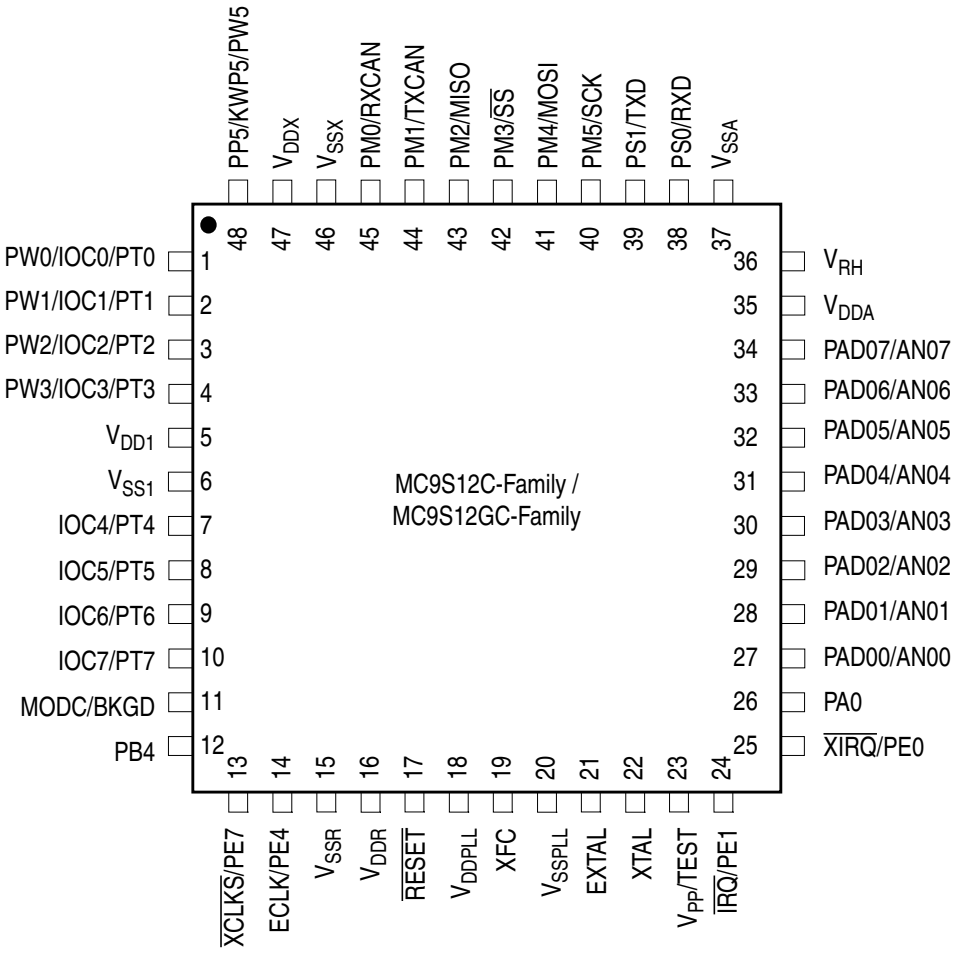


Figure 1-9. Pin Assignments in 48-Pin LQFP

2.3.2 Register Descriptions

Table 2-2 summarizes the effect on the various configuration bits — data direction (DDR), input/output level (I/O), reduced drive (RDR), pull enable (PE), pull select (PS), and interrupt enable (IE) for the ports. The configuration bit PS is used for two purposes:

1. Configure the sensitive interrupt edge (rising or falling), if interrupt is enabled.
2. Select either a pull-up or pull-down device if PE is active.

Table 2-2. Pin Configuration Summary

DDR	IO	RDR	PE	PS	IE[1]	Function	Pull Device	Interrupt
0	X	X	0	X	0	Input	Disabled	Disabled
0	X	X	1	0	0	Input	Pull up	Disabled
0	X	X	1	1	0	Input	Pull down	Disabled
0	X	X	0	0	1	Input	Disabled	Falling edge
0	X	X	0	1	1	Input	Disabled	Rising edge
0	X	X	1	0	1	Input	Pull up	Falling edge
0	X	X	1	1	1	Input	Pull down	rising edge
1	0	0	X	X	0	Output, full drive to 0	Disabled	Disabled
1	1	0	X	X	0	Output, full drive to 1	Disabled	Disabled
1	0	1	X	X	0	Output, reduced drive to 0	Disabled	Disabled
1	1	1	X	X	0	Output, reduced drive to 1	Disabled	Disabled
1	0	0	X	0	1	Output, full drive to 0	Disabled	Falling edge
1	1	0	X	1	1	Output, full drive to 1	Disabled	Rising edge
1	0	1	X	0	1	Output, reduced drive to 0	Disabled	Falling edge
1	1	1	X	1	1	Output, reduced drive to 1	Disabled	Rising edge

1. Applicable only on ports P and J.

NOTE

All bits of all registers in this module are completely synchronous to internal clocks during a register read.

3.3.2.4 Miscellaneous System Control Register (MISC)

Module Base + 0x0013
Starting address location affected by INITRG register setting.

	7	6	5	4	3	2	1	0
R	0	0	0	0	EXSTR1	EXSTR0	ROMHM	ROMON
W								
Reset: Expanded or Emulation	0	0	0	0	1	1	0	—[1]
Reset: Peripheral or Single Chip	0	0	0	0	1	1	0	1
Reset: Special Test	0	0	0	0	1	1	0	0

1. The reset state of this bit is determined at the chip integration level.

= Unimplemented or Reserved

Figure 3-6. Miscellaneous System Control Register (MISC)

Read: Anytime

Write: As stated in each bit description

NOTE

Writes to this register take one cycle to go into effect.

This register initializes miscellaneous control functions.

Table 3-5. INITEE Field Descriptions

Field	Description
3:2 EXSTR[1:0]	**External Access Stretch Bits 1 and 0** Write: once in normal and emulation modes and anytime in special modes This two-bit field determines the amount of clock stretch on accesses to the external address space as shown in Table 3-6. In single chip and peripheral modes these bits have no meaning or effect.
1 ROMHM	**FLASH EEPROM or ROM Only in Second Half of Memory Map** Write: once in normal and emulation modes and anytime in special modes 0 The fixed page(s) of FLASH EEPROM or ROM in the lower half of the memory map can be accessed. 1 Disables direct access to the FLASH EEPROM or ROM in the lower half of the memory map. These physical locations of the FLASH EEPROM or ROM remain accessible through the program page window.
0 ROMON	**ROMON — Enable FLASH EEPROM or ROM** Write: once in normal and emulation modes and anytime in special modes This bit is used to enable the FLASH EEPROM or ROM memory in the memory map. 0 Disables the FLASH EEPROM or ROM from the memory map. 1 Enables the FLASH EEPROM or ROM in the memory map.

4.3.2.5 Reserved Registers

Module Base + 0x0004
Starting address location affected by INITRG register setting.

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 4-6. Reserved Register

Module Base + 0x0005
Starting address location affected by INITRG register setting.

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 4-7. Reserved Register

Module Base + 0x0006
Starting address location affected by INITRG register setting.

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 4-8. Reserved Register

Module Base + 0x0007
Starting address location affected by INITRG register setting.

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 4-9. Reserved Register

NOTE

To ensure that you read the value present on the PORTE pins, always wait at least one cycle after writing to the DDRE register before reading from the PORTE register.

4.3.2.7 Data Direction Register E (DDRE)

Module Base + 0x0009
Starting address location affected by INITRG register setting.

	7	6	5	4	3	2	1	0
R	Bit 7	6	5	4	3	Bit 2	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 4-11. Data Direction Register E (DDRE)

Read: Anytime when register is in the map

Write: Anytime when register is in the map

Data direction register E is associated with port E. For bits in port E that are configured as general-purpose I/O lines, DDRE determines the primary direction of each of these pins. A 1 causes the associated bit to be an output and a 0 causes the associated bit to be an input. Port E bit 1 (associated with $\overline{\text{IRQ}}$) and bit 0 (associated with $\overline{\text{XIRQ}}$) cannot be configured as outputs. Port E, bits 1 and 0, can be read regardless of whether the alternate interrupt function is enabled. The value in a DDR bit also affects the source of data for reads of the corresponding PORTE register. If the DDR bit is 0 (input) the buffered pin input state is read. If the DDR bit is 1 (output) the associated port data register bit state is read.

This register is not in the on-chip memory map in expanded and special peripheral modes. Therefore, these accesses will be echoed externally. Also, it is not in the map in expanded modes while the EME control bit is set.

Table 4-5. DDRE Field Descriptions

Field	Description
7:2 DDRE	**Data Direction Port E** 0 Configure the corresponding I/O pin as an input 1 Configure the corresponding I/O pin as an output **Note:** It is unwise to write PORTE and DDRE as a word access. If you are changing port E pins from inputs to outputs, the data may have extra transitions during the write. It is best to initialize PORTE before enabling as outputs.

Table 7-12. DBGCC Field Descriptions

Field	Description
15:0	**Comparator C Compare Bits** — The comparator C compare bits control whether comparator C will compare the address bus bits [15:0] to a logic 1 or logic 0. See Table 7-13. 0 Compare corresponding address bit to a logic 0 1 Compare corresponding address bit to a logic 1 **Note:** This register will be cleared automatically when the DBG module is armed in LOOP1 mode.

Table 7-13. Comparator C Compares

PAGSEL	EXTCMP Compare	High-Byte Compare
x0	No compare	DBGCCH[7:0] = AB[15:8]
x1	EXTCMP[5:0] = XAB[21:16]	DBGCCH[7:0] = XAB[15:14],AB[13:8]

7.3.2.7 Debug Control Register 2 (DBGC2)

Module Base + 0x0028
Starting address location affected by INITRG register setting.

	7	6	5	4	3	2	1	0
R W	BKABEN(1)	FULL	BDM	TAGAB	BKCEN(2)	TAGC2	RWCEN2	RWC2
Reset	0	0	0	0	0	0	0	0

1. When BKABEN is set (BKP mode), all bits in DBGC2 are available. When BKABEN is cleared and DBG is used in DBG mode, bits FULL and TAGAB have no meaning.
2. These bits can be used in BKP mode and DBG mode (when capture mode is not set in LOOP1) to provide a third breakpoint.

Figure 7-13. Debug Control Register 2 (DBGC2)

Table 7-14. DBGC2 Field Descriptions

Field	Description
7 BKABEN	**Breakpoint Using Comparator A and B Enable** — This bit enables the breakpoint capability using comparator A and B, when set (BKP mode) the DBGEN bit in DBGC1 cannot be set. 0 Breakpoint module off 1 Breakpoint module on
6 FULL	**Full Breakpoint Mode Enable** — This bit controls whether the breakpoint module is in dual mode or full mode. In full mode, comparator A is used to match address and comparator B is used to match data. See Section 7.4.1.2, “Full Breakpoint Mode,” for more details. 0 Dual address mode enabled 1 Full breakpoint mode enabled
5 BDM	**Background Debug Mode Enable** — This bit determines if the breakpoint causes the system to enter background debug mode (BDM) or initiate a software interrupt (SWI). 0 Go to software interrupt on a break request 1 Go to BDM on a break request

Table 9-11. Outcome of Clock Loss in Wait Mode (continued)

CME	SCME	SCMIE	CRG Actions
1	1	1	Clock failure --> – VREG enabled, – PLL enabled, – SCM activated, – Start Clock Quality Check, – SCMIF set. SCMIF generates Self-Clock Mode wakeup interrupt. – Exit Wait Mode in SCM using PLL clock (f_{SCM}) as system clock, – Continue to perform a additional Clock Quality Checks until OSCCLK is o.k. again.

9.4.10 Low-Power Operation in Stop Mode

All clocks are stopped in STOP mode, dependent of the setting of the PCE, PRE and PSTP bit. The oscillator is disabled in STOP mode unless the PSTP bit is set. All counters and dividers remain frozen but do not initialize. If the PRE or PCE bits are set, the RTI or COP continues to run in pseudo-stop mode. In addition to disabling system and core clocks the CRG requests other functional units of the MCU (e.g. voltage-regulator) to enter their individual power-saving modes (if available). This is the main difference between pseudo-stop mode and wait mode.

After executing the STOP instruction the core requests the CRG to switch the MCU into stop mode. If the PLLSEL bit remains set when entering stop mode, the CRG will switch the system and core clocks to OSCCLK by clearing the PLLSEL bit. Then the CRG disables the PLL, disables the core clock and finally disables the remaining system clocks. As soon as all clocks are switched off, stop mode is active.

If pseudo-stop mode (PSTP = 1) is entered from self-clock mode the CRG will continue to check the clock quality until clock check is successful. The PLL and the voltage regulator (VREG) will remain enabled. If full stop mode (PSTP = 0) is entered from self-clock mode an ongoing clock quality check will be stopped. A complete timeout window check will be started when stop mode is exited again.

Wake-up from stop mode also depends on the setting of the PSTP bit.

Table 10-1. CANCTL0 Register Field Descriptions (continued)

Field	Description
1 SLPRQ[5]	**Sleep Mode Request** — This bit requests the MSCAN to enter sleep mode, which is an internal power saving mode (see Section 10.4.5.4, "MSCAN Sleep Mode"). The sleep mode request is serviced when the CAN bus is idle, i.e., the module is not receiving a message and all transmit buffers are empty. The module indicates entry to sleep mode by setting SLPAK = 1 (see Section 10.3.2.2, "MSCAN Control Register 1 (CANCTL1)"). SLPRQ cannot be set while the WUPIF flag is set (see Section 10.3.2.5, "MSCAN Receiver Flag Register (CANRFLG)"). Sleep mode will be active until SLPRQ is cleared by the CPU or, depending on the setting of WUPE, the MSCAN detects activity on the CAN bus and clears SLPRQ itself. 0 Running — The MSCAN functions normally 1 Sleep mode request — The MSCAN enters sleep mode when CAN bus idle
0 INITRQ[6],[7]	**Initialization Mode Request** — When this bit is set by the CPU, the MSCAN skips to initialization mode (see Section 10.4.5.5, "MSCAN Initialization Mode"). Any ongoing transmission or reception is aborted and synchronization to the CAN bus is lost. The module indicates entry to initialization mode by setting INITAK = 1 (Section 10.3.2.2, "MSCAN Control Register 1 (CANCTL1)"). The following registers enter their hard reset state and restore their default values: CANCTL0[8], CANRFLG[9], CANRIER[10], CANTFLG, CANTIER, CANTARQ, CANTAAK, and CANTBSEL. The registers CANCTL1, CANBTR0, CANBTR1, CANIDAC, CANIDAR0-7, and CANIDMR0-7 can only be written by the CPU when the MSCAN is in initialization mode (INITRQ = 1 and INITAK = 1). The values of the error counters are not affected by initialization mode. When this bit is cleared by the CPU, the MSCAN restarts and then tries to synchronize to the CAN bus. If the MSCAN is not in bus-off state, it synchronizes after 11 consecutive recessive bits on the CAN bus; if the MSCAN is in bus-off state, it continues to wait for 128 occurrences of 11 consecutive recessive bits. Writing to other bits in CANCTL0, CANRFLG, CANRIER, CANTFLG, or CANTIER must be done only after initialization mode is exited, which is INITRQ = 0 and INITAK = 0. 0 Normal operation 1 MSCAN in initialization mode

1. The MSCAN must be in normal mode for this bit to become set.
2. See the Bosch CAN 2.0A/B specification for a detailed definition of transmitter and receiver states.
3. In order to protect from accidentally violating the CAN protocol, the TXCAN pin is immediately forced to a recessive state when the CPU enters wait (CSWAI = 1) or stop mode (see Section 10.4.5.2, "Operation in Wait Mode" and Section 10.4.5.3, "Operation in Stop Mode").
4. The CPU has to make sure that the WUPE register and the WUPIE wake-up interrupt enable register (see Section 10.3.2.6, "MSCAN Receiver Interrupt Enable Register (CANRIER)) is enabled, if the recovery mechanism from stop or wait is required.
5. The CPU cannot clear SLPRQ before the MSCAN has entered sleep mode (SLPRQ = 1 and SLPAK = 1).
6. The CPU cannot clear INITRQ before the MSCAN has entered initialization mode (INITRQ = 1 and INITAK = 1).
7. In order to protect from accidentally violating the CAN protocol, the TXCAN pin is immediately forced to a recessive state when the initialization mode is requested by the CPU. Thus, the recommended procedure is to bring the MSCAN into sleep mode (SLPRQ = 1 and SLPAK = 1) before requesting initialization mode.
8. Not including WUPE, INITRQ, and SLPRQ.
9. TSTAT1 and TSTAT0 are not affected by initialization mode.
10. RSTAT1 and RSTAT0 are not affected by initialization mode.

10.3.2.2 MSCAN Control Register 1 (CANCTL1)

The CANCTL1 register provides various control bits and handshake status information of the MSCAN module as described below.

Table 12-12 is used to summarize which channels are used to set the various control bits when in 16-bit mode.

Table 12-12. 16-bit Concatenation Mode Summary

CONxx	PWMEx	PPOLx	PCLKx	CAEx	PWMx Output
CON45	PWME5	PPOL5	PCLK5	CAE5	PWM5
CON23	PWME3	PPOL3	PCLK3	CAE3	PWM3
CON01	PWME1	PPOL1	PCLK1	CAE1	PWM1

12.4.2.8 PWM Boundary Cases

Table 12-13 summarizes the boundary conditions for the PWM regardless of the output mode (left aligned or center aligned) and 8-bit (normal) or 16-bit (concatenation):

Table 12-13. PWM Boundary Cases

PWMDTYx	PWMPERx	PPOLx	PWMx Output
0x0000 (indicates no duty)	>0x0000	1	Always Low
0x0000 (indicates no duty)	>0x0000	0	Always High
XX	0x0000(1) (indicates no period)	1	Always High
XX	0x0000[1] (indicates no period)	0	Always Low
>= PWMPERx	XX	1	Always High
>= PWMPERx	XX	0	Always Low

1. Counter = 0x0000 and does not count.

12.5 Resets

The reset state of each individual bit is listed within the register description section (see Section 12.3, “Memory Map and Register Definition,” which details the registers and their bit-fields. All special functions or modes which are initialized during or just following reset are described within this section.

- The 8-bit up/down counter is configured as an up counter out of reset.
- All the channels are disabled and all the counters don’t count.

12.6 Interrupts

The PWM8B6CV1 module has only one interrupt which is generated at the time of emergency shutdown, if the corresponding enable bit (PWMIE) is set. This bit is the enable for the interrupt. The interrupt flag PWMIF is set whenever the input level of the PWM5 channel changes while PWM5ENA=1 or when PWMENA is being asserted while the level at PWM5 is active.

A description of the registers involved and affected due to this interrupt is explained in Section 12.3.2.15, “PWM Shutdown Register (PWMSDN).”

13.3.2.1 SCI Baud Rate Registers (SCIBDH and SCHBDL)

Module Base + 0x_0000

	7	6	5	4	3	2	1	0
R	0	0	0	SBR12	SBR11	SBR10	SBR9	SBR8
W								
Reset	0	0	0	0	0	0	0	0

Module Base + 0x_0001

	7	6	5	4	3	2	1	0
R	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0
W								
Reset	0	0	0	0	0	1	0	0

= Unimplemented or Reserved

Figure 13-3. SCI Baud Rate Registers (SCIBDH and SCIBDL)

The SCI Baud Rate Register is used by the counter to determine the baud rate of the SCI. The formula for calculating the baud rate is:

SCI baud rate = SCI module clock / (16 x BR)

where:

BR is the content of the SCI baud rate registers, bits SBR12 through SBR0. The baud rate registers can contain a value from 1 to 8191.

Read: Anytime. If only SCIBDH is written to, a read will not return the correct data until SCIBDL is written to as well, following a write to SCIBDH.

Write: Anytime

Table 13-1. SCIBDH AND SCIBDL Field Descriptions

Field	Description
4–0 7–0 SBR[12:0]	**SCI Baud Rate Bits** — The baud rate for the SCI is determined by these 13 bits. **Note:** The baud rate generator is disabled until the TE bit or the RE bit is set for the first time after reset. The baud rate generator is disabled when BR = 0. Writing to SCIBDH has no effect without writing to SCIBDL, since writing to SCIBDH puts the data in a temporary location until SCIBDL is written to.

15.6.2 Pulse Accumulator Input Interrupt (PAOVI)

This active high output will be asserted by the module to request a timer pulse accumulator input interrupt to be serviced by the system controller.

15.6.3 Pulse Accumulator Overflow Interrupt (PAOVF)

This active high output will be asserted by the module to request a timer pulse accumulator overflow interrupt to be serviced by the system controller.

15.6.4 Timer Overflow Interrupt (TOF)

This active high output will be asserted by the module to request a timer overflow interrupt to be serviced by the system controller.

16.2 External Signal Description

Due to the nature of VREG3V3V2 being a voltage regulator providing the chip internal power supply voltages most signals are power supply signals connected to pads.

Table 16-1 shows all signals of VREG3V3V2 associated with pins.

Table 16-1. VREG3V3V2 — Signal Properties

Name	Port	Function	Reset State	Pull Up
V_{DDR}	—	VREG3V3V2 power input (positive supply)	—	—
V_{DDA}	—	VREG3V3V2 quiet input (positive supply)	—	—
V_{SSA}	—	VREG3V3V2 quiet input (ground)	—	—
V_{DD}	—	VREG3V3V2 primary output (positive supply)	—	—
V_{SS}	—	VREG3V3V2 primary output (ground)	—	—
V_{DDPLL}	—	VREG3V3V2 secondary output (positive supply)	—	—
V_{SSPLL}	—	VREG3V3V2 secondary output (ground)	—	—
V_{REGEN} (optional)	—	VREG3V3V2 (Optional) Regulator Enable	—	—

NOTE

Check device overview chapter for connectivity of the signals.

16.2.1 V_{DDR} — Regulator Power Input

Signal V_{DDR} is the power input of VREG3V3V2. All currents sourced into the regulator loads flow through this pin. A chip external decoupling capacitor (100 nF...220 nF, X7R ceramic) between V_{DDR} and V_{SSR} can smoothen ripple on V_{DDR}.

For entering Shutdown Mode, pin V_{DDR} should also be tied to ground on devices without a V_{REGEN} pin.

16.2.2 V_{DDA}, V_{SSA} — Regulator Reference Supply

Signals V_{DDA}/V_{SSA} which are supposed to be relatively quiet are used to supply the analog parts of the regulator. Internal precision reference circuits are supplied from these signals. A chip external decoupling capacitor (100 nF...220 nF, X7R ceramic) between V_{DDA} and V_{SSA} can further improve the quality of this supply.

16.4.1 REG — Regulator Core

VREG3V3V2, respectively its regulator core has two parallel, independent regulation loops (REG1 and REG2) that differ only in the amount of current that can be sourced to the connected loads. Therefore, only REG1 providing the supply at V_{DD}/V_{SS} is explained. The principle is also valid for REG2.

The regulator is a linear series regulator with a bandgap reference in its Full Performance Mode and a voltage clamp in Reduced Power Mode. All load currents flow from input V_{DDR} to V_{SS} or V_{SSPLL}, the reference circuits are connected to V_{DDA} and V_{SSA}.

16.4.2 Full-Performance Mode

In Full Performance Mode, a fraction of the output voltage (V_{DD}) and the bandgap reference voltage are fed to an operational amplifier. The amplified input voltage difference controls the gate of an output driver which basically is a large NMOS transistor connected to the output.

16.4.3 Reduced-Power Mode

In Reduced Power Mode, the driver gate is connected to a buffered fraction of the input voltage (V_{DDR}). The operational amplifier and the bandgap are disabled to reduce power consumption.

16.4.4 LVD — Low-Voltage Detect

sub-block LVD is responsible for generating the low-voltage interrupt (LVI). LVD monitors the input voltage (V_{DDA}–V_{SSA}) and continuously updates the status flag LVDS. Interrupt flag LVIF is set whenever status flag LVDS changes its value. The LVD is available in FPM and is inactive in Reduced Power Mode and Shutdown Mode.

16.4.5 POR — Power-On Reset

This functional block monitors output V_{DD}. If V_{DD} is below V_{PORD}, signal POR is high, if it exceeds V_{PORD}, the signal goes low. The transition to low forces the CPU in the power-on sequence.

Due to its role during chip power-up this module must be active in all operating modes of VREG3V3V2.

16.4.6 LVR — Low-Voltage Reset

Block LVR monitors the primary output voltage V_{DD}. If it drops below the assertion level (V_{LVRA}) signal LVR asserts and when rising above the deassertion level (V_{LVRD}) signal LVR negates again. The LVR function is available only in Full Performance Mode.

16.4.7 CTRL — Regulator Control

This part contains the register block of VREG3V3V2 and further digital functionality needed to control the operating modes. CTRL also represents the interface to the digital core logic.

Module Base + 0x000F

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 17-20. RESERVED6

All bits read 0 and are not writable.

17.4 Functional Description

17.4.1 Flash Command Operations

Write operations are used for the program, erase, and erase verify algorithms described in this section. The program and erase algorithms are controlled by a state machine whose timebase FCLK is derived from the oscillator clock via a programmable divider. The FCMD register as well as the associated FADDR and FDATA registers operate as a buffer and a register (2-stage FIFO) so that a new command along with the necessary data and address can be stored to the buffer while the previous command is still in progress. This pipelined operation allows a time optimization when programming more than one word on a specific row, as the high voltage generation can be kept active in between two programming commands. The pipelined operation also allows a simplification of command launching. Buffer empty as well as command completion are signalled by flags in the FSTAT register with corresponding interrupts generated, if enabled.

The next sections describe:

- How to write the FCLKDIV register
- Command write sequence used to program, erase or erase verify the Flash array
- Valid Flash commands
- Errors resulting from illegal Flash operations

17.4.1.1 Writing the FCLKDIV Register

Prior to issuing any Flash command after a reset, it is first necessary to write the FCLKDIV register to divide the oscillator clock down to within the 150-kHz to 200-kHz range. Since the program and erase timings are also a function of the bus clock, the FCLKDIV determination must take this information into account.

If we define:

- FCLK as the clock of the Flash timing control block
- Tbus as the period of the bus clock
- INT(x) as taking the integer part of x (e.g., INT(4.323) = 4),

Table 18-2. Flash Array Memory Map Summary

MCU Address Range	PPAGE	Protectable Low Range	Protectable High Range	Array Relative Address[1]
0x4000–0x7FFF	Unpaged (0x3E)	0x4000–0x43FF 0x4000–0x47FF 0x4000–0x4FFF 0x4000–0x5FFF	N.A.	0x18000–0x1BFFF
0x8000–0xBFFF	0x3E	0x8000–0x83FF 0x8000–0x87FF 0x8000–0x8FFF 0x8000–0x9FFF	N.A.	0x18000–0x1BFFF
	0x3F	N.A.	0xB800–0xBFFF 0xB000–0xBFFF 0xA000–0xBFFF 0x8000–0xBFFF	0x1C000–0x1FFFF
0xC000–0xFFFF	Unpaged (0x3F)	N.A.	0xF800–0xFFFF 0xF000–0xFFFF 0xE000–0xFFFF 0xC000–0xFFFF	0x1C000–0x1FFFF

1. Inside Flash block.

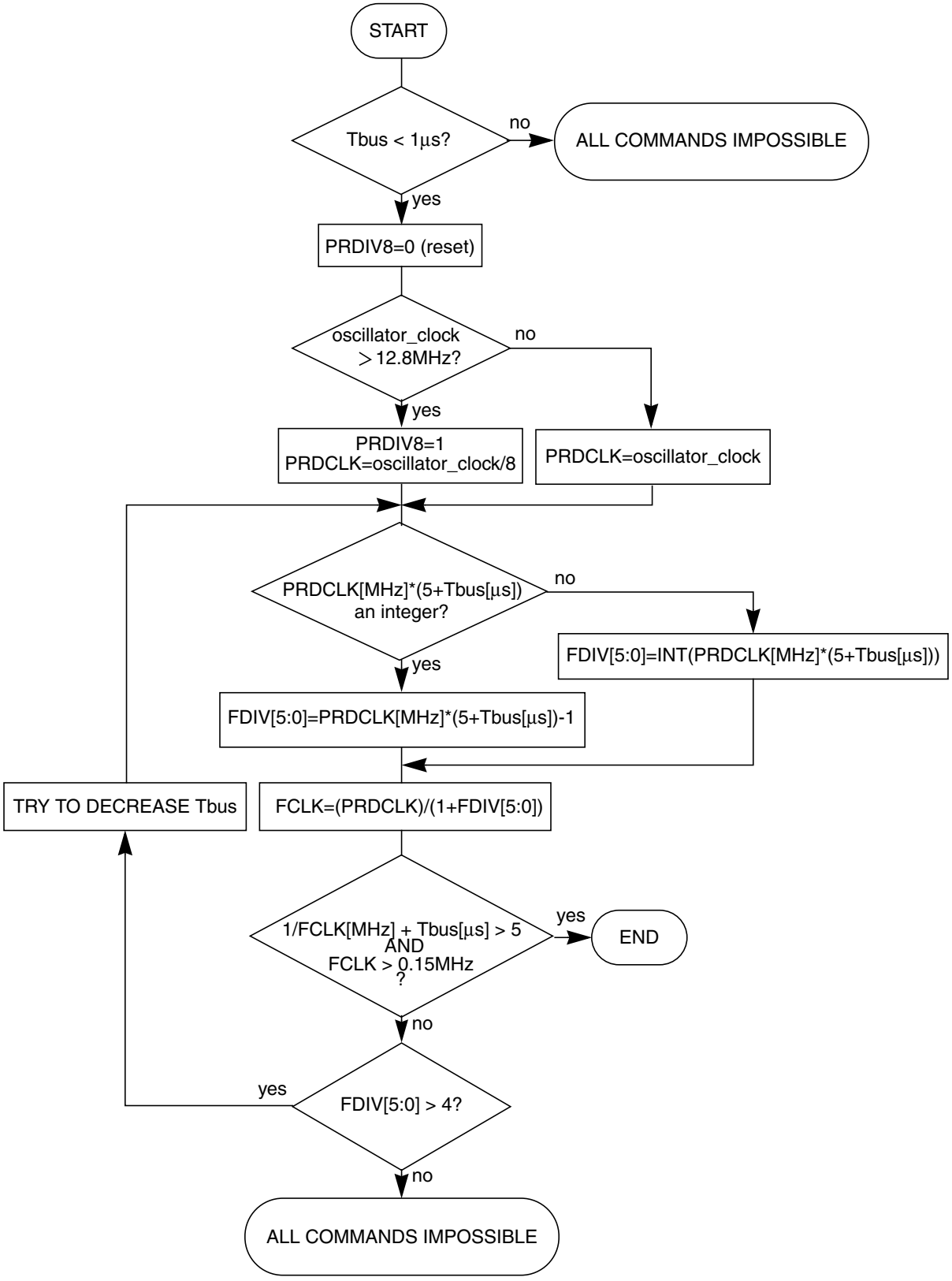
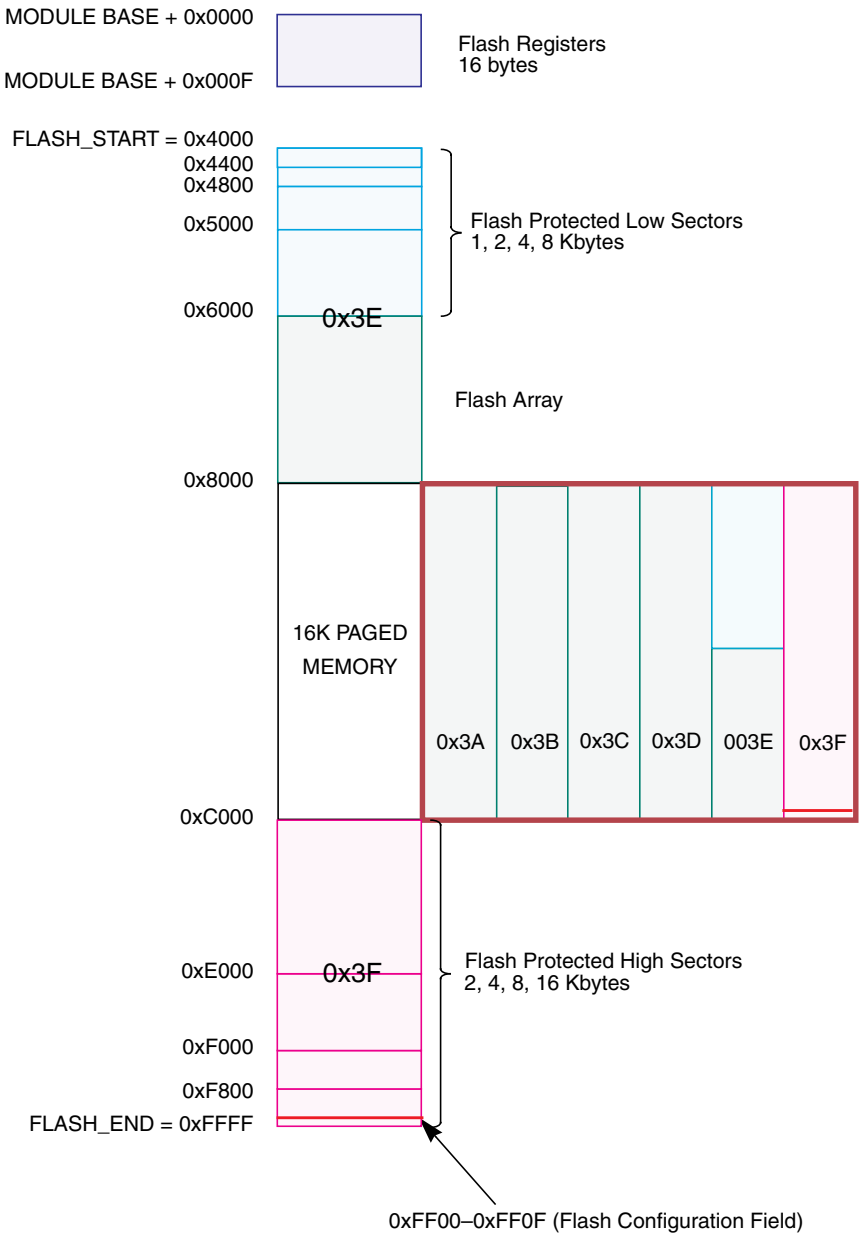


Figure 19-24. PRDIV8 and FDIV Bits Determination Procedure



Note: 0x3A–0x3F correspond to the PPAGE register content

Figure 20-4. Flash Memory Map

A.2.5 ATD Accuracy (3.3V Range)

Table A-13 specifies the ATD conversion performance excluding any errors due to current injection, input capacitance and source resistance.

Table A-13. ATD Conversion Performance

Conditions are shown in Table A-4 unless otherwise noted
$V_{REF} = V_{RH} - V_{RL}$ = 3.328V. Resulting to one 8 bit count = 13mV and one 10 bit count = 3.25mV
f_{ATDCLK} = 2.0MHz

Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	P	10-Bit Resolution	LSB	—	3.25	—	mV
2	P	10-Bit Differential Nonlinearity	DNL	–1.5	—	1.5	Counts
3	P	10-Bit Integral Nonlinearity	INL	–3.5	±1.5	3.5	Counts
4	P	10-Bit Absolute Error(1)	AE	–5	±2.5	5	Counts
5	P	8-Bit Resolution	LSB	—	13	—	mV
6	P	8-Bit Differential Nonlinearity	DNL	–0.5	—	0.5	Counts
7	P	8-Bit Integral Nonlinearity	INL	–1.5	±1	1.5	Counts
8	P	8-Bit Absolute Error[1]	AE	–2.0	±1.5	2.0	Counts

1. These values include the quantization error which is inherently 1/2 count for any A/D converter.

For the following definitions see also Figure A-1.

Differential Non-Linearity (DNL) is defined as the difference between two adjacent switching steps.

$$DNL(i) = \frac{V_i - V_{i-1}}{1LSB} - 1$$

The Integral Non-Linearity (INL) is defined as the sum of all DNLs:

$$INL(n) = \sum_{i=1}^{n} DNL(i) = \frac{V_n - V_0}{1LSB} - n$$