Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	HCS12
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, EBI/EMI, SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	60
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-QFP
Supplier Device Package	80-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s12c64cfue

Chapter 14
Serial Peripheral Interface (SPIV3) Block Description

Chapter 15
Timer Module (TIM16B8CV1) Block Description

0x00E0–0x00FF PWM (Pulse Width Modulator) (continued)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00F6	PWMPER4	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$00F7	PWMPER5	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$00F8	PWMDTY0	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$00F9	PWMDTY1	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$00FA	PWMDTY2	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$00FB	PWMDTY3	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$00FC	PWMDTY4	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$00FD	PWMDTY5	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$00FE	Reserved	Read:	PWMIF	PWMIE	0	PWMLVL	0	PWM5IN	PWM5INL	PWM5ENA
		Write:			PWMRSTRT					
$00FF	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

0x0110–0x013F Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0110–0x003F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

0x0140–0x017F CAN (Scalable Controller Area Network — MSCAN)[1]

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0140	CANCTL0	Read:	RXFRM	RXACT	CSWAI	SYNCH	TIME	WUPE	SLPRQ	INITRQ
		Write:								
0x0141	CANCTL1	Read:	CANE	CLKSRC	LOOPB	LISTEN	0	WUPM	SLPAK	INITAK
		Write:								
0x0142	CANBTR0	Read:	SJW1	SJW0	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0
		Write:								
0x0143	CANBTR1	Read:	SAMP	TSEG22	TSEG21	TSEG20	TSEG13	TSEG12	TSEG11	TSEG10
		Write:								
0x0144	CANRFLG	Read:	WUPIF	CSCIF	RSTAT1	RSTAT0	TSTAT1	TSTAT0	OVRIF	RXF
		Write:								
0x0145	CANRIER	Read:	WUPIE	CSCIE	RSTATE1	RSTATE0	TSTATE1	TSTATE0	OVRIE	RXFIE
		Write:								

the Flash EEPROM memory in the memory map (ROMCTL). At the rising edge of $\overline{\text{RESET}}$, the state of this pin is latched to the ROMON bit.

- PP6 = 1 in emulation modes equates to ROMON = 0 (ROM space externally mapped)
- PP6 = 0 in expanded modes equates to ROMON = 0 (ROM space externally mapped)

1.3.4.19 PP[5:0] / KWP[5:0] / PW[5:0] — Port P I/O Pins [5:0]

PP[5:0] are general purpose input or output pins, shared with the keypad interrupt function. When configured as inputs, they can generate interrupts causing the MCU to exit stop or wait mode.

PP[5:0] are also shared with the PWM output signals, PW[5:0]. Pins PP[2:0] are only available in the 80-pin package version. Pins PP[4:3] are not available in the 48-pin package version.

1.3.4.20 PJ[7:6] / KWJ[7:6] — Port J I/O Pins [7:6]

PJ[7:6] are general purpose input or output pins, shared with the keypad interrupt function. When configured as inputs, they can generate interrupts causing the MCU to exit stop or wait mode. These pins are not available in the 48-pin package version nor in the 52-pin package version.

1.3.4.21 PM5 / SCK — Port M I/O Pin 5

PM5 is a general purpose input or output pin and also the serial clock pin SCK for the serial peripheral interface (SPI).

1.3.4.22 PM4 / MOSI — Port M I/O Pin 4

PM4 is a general purpose input or output pin and also the master output (during master mode) or slave input (during slave mode) pin for the serial peripheral interface (SPI).

1.3.4.23 PM3 / $\overline{\text{SS}}$ — Port M I/O Pin 3

PM3 is a general purpose input or output pin and also the slave select pin $\overline{\text{SS}}$ for the serial peripheral interface (SPI).

1.3.4.24 PM2 / MISO — Port M I/O Pin 2

PM2 is a general purpose input or output pin and also the master input (during master mode) or slave output (during slave mode) pin for the serial peripheral interface (SPI).

1.3.4.25 PM1 / TXCAN — Port M I/O Pin 1

PM1 is a general purpose input or output pin and the transmit pin, TXCAN, of the CAN module if available.

1.3.4.26 PM0 / RXCAN — Port M I/O Pin 0

PM0 is a general purpose input or output pin and the receive pin, RXCAN, of the CAN module if available.

2.3.2.2.6 Port S Polarity Select Register (PPSS)

Module Base + 0x000D

	7	6	5	4	3	2	1	0
R	0	0	0	0	PPSS3	PPSS2	PPSS1	PPSS0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 2-15. Port S Polarity Select Register (PPSS)

Read: Anytime.

Write: Anytime.

Table 2-14. PPSS Field Descriptions

Field	Description
3–0 PPSS[3:0]	**Pull Select Port S** — This register selects whether a pull-down or a pull-up device is connected to the pin. 0 A pull-up device is connected to the associated port S pin, if enabled by the associated bit in register PERS and if the port is used as input or as wired-or output. 1 A pull-down device is connected to the associated port S pin, if enabled by the associated bit in register PERS and if the port is used as input.

2.3.2.2.7 Port S Wired-OR Mode Register (WOMS)

Module Base + 0x000E

	7	6	5	4	3	2	1	0
R	0	0	0	0	WOMS3	WOMS2	WOMS1	WOMS0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 2-16. Port S Wired-Or Mode Register (WOMS)

Read: Anytime.

Write: Anytime.

Table 2-15. WOMS Field Descriptions

Field	Description
3–0 WOMS[3:0]	**Wired-OR Mode Port S** — This register configures the output pins as wired-or. If enabled the output is driven active low only (open-drain). A logic level of “1” is not driven. This bit has no influence on pins used as inputs. 0 Output buffers operate as push-pull outputs. 1 Output buffers operate as open-drain outputs.

2.4.1.4 Reduced Drive Register

If the port is used as an output the register allows the configuration of the drive strength.

2.4.1.5 Pull Device Enable Register

This register turns on a pull-up or pull-down device. It becomes only active if the pin is used as an input or as a wired-or output.

2.4.1.6 Polarity Select Register

This register selects either a pull-up or pull-down device if enabled. It becomes only active if the pin is used as an input. A pull-up device can be activated if the pin is used as a wired-OR output.

2.4.2 Port Descriptions

2.4.2.1 Port T

This port is associated with the Standard Capture Timer. PWM output channels can be rerouted from port P to port pins T. In all modes, port T pins can be used for either general-purpose I/O, Standard Capture Timer I/O or as PWM channels module, if so configured by MODRR.

During reset, port T pins are configured as high-impedance inputs.

2.4.2.2 Port S

This port is associated with the serial SCI module. Port S pins PS[3:0] can be used either for general-purpose I/O, or with the SCI subsystem.

During reset, port S pins are configured as inputs with pull-up.

2.4.2.3 Port M

This port is associated with the MSCAN and SPI module. Port M pins PM[5:0] can be used either for general-purpose I/O, with the MSCAN or SPI subsystems.

During reset, port M pins are configured as inputs with pull-up.

2.4.2.4 Port AD

This port is associated with the ATD module. Port AD pins can be used either for general-purpose I/O, or for the ATD subsystem. There are 2 data port registers associated with the Port AD: PTAD[7:0], located in the PIM and PORTAD[7:0] located in the ATD.

To use PTAD[n] as a standard input port, the corresponding DDRD[n] must be cleared. To use PTAD[n] as a standard output port, the corresponding DDRD[n] must be set

NOTE: To use PORTAD[n], located in the ATD as an input port register, DDRD[n] must be cleared and ATDDIEN[n] must be set. *Please refer to ATD Block Guide for details*.

3.3.2.7 Memory Size Register 0 (MEMSIZ0)

Module Base + 0x001C
Starting address location affected by INITRG register setting.

	7	6	5	4	3	2	1	0
R	REG_SW0	0	EEP_SW1	EEP_SW0	0	RAM_SW2	RAM_SW1	RAM_SW0
W								
Reset	—	—	—	—	—	—	—	—

= Unimplemented or Reserved

Figure 3-9. Memory Size Register 0 (MEMSIZ0)

Read: Anytime

Write: Writes have no effect

Reset: Defined at chip integration, see device overview section.

The MEMSIZ0 register reflects the state of the register, EEPROM and RAM memory space configuration switches at the core boundary which are configured at system integration. This register allows read visibility to the state of these switches.

Table 3-7. MEMSIZ0 Field Descriptions

Field	Description
7 REG_SW0	**Allocated System Register Space** 0 Allocated system register space size is 1K byte 1 Allocated system register space size is 2K byte
5:4 EEP_SW[1:0]	**Allocated System EEPROM Memory Space** — The allocated system EEPROM memory space size is as given in Table 3-8.
2 RAM_SW[2:0]	**Allocated System RAM Memory Space** — The allocated system RAM memory space size is as given in Table 3-9.

Table 3-8. Allocated EEPROM Memory Space

eep_sw1:eep_sw0	Allocated EEPROM Space
00	0K byte
01	2K bytes
10	4K bytes
11	8K bytes

Table 3-9. Allocated RAM Memory Space

ram_sw2:ram_sw0	Allocated RAM Space	RAM Mappable Region	INITRM Bits Used	RAM Reset Base Address[1]
000	2K bytes	2K bytes	RAM[15:11]	0x0800
001	4K bytes	4K bytes	RAM[15:12]	0x0000
010	6K bytes	8K bytes[2]	RAM[15:13]	0x0800

4.3.2.4 Data Direction Register B (DDRB)

Module Base + 0x0003
Starting address location affected by INITRG register setting.

	7	6	5	4	3	2	1	0
R W	Bit 7	6	5	4	3	2	1	Bit 0
Reset	0	0	0	0	0	0	0	0

Figure 4-5. Data Direction Register B (DDRB)

Read: Anytime when register is in the map

Write: Anytime when register is in the map

This register controls the data direction for port B. When port B is operating as a general-purpose I/O port, DDRB determines the primary direction for each port B pin. A 1 causes the associated port pin to be an output and a 0 causes the associated pin to be a high-impedance input. The value in a DDR bit also affects the source of data for reads of the corresponding PORTB register. If the DDR bit is 0 (input) the buffered pin input state is read. If the DDR bit is 1 (output) the associated port data register bit state is read.

This register is not in the on-chip memory map in expanded and special peripheral modes. Therefore, these accesses will be echoed externally. It is reset to 0x00 so the DDR does not override the three-state control signals.

Table 4-4. DDRB Field Descriptions

Field	Description
7:0 DDRB	**Data Direction Port B** 0 Configure the corresponding I/O pin as an input 1 Configure the corresponding I/O pin as an output

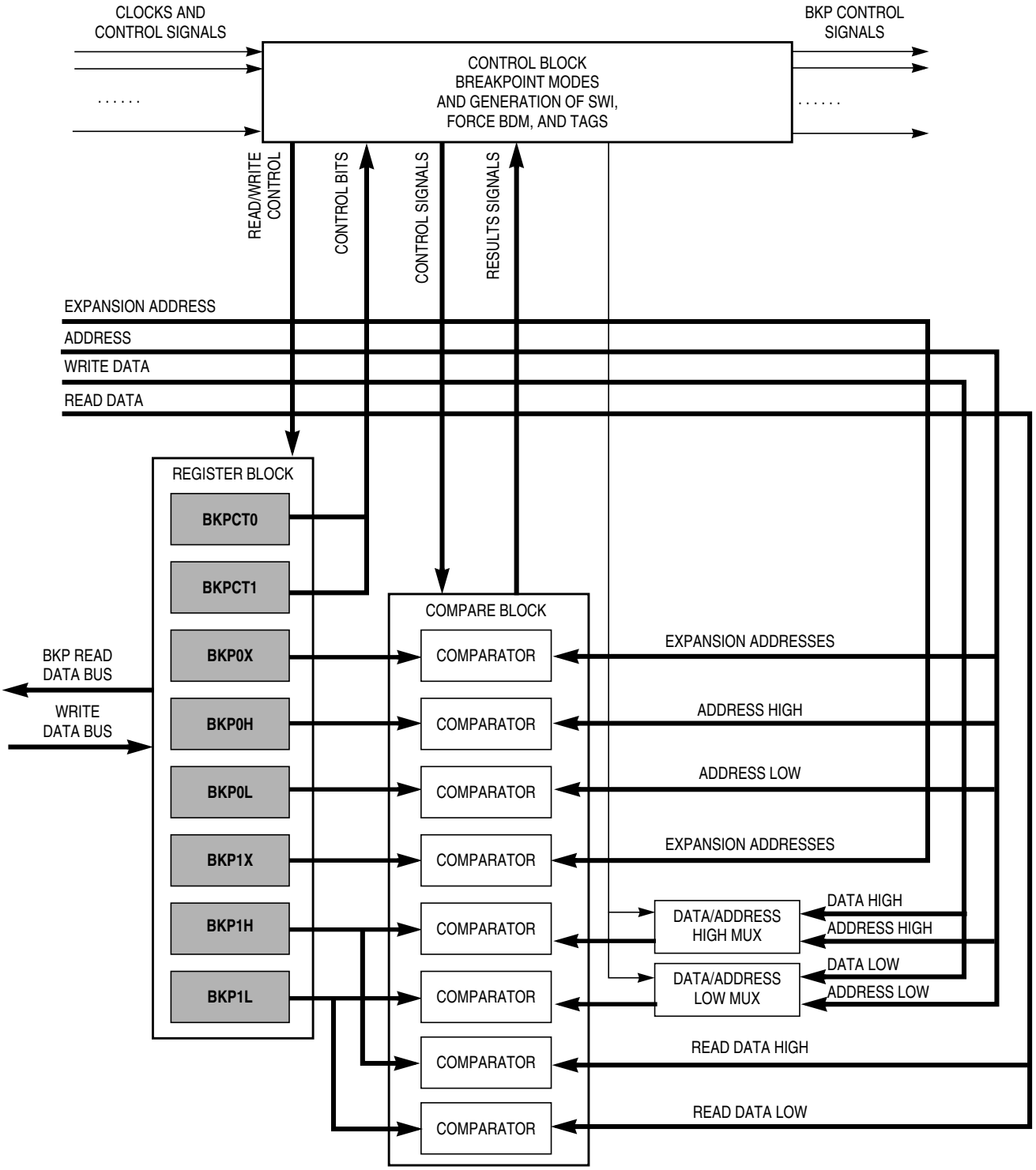

Figure 7-1. DBG Block Diagram in BKP Mode

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x001E	ATDDR7H	R	BIT 9 MSB BIT 7 MSB	BIT 8 BIT 6	BIT 7 BIT 5	BIT 6 BIT 4	BIT 5 BIT 3	BIT 4 BIT 2	BIT 3 BIT 1	BIT 2 BIT 0
		W								
0x001F	ATDDR7L	R	BIT 1 u	BIT 0 u	0 0	0 0	0 0	0 0	0 0	0 0
		W								
Right Justified Result Data										
0x0010	ATDDR0H	R	0 0	0 0	0 0	0 0	0 0	0 0	BIT 9 MSB 0	BIT 8 0
		W								
0x0011	ATDDR0L	R	BIT 7 BIT 7 MSB	BIT 6 BIT 6	BIT 5 BIT 5	BIT 4 BIT 4	BIT 3 BIT 3	BIT 2 BIT 2	BIT 1 BIT 1	BIT 0 BIT 0
		W								
0x0012	ATDDR1H	R	0 0	0 0	0 0	0 0	0 0	0 0	BIT 9 MSB 0	BIT 8 0
		W								
0x0013	ATDDR1L	R	BIT 7 BIT 7 MSB	BIT 6 BIT 6	BIT 5 BIT 5	BIT 4 BIT 4	BIT 3 BIT 3	BIT 2 BIT 2	BIT 1 BIT 1	BIT 0 BIT 0
		W								
0x0014	ATDDR2H	R	0 0	0 0	0 0	0 0	0 0	0 0	BIT 9 MSB 0	BIT 8 0
		W								
0x0015	ATDDR2L	R	BIT 7 BIT 7 MSB	BIT 6 BIT 6	BIT 5 BIT 5	BIT 4 BIT 4	BIT 3 BIT 3	BIT 2 BIT 2	BIT 1 BIT 1	BIT 0 BIT 0
		W								
0x0016	ATDDR3H	R	0 0	0 0	0 0	0 0	0 0	0 0	BIT 9 MSB 0	BIT 8 0
		W								
0x0017	ATDDR3L	R	BIT 7 BIT 7 MSB	BIT 6 BIT 6	BIT 5 BIT 5	BIT 4 BIT 4	BIT 3 BIT 3	BIT 2 BIT 2	BIT 1 BIT 1	BIT 0 BIT 0
		W								
0x0018	ATDDR4H	R	0 0	0 0	0 0	0 0	0 0	0 0	BIT 9 MSB 0	BIT 8 0
		W								
0x0019	ATDDR4L	R	BIT 7 BIT 7 MSB	BIT 6 BIT 6	BIT 5 BIT 5	BIT 4 BIT 4	BIT 3 BIT 3	BIT 2 BIT 2	BIT 1 BIT 1	BIT 0 BIT 0
		W								
0x001A	ATDDR5H	R	0 0	0 0	0 0	0 0	0 0	0 0	BIT 9 MSB 0	BIT 8 0
		W								
0x001B	ATDDR5L	R	BIT 7 BIT 7 MSB	BIT 6 BIT 6	BIT 5 BIT 5	BIT 4 BIT 4	BIT 3 BIT 3	BIT 2 BIT 2	BIT 1 BIT 1	BIT 0 BIT 0
		W								

= Unimplemented or Reserved

Figure 8-2. ATD Register Summary (Sheet 3 of 4)

10.3.2.4 MSCAN Bus Timing Register 1 (CANBTR1)

The CANBTR1 register configures various CAN bus timing parameters of the MSCAN module.

Module Base + 0x0003

	7	6	5	4	3	2	1	0
R W	SAMP	TSEG22	TSEG21	TSEG20	TSEG13	TSEG12	TSEG11	TSEG10
Reset:	0	0	0	0	0	0	0	0

Figure 10-7. MSCAN Bus Timing Register 1 (CANBTR1)

Read: Anytime
Write: Anytime in initialization mode (INITRQ = 1 and INITAK = 1)

Table 10-6. CANBTR1 Register Field Descriptions

Field	Description
7 SAMP	**Sampling** — This bit determines the number of CAN bus samples taken per bit time. 0 One sample per bit. 1 Three samples per bit(1). If SAMP = 0, the resulting bit value is equal to the value of the single bit positioned at the sample point. If SAMP = 1, the resulting bit value is determined by using majority rule on the three total samples. For higher bit rates, it is recommended that only one sample is taken per bit time (SAMP = 0).
6:4 TSEG2[2:0]	**Time Segment 2** — Time segments within the bit time fix the number of clock cycles per bit time and the location of the sample point (see Figure 10-43). Time segment 2 (TSEG2) values are programmable as shown in Table 10-7.
3:0 TSEG1[3:0]	**Time Segment 1** — Time segments within the bit time fix the number of clock cycles per bit time and the location of the sample point (see Figure 10-43). Time segment 1 (TSEG1) values are programmable as shown in Table 10-8.

1. In this case, PHASE_SEG1 must be at least 2 time quanta (Tq).

Table 10-7. Time Segment 2 Values

TSEG22	TSEG21	TSEG20	Time Segment 2
0	0	0	1 Tq clock cycle(1)
0	0	1	2 Tq clock cycles
:	:	:	:
1	1	0	7 Tq clock cycles
1	1	1	8 Tq clock cycles

1. This setting is not valid. Please refer to Table 10-34 for valid settings.

Table 10-8. Time Segment 1 Values

TSEG13	TSEG12	TSEG11	TSEG10	Time segment 1
0	0	0	0	1 Tq clock cycle(1)
0	0	0	1	2 Tq clock cycles[1]
0	0	1	0	3 Tq clock cycles[1]
0	0	1	1	4 Tq clock cycles
:	:	:	:	:
1	1	1	0	15 Tq clock cycles
1	1	1	1	16 Tq clock cycles

1. This setting is not valid. Please refer to Table 10-34 for valid settings.

The bit time is determined by the oscillator frequency, the baud rate prescaler, and the number of time quanta (Tq) clock cycles per bit (as shown in Table 10-7 and Table 10-8).

Eqn. 10-1

$$\text{Bit Time} = \frac{(\text{Prescaler value})}{f_{CANCLK}} \bullet (1 + \text{TimeSegment1} + \text{TimeSegment2})$$

10.3.2.5 MSCAN Receiver Flag Register (CANRFLG)

A flag can be cleared only by software (writing a 1 to the corresponding bit position) when the condition which caused the setting is no longer valid. Every flag has an associated interrupt enable bit in the CANRIER register.

Module Base + 0x0004

	7	6	5	4	3	2	1	0
R	WUPIF	CSCIF	RSTAT1	RSTAT0	TSTAT1	TSTAT0	OVRIF	RXF
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 10-8. MSCAN Receiver Flag Register (CANRFLG)

NOTE

The CANRFLG register is held in the reset state[1] when the initialization mode is active (INITRQ = 1 and INITAK = 1). This register is writable again as soon as the initialization mode is exited (INITRQ = 0 and INITAK = 0).

Read: Anytime
Write: Anytime when out of initialization mode, except RSTAT[1:0] and TSTAT[1:0] flags which are read-only; write of 1 clears flag; write of 0 is ignored.

1. The RSTAT[1:0], TSTAT[1:0] bits are not affected by initialization mode.

Table 12-1. PWM8B6CV1 Memory Map

Address Offset	Register	Access
0x0000	PWM Enable Register (PWME)	R/W
0x0001	PWM Polarity Register (PWMPOL)	R/W
0x0002	PWM Clock Select Register (PWMCLK)	R/W
0x0003	PWM Prescale Clock Select Register (PWMPRCLK)	R/W
0x0004	PWM Center Align Enable Register (PWMCAE)	R/W
0x0005	PWM Control Register (PWMCTL)	R/W
0x0006	PWM Test Register (PWMTST)(1)	R/W
0x0007	PWM Prescale Counter Register (PWMPRSC)(2)	R/W
0x0008	PWM Scale A Register (PWMSCLA)	R/W
0x0009	PWM Scale B Register (PWMSCLB)	R/W
0x000A	PWM Scale A Counter Register (PWMSCNTA)(3)	R/W
0x000B	PWM Scale B Counter Register (PWMSCNTB)(4)	R/W
0x000C	PWM Channel 0 Counter Register (PWMCNT0)	R/W
0x000D	PWM Channel 1 Counter Register (PWMCNT1)	R/W
0x000E	PWM Channel 2 Counter Register (PWMCNT2)	R/W
0x000F	PWM Channel 3 Counter Register (PWMCNT3)	R/W
0x0010	PWM Channel 4 Counter Register (PWMCNT4)	R/W
0x0011	PWM Channel 5 Counter Register (PWMCNT5)	R/W
0x0012	PWM Channel 0 Period Register (PWMPER0)	R/W
0x0013	PWM Channel 1 Period Register (PWMPER1)	R/W
0x0014	PWM Channel 2 Period Register (PWMPER2)	R/W
0x0015	PWM Channel 3 Period Register (PWMPER3)	R/W
0x0016	PWM Channel 4 Period Register (PWMPER4)	R/W
0x0017	PWM Channel 5 Period Register (PWMPER5)	R/W
0x0018	PWM Channel 0 Duty Register (PWMDTY0)	R/W
0x0019	PWM Channel 1 Duty Register (PWMDTY1)	R/W
0x001A	PWM Channel 2 Duty Register (PWMDTY2)	R/W
0x001B	PWM Channel 3 Duty Register (PWMDTY3)	R/W
0x001C	PWM Channel 4 Duty Register (PWMDTY4)	R/W
0x001D	PWM Channel 5 Duty Register (PWMDTY5)	R/W
0x001E	PWM Shutdown Register (PWMSDN)	R/W

1. PWMTST is intended for factory test purposes only.
2. PWMPRSC is intended for factory test purposes only.
3. PWMSCNTA is intended for factory test purposes only.
4. PWMSCNTB is intended for factory test purposes only.

12.4 Functional Description

12.4.1 PWM Clock Select

There are four available clocks called clock A, clock B, clock SA (scaled A), and clock SB (scaled B). These four clocks are based on the bus clock**.**

Clock A and B can be software selected to be 1, 1/2, 1/4, 1/8,..., 1/64, 1/128 times the bus clock. Clock SA uses clock A as an input and divides it further with a reloadable counter. Similarly, clock SB uses clock B as an input and divides it further with a reloadable counter. The rates available for clock SA are software selectable to be clock A divided by 2, 4, 6, 8, ..., or 512 in increments of divide by 2. Similar rates are available for clock SB. Each PWM channel has the capability of selecting one of two clocks, either the pre-scaled clock (clock A or B) or the scaled clock (clock SA or SB).

The block diagram in Figure 12-34 shows the four different clocks and how the scaled clocks are created.

12.4.1.1 Prescale

The input clock to the PWM prescaler is the bus clock. It can be disabled whenever the part is in freeze mode by setting the PFRZ bit in the PWMCTL register. If this bit is set, whenever the MCU is in freeze mode the input clock to the prescaler is disabled. This is useful for emulation in order to freeze the PWM. The input clock can also be disabled when all six PWM channels are disabled (PWME5–PWME0 = 0) This is useful for reducing power by disabling the prescale counter.

Clock A and clock B are scaled values of the input clock. The value is software selectable for both clock A and clock B and has options of 1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, or 1/128 times the bus clock. The value selected for clock A is determined by the PCKA2, PCKA1, and PCKA0 bits in the PWMPRCLK register. The value selected for clock B is determined by the PCKB2, PCKB1, and PCKB0 bits also in the PWMPRCLK register.

13.3.2.5 SCI Status Register 2 (SCISR2)

Module Base + 0x_0005

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	BK13	TXDIR	RAF
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 13-7. SCI Status Register 2 (SCISR2)

Read: Anytime

Write: Anytime; writing accesses SCI status register 2; writing to any bits except TXDIR and BRK13 (SCISR2[1] & [2]) has no effect

Table 13-6. SCISR2 Field Descriptions

Field	Description
2 BK13	**Break Transmit Character Length** — This bit determines whether the transmit break character is 10 or 11 bit respectively 13 or 14 bits long. The detection of a framing error is not affected by this bit. 0 Break Character is 10 or 11 bit long 1 Break character is 13 or 14 bit long
1 TXDIR	**Transmitter Pin Data Direction in Single-Wire Mode.** — This bit determines whether the TXD pin is going to be used as an input or output, in the Single-Wire mode of operation. This bit is only relevant in the Single-Wire mode of operation. 0 TXD pin to be used as an input in Single-Wire mode 1 TXD pin to be used as an output in Single-Wire mode
0 RAF	**Receiver Active Flag** — RAF is set when the receiver detects a logic 0 during the RT1 time period of the start bit search. RAF is cleared when the receiver detects an idle character. 0 No reception in progress 1 Reception in progress

With the misaligned character shown in Figure 13-20, the receiver counts 167 RTr cycles at the point when the count of the transmitting device is 10 bit times x 16 RTt cycles = 160 RTt cycles.

The maximum percent difference between the receiver count and the transmitter count of a slow 9-bit character with no errors is:

((167 – 160) / 167) X 100 = 4.19%

13.4.4.5.2 Fast Data Tolerance

Figure 13-21 shows how much a fast received frame can be misaligned. The fast stop bit ends at RT10 instead of RT16 but is still sampled at RT8, RT9, and RT10.

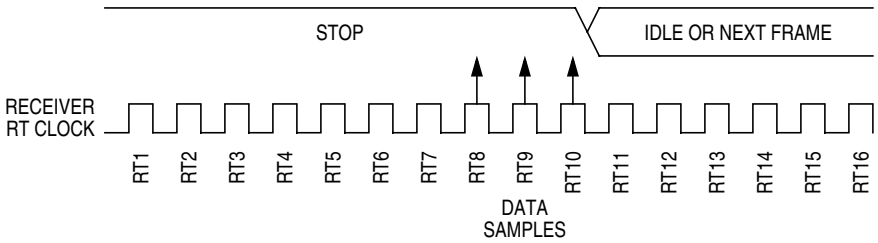

Figure 13-21. Fast Data

For an 8-bit data character, it takes the receiver 9 bit times x 16 RTr cycles + 10 RTr cycles = 154 RTr cycles to finish data sampling of the stop bit.

With the misaligned character shown in Figure 13-21, the receiver counts 154 RTr cycles at the point when the count of the transmitting device is 10 bit times x 16 RTt cycles = 160 RTt cycles.

The maximum percent difference between the receiver count and the transmitter count of a fast 8-bit character with no errors is:

((160 – 154) / 160) x 100 = 3.75%

For a 9-bit data character, it takes the receiver 10 bit times x 16 RTr cycles + 10 RTr cycles = 170 RTr cycles to finish data sampling of the stop bit.

With the misaligned character shown in Figure 13-21, the receiver counts 170 RTr cycles at the point when the count of the transmitting device is 11 bit times x 16 RTt cycles = 176 RTt cycles.

The maximum percent difference between the receiver count and the transmitter count of a fast 9-bit character with no errors is:

((176 – 170) / 176) x 100 = 3.40%

13.4.4.6 Receiver Wakeup

To enable the SCI to ignore transmissions intended only for other receivers in multiple-receiver systems, the receiver can be put into a standby state. Setting the receiver wakeup bit, RWU, in SCI control register 2 (SCICR2) puts the receiver into standby state during which receiver interrupts are disabled.The SCI will still load the receive data into the SCIDRH/L registers, but it will not set the RDRF flag.

Chapter 15
Timer Module (TIM16B8CV1) Block Description

Table 15-1. Revision History

Version Number	Revision Dates	Effective Date	Author	Description of Changes
01.03	06 Feb 2006	06 Feb 2006	S. Chinnam	Corrected the type at 0x006 and later in the document from TSCR2 and TSCR1
01.04	08 July 2008	08 July 2008	S. Chinnam	Revised flag clearing procedure, whereby TEN bit must be set when clearing flags.
01.05	05 May 2010	05 May 2010	Ame Wang	-in 15.3.2.8/15-446,add Table 15-11 -in 15.3.2.11/15-450,TCRE bit description part,add Note -in 15.4.3/15-459,add Figure 15-29

15.1 Introduction

The basic timer consists of a 16-bit, software-programmable counter driven by a seven-stage programmable prescaler.

This timer can be used for many purposes, including input waveform measurements while simultaneously generating an output waveform. Pulse widths can vary from microseconds to many seconds.

This timer contains 8 complete input capture/output compare channels and one pulse accumulator. The input capture function is used to detect a selected transition edge and record the time. The output compare function is used for generating output signals or for timer software delays. The 16-bit pulse accumulator is used to operate as a simple event counter or a gated time accumulator. The pulse accumulator shares timer channel 7 when in event mode.

A full access for the counter registers or the input capture/output compare registers should take place in one clock cycle. Accessing high byte and low byte separately for all of these registers may not yield the same result as accessing them in one word.

15.1.1 Features

The TIM16B8CV1 includes these distinctive features:

- Eight input capture/output compare channels.
- Clock prescaling.
- 16-bit counter.
- 16-bit pulse accumulator.

Table 17-13. FCMD Field Descriptions

Field	Description
6, 5, 2, 0 CMDB[6:5] CMDB[2] CMDB[0]	Valid Flash commands are shown in Table 17-14. An attempt to execute any command other than those listed in Table 17-14 will set the ACCERR bit in the FSTAT register (see Section 17.3.2.6).

Table 17-14. Valid Flash Command List

CMDB	NVM Command
0x05	Erase verify
0x20	Word program
0x40	Sector erase
0x41	Mass erase

17.3.2.8 RESERVED2

This register is reserved for factory testing and is not accessible to the user.

Module Base + 0x0007

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 17-12. RESERVED2

All bits read 0 and are not writable.

17.3.2.9 Flash Address Register (FADDR)

FADDRHI and FADDRLO are the Flash address registers.

Module Base + 0x0008

	7	6	5	4	3	2	1	0
R	0	0	0	FABHI				
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 17-13. Flash Address High Register (FADDRHI)

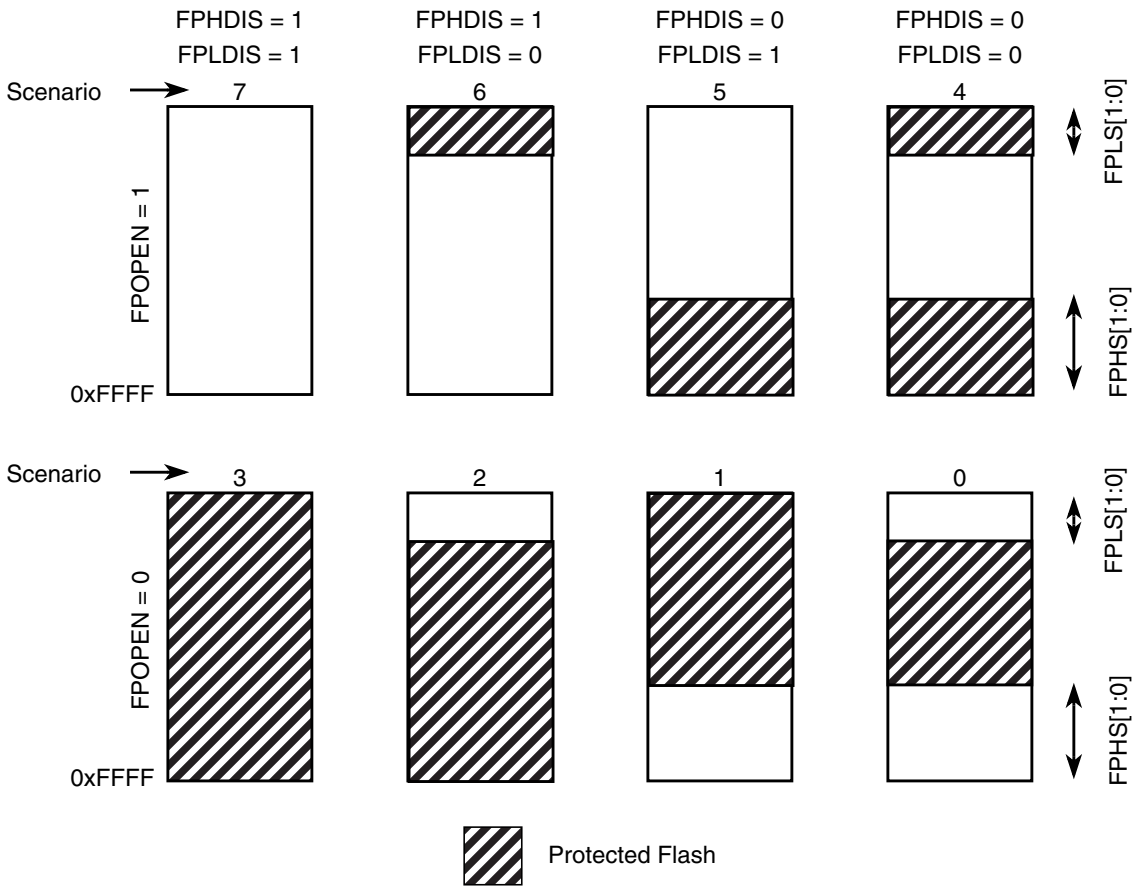

Figure 19-11. Flash Protection Scenarios

19.3.2.5.1 Flash Protection Restrictions

The general guideline is that protection can only be added, not removed. All valid transitions between Flash protection scenarios are specified in Table 19-13. Any attempt to write an invalid scenario to the FPROT register will be ignored and the FPROT register will remain unchanged. The contents of the FPROT register reflect the active protection scenario.

Table 19-13. Flash Protection Scenario Transitions

From Protection Scenario	To Protection Scenario[1]							
	0	1	2	3	4	5	6	7
0	X	X	X	X				
1		X		X				
2			X	X				
3				X				
4				X	X			
5			X	X	X	X		

19.4.1.3.2 Program Command

The program operation will program a previously erased word in the Flash array using an embedded algorithm.

An example flow to execute the program operation is shown in Figure 19-26. The program command write sequence is as follows:

1. Write to a Flash array address to start the command write sequence for the program command. The data written will be programmed to the Flash array address written.
2. Write the program command, 0x20, to the FCMD register.
3. Clear the CBEIF flag in the FSTAT register by writing a 1 to CBEIF to launch the program command.

If a word to be programmed is in a protected area of the Flash array, the PVIOL flag in the FSTAT register will set and the program command will not launch. Once the program command has successfully launched, the CCIF flag in the FSTAT register will set after the program operation has completed unless a new command write sequence has been buffered. By executing a new program command write sequence on sequential words after the CBEIF flag in the FSTAT register has been set, up to 55% faster programming time per word can be effectively achieved than by waiting for the CCIF flag to set after each program operation.

21.4.1.3.1 Erase Verify Command

The erase verify operation will verify that a Flash array is erased.

An example flow to execute the erase verify operation is shown in Figure 21-22. The erase verify command write sequence is as follows:

1. Write to a Flash array address to start the command write sequence for the erase verify command. The address and data written will be ignored.
2. Write the erase verify command, 0x05, to the FCMD register.
3. Clear the CBEIF flag in the FSTAT register by writing a 1 to CBEIF to launch the erase verify command.

After launching the erase verify command, the CCIF flag in the FSTAT register will set after the operation has completed unless a new command write sequence has been buffered. Upon completion of the erase verify operation, the BLANK flag in the FSTAT register will be set if all addresses in the Flash array are verified to be erased. If any address in the Flash array is not erased, the erase verify operation will terminate and the BLANK flag in the FSTAT register will remain clear.