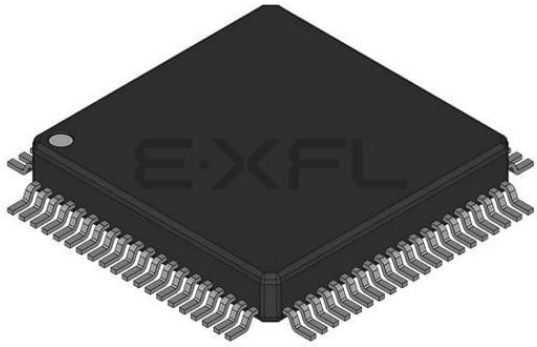

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Details	
Product Status	Active
Core Processor	HCS12
Core Size	16-Bit
Speed	25MHz
Connectivity	EBI/EMI, SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	60
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	80-QFP
Supplier Device Package	80-QFP (14x14)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9s12gc128mfue

0x00C8–0x00CF SCI (Asynchronous Serial Interface) (continued)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00CD	SCISR2	Read:	0	0	0	0	0	BRK13	TXDIR	RAF
		Write:								
0x00CE	SCIDRH	Read:	R8	T8	0	0	0	0	0	0
		Write:								
0x00CF	SCIDRL	Read:	R7	R6	R5	R4	R3	R2	R1	R0
		Write:	T7	T6	T5	T4	T3	T2	T1	T0

0x00D0–0x00D7 Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00D0–0x00D7	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

0x00D8–0x00DF SPI (Serial Peripheral Interface)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00D8	SPICR1	Read: Write:	SPIE	SPE	SPTIE	MSTR	CPOL	CPHA	SSOE	LSBFE
0x00D9	SPICR2	Read:	0	0	0	MODFEN	BIDIROE	0	SPISWAI	SPC0
		Write:								
0x00DA	SPIBR	Read:	0	SPPR2	SPPR1	SPPR0	0	SPR2	SPR1	SPR0
		Write:								
0x00DB	SPISR	Read:	SPIF	0	SPTEF	MODF	0	0	0	0
		Write:								
0x00DC	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
0x00DD	SPIDR	Read: Write:	Bit7	6	5	4	3	2	1	Bit0
0x00DE	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
0x00DF	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

2.3.2.1.2 Port T Input Register (PTIT)

Module Base + 0x0001

	7	6	5	4	3	2	1	0
R	PTIT7	PTIT6	PTIT5	PTIT4	PTIT3	PTIT2	PTIT1	PTIT0
W								
Reset	—	—	—	—	—	—	—	—

= Unimplemented or Reserved

Figure 2-4. Port T Input Register (PTIT)

Read: Anytime.

Write: Never, writes to this register have no effect.

Table 2-4. PTIT Field Descriptions

Field	Description
7–0 PTIT[7:0]	**Port T Input Register** — This register always reads back the status of the associated pins. This can also be used to detect overload or short circuit conditions on output pins.

2.3.2.1.3 Port T Data Direction Register (DDRT)

Module Base + 0x0002

	7	6	5	4	3	2	1	0
R W	DDRT7	DDRT6	DDRT5	DDRT4	DDRT3	DDRT2	DDRT1	DDRT0
Reset	0	0	0	0	0	0	0	0

Figure 2-5. Port T Data Direction Register (DDRT)

Read: Anytime.

Write: Anytime.

Table 2-5. DDRT Field Descriptions

Field	Description
7–0 DDRT[7:0]	**Data Direction Port T** — This register configures each port T pin as either input or output. The standard TIM / PWM modules forces the I/O state to be an output for each standard TIM / PWM module port associated with an enabled output compare. In these cases the data direction bits will not change. The DDRT bits revert to controlling the I/O direction of a pin when the associated timer output compare is disabled. The timer input capture always monitors the state of the pin. 0 Associated pin is configured as input. 1 Associated pin is configured as output. **Note:** Due to internal synchronization circuits, it can take up to 2 bus cycles until the correct value is read on PTT or PTIT registers, when changing the DDRT register.

3.3.2.7 Memory Size Register 0 (MEMSIZ0)

Module Base + 0x001C
Starting address location affected by INITRG register setting.

	7	6	5	4	3	2	1	0
R	REG_SW0	0	EEP_SW1	EEP_SW0	0	RAM_SW2	RAM_SW1	RAM_SW0
W								
Reset	—	—	—	—	—	—	—	—

= Unimplemented or Reserved

Figure 3-9. Memory Size Register 0 (MEMSIZ0)

Read: Anytime

Write: Writes have no effect

Reset: Defined at chip integration, see device overview section.

The MEMSIZ0 register reflects the state of the register, EEPROM and RAM memory space configuration switches at the core boundary which are configured at system integration. This register allows read visibility to the state of these switches.

Table 3-7. MEMSIZ0 Field Descriptions

Field	Description
7 REG_SW0	**Allocated System Register Space** 0 Allocated system register space size is 1K byte 1 Allocated system register space size is 2K byte
5:4 EEP_SW[1:0]	**Allocated System EEPROM Memory Space** — The allocated system EEPROM memory space size is as given in Table 3-8.
2 RAM_SW[2:0]	**Allocated System RAM Memory Space** — The allocated system RAM memory space size is as given in Table 3-9.

Table 3-8. Allocated EEPROM Memory Space

eep_sw1:eep_sw0	Allocated EEPROM Space
00	0K byte
01	2K bytes
10	4K bytes
11	8K bytes

Table 3-9. Allocated RAM Memory Space

ram_sw2:ram_sw0	Allocated RAM Space	RAM Mappable Region	INITRM Bits Used	RAM Reset Base Address[1]
000	2K bytes	2K bytes	RAM[15:11]	0x0800
001	4K bytes	4K bytes	RAM[15:12]	0x0000
010	6K bytes	8K bytes[2]	RAM[15:13]	0x0800

Table 5-2. ITCR Field Descriptions

Field	Description
4 WRTINT	**Write to the Interrupt Test Registers** Read: anytime Write: only in special modes and with I-bit mask and X-bit mask set. 0 Disables writes to the test registers; reads of the test registers will return the state of the interrupt inputs. 1 Disconnect the interrupt inputs from the priority decoder and use the values written into the ITEST registers instead. **Note:** Any interrupts which are pending at the time that WRTINT is set will remain until they are overwritten.
3:0 ADR[3:0]	**Test Register Select Bits** Read: anytime Write: anytime These bits determine which test register is selected on a read or write. The hexadecimal value written here will be the same as the upper nibble of the lower byte of the vector selects. That is, an “F” written into ADR[3:0] will select vectors 0xFFFE–0xFFF0 while a “7” written to ADR[3:0] will select vectors 0xFF7E–0xFF70.

5.3.2.2 Interrupt Test Registers

Module Base + 0x0016
Starting address location affected by INITRG register setting.

	7	6	5	4	3	2	1	0
R W	INTE	INTC	INTA	INT8	INT6	INT4	INT2	INT0
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 5-3. Interrupt TEST Registers (ITEST)

Read: Only in special modes. Reads will return either the state of the interrupt inputs of the interrupt sub-block (WRTINT = 0) or the values written into the TEST registers (WRTINT = 1). Reads will always return 0s in normal modes.

Write: Only in special modes and with WRTINT = 1 and CCR I mask = 1.

7.3.2.5 Debug Comparator C Extended Register (DBGCCX)

Module Base + 0x0025
Starting address location affected by INITRG register setting.

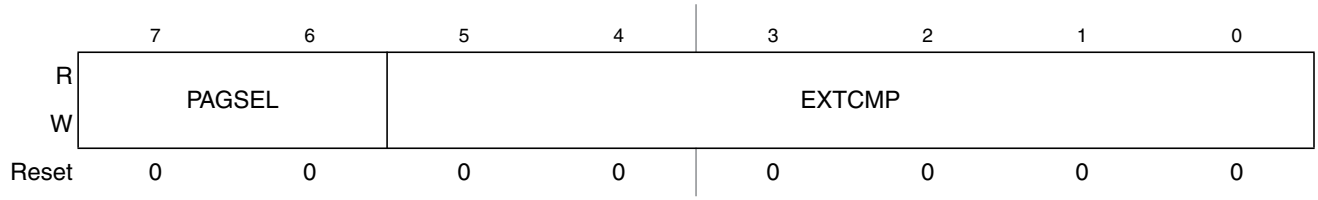

Figure 7-9. Debug Comparator C Extended Register (DBGCCX)

Table 7-10. DBGCCX Field Descriptions

Field	Description
7:6 PAGSEL	**Page Selector Field** — In both BKP and DBG mode, PAGSEL selects the type of paging as shown in Table 7-11. DPAGE and EPAGE are not yet implemented so the value in bit 7 will be ignored (i.e., PAGSEL values of 10 and 11 will be interpreted as values of 00 and 01, respectively).
5:0 EXTCMP	**Comparator C Extended Compare Bits** — The EXTCMP bits are used as comparison address bits as shown in Table 7-11 along with the appropriate PPAGE, DPAGE, or EPAGE signal from the core. **Note:** Comparator C can be used when the DBG module is configured for BKP mode. Extended addressing comparisons for comparator C use PAGSEL and will operate differently to the way that comparator A and B operate in BKP mode.

Table 7-11. PAGSEL Decoding(1)

PAGSEL	Description	EXTCMP	Comment
00	Normal (64k)	Not used	No paged memory
01	PPAGE (256 — 16K pages)	EXTCMP[5:0] is compared to address bits [21:16](2)	PPAGE[7:0] / XAB[21:14] becomes address bits [21:14]1
10(3)	DPAGE (reserved) (256 — 4K pages)	EXTCMP[3:0] is compared to address bits [19:16]	DPAGE / XAB[21:14] becomes address bits [19:12]
112	EPAGE (reserved) (256 — 1K pages)	EXTCMP[1:0] is compared to address bits [17:16]	EPAGE / XAB[21:14] becomes address bits [17:10]

1. See Figure 7-10.
2. Current HCS12 implementations have PPAGE limited to 6 bits. Therefore, EXTCMP[5:4] should be set to 00.
3. Data page (DPAGE) and Extra page (EPAGE) are reserved for implementation on devices that support paged data and extra space.

8.1.2.2 MCU Operating Modes

- **Stop Mode**

  Entering stop mode causes all clocks to halt and thus the system is placed in a minimum power standby mode. This aborts any conversion sequence in progress. During recovery from stop mode, there must be a minimum delay for the stop recovery time, t_{SR}, before initiating a new ATD conversion sequence.

- **Wait Mode**

  Entering wait mode the ATD conversion either continues or aborts for low power depending on the logical value of the AWAIT bit.

- **Freeze Mode**

  In freeze mode the ATD10B8C will behave according to the logical values of the FRZ1 and FRZ0 bits. This is useful for debugging and emulation.

8.1.3 Block Diagram

Figure 8-1 is a block diagram of the ATD.

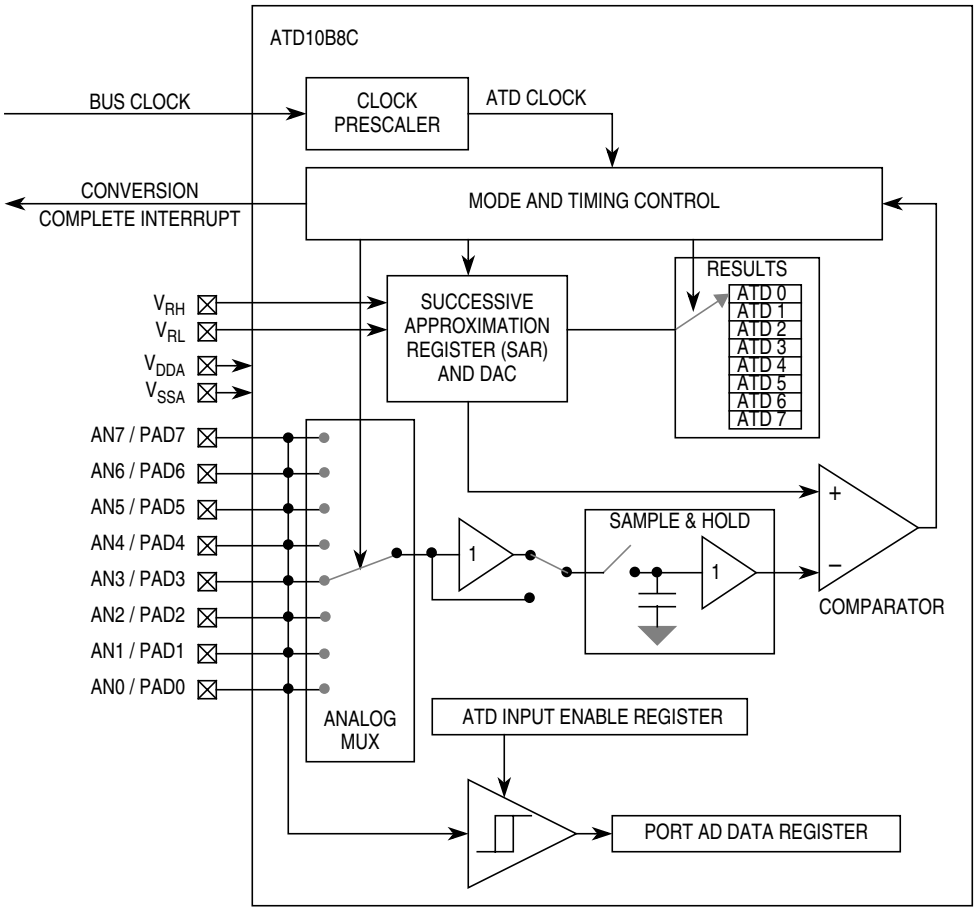

Figure 8-1. ATD10B8C Block Diagram

9.4.2 System Clocks Generator

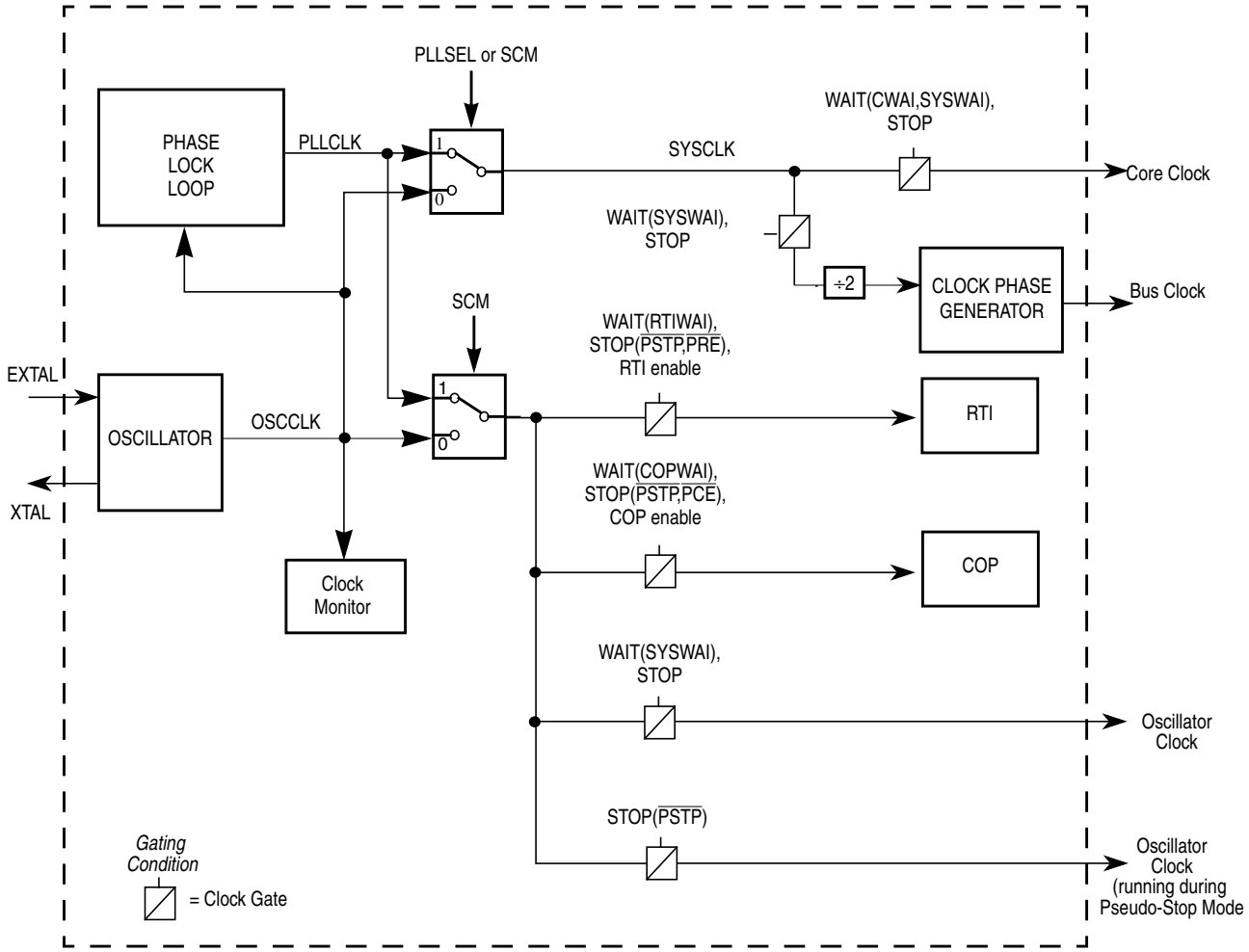

Figure 9-17. System Clocks Generator

The clock generator creates the clocks used in the MCU (see Figure 9-17). The gating condition placed on top of the individual clock gates indicates the dependencies of different modes (stop, wait) and the setting of the respective configuration bits.

The peripheral modules use the bus clock. Some peripheral modules also use the oscillator clock. The memory blocks use the bus clock. If the MCU enters self-clock mode (see Section 9.4.7.2, “Self-Clock Mode”), oscillator clock source is switched to PLLCLK running at its minimum frequency f_{SCM}. The bus clock is used to generate the clock visible at the ECLK pin. The core clock signal is the clock for the CPU. The core clock is twice the bus clock as shown in Figure 9-18. But note that a CPU cycle corresponds to one bus clock.

PLL clock mode is selected with PLLSEL bit in the CLKSEL register. When selected, the PLL output clock drives SYSCLK for the main system including the CPU and peripherals. The PLL cannot be turned off by clearing the PLLON bit, if the PLL clock is selected. When PLLSEL is changed, it takes a maximum

11.3 Memory Map and Register Definition

The CRG contains the registers and associated bits for controlling and monitoring the OSCV2 module.

11.4 Functional Description

The OSCV2 block has two external pins, EXTAL and XTAL. The oscillator input pin, EXTAL, is intended to be connected to either a crystal or an external clock source. The selection of Colpitts oscillator or Pierce oscillator/external clock depends on the XCLKS signal which is sampled during reset. The XTAL pin is an output signal that provides crystal circuit feedback.

A buffered EXTAL signal, OSCCLK, becomes the internal reference clock. To improve noise immunity, the oscillator is powered by the V_{DDPLL} and V_{SSPLL} power supply pins.

The Pierce oscillator can be used for higher frequencies compared to the low power Colpitts oscillator.

11.4.1 Amplitude Limitation Control (ALC)

The Colpitts oscillator is equipped with a feedback system which does not waste current by generating harmonics. Its configuration is “Colpitts oscillator with translated ground.” The transconductor used is driven by a current source under the control of a peak detector which will measure the amplitude of the AC signal appearing on EXTAL node in order to implement an amplitude limitation control (ALC) loop. The ALC loop is in charge of reducing the quiescent current in the transconductor as a result of an increase in the oscillation amplitude. The oscillation amplitude can be limited to two values. The normal amplitude which is intended for non power saving modes and a small amplitude which is intended for low power operation modes. Please refer to the CRG block description chapter for the control and assignment of the amplitude value to operation modes.

11.4.2 Clock Monitor (CM)

The clock monitor circuit is based on an internal resistor-capacitor (RC) time delay so that it can operate without any MCU clocks. If no OSCCLK edges are detected within this RC time delay, the clock monitor indicates a failure which asserts self clock mode or generates a system reset depending on the state of SCME bit. If the clock monitor is disabled or the presence of clocks is detected no failure is indicated.The clock monitor function is enabled/disabled by the CME control bit, described in the CRG block description chapter.

11.5 Interrupts

OSCV2 contains a clock monitor, which can trigger an interrupt or reset. The control bits and status bits for the clock monitor are described in the CRG block description chapter.

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x000F PWMCNT3	R	Bit 7	6	5	4	3	2	1	Bit 0
	W	0	0	0	0	0	0	0	0
0x0010 PWMCNT4	R	Bit 7	6	5	4	3	2	1	Bit 0
	W	0	0	0	0	0	0	0	0
0x0011 PWMCNT5	R	Bit 7	6	5	4	3	2	1	Bit 0
	W	0	0	0	0	0	0	0	0
0x0012 PWMPER0	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x0013 PWMPER1	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x0014 PWMPER2	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x0015 PWMPER3	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x0016 PWMPER4	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x0017 PWMPER5	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x0018 PWMDTY0	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x0019 PWMPER1	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x001A PWMPER2	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x001B PWMPER3	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x001C PWMPER4	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x001D PWMPER5	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x001E PWMSDB	R	PWMIF	PWMIE	0	PWMLVL	0	PWM5IN	PWM5INL	PWM5ENA
	W			PWMRSTRT					

= Unimplemented or Reserved

Figure 12-2. PWM Register Summary (continued)

12.4.2.1 PWM Enable

Each PWM channel has an enable bit (PWMEx) to start its waveform output. When any of the PWMEx bits are set (PWMEx = 1), the associated PWM output signal is enabled immediately. However, the actual PWM waveform is not available on the associated PWM output until its clock source begins its next cycle due to the synchronization of PWMEx and the clock source. An exception to this is when channels are concatenated. Refer to Section 12.4.2.7, "PWM 16-Bit Functions," for more detail.

NOTE

The first PWM cycle after enabling the channel can be irregular.

On the front end of the PWM timer, the clock is enabled to the PWM circuit by the PWMEx bit being high. There is an edge-synchronizing circuit to guarantee that the clock will only be enabled or disabled at an edge. When the channel is disabled (PWMEx = 0), the counter for the channel does not count.

12.4.2.2 PWM Polarity

Each channel has a polarity bit to allow starting a waveform cycle with a high or low signal. This is shown on the block diagram as a mux select of either the Q output or the $\overline{Q}$ output of the PWM output flip-flop. When one of the bits in the PWMPOL register is set, the associated PWM channel output is high at the beginning of the waveform, then goes low when the duty count is reached. Conversely, if the polarity bit is 0, the output starts low and then goes high when the duty count is reached.

12.4.2.3 PWM Period and Duty

Dedicated period and duty registers exist for each channel and are double buffered so that if they change while the channel is enabled, the change will NOT take effect until one of the following occurs:

- The effective period ends
- The counter is written (counter resets to 0x0000)
- The channel is disabled

In this way, the output of the PWM will always be either the old waveform or the new waveform, not some variation in between. If the channel is not enabled, then writes to the period and duty registers will go directly to the latches as well as the buffer.

A change in duty or period can be forced into effect "immediately" by writing the new value to the duty and/or period registers and then writing to the counter. This forces the counter to reset and the new duty and/or period values to be latched. In addition, because the counter is readable it is possible to know where the count is with respect to the duty value and software can be used to make adjustments.

NOTE

When forcing a new period or duty into effect immediately, an irregular PWM cycle can occur.

Depending on the polarity bit, the duty registers will contain the count of either the high time or the low time.

15.1.2 Modes of Operation

Stop: Timer is off because clocks are stopped.

Freeze: Timer counter keep on running, unless TSFRZ in TSCR (0x0006) is set to 1.

Wait: Counters keep on running, unless TSWAI in TSCR (0x0006) is set to 1.

Normal: Timer counter keep on running, unless TEN in TSCR (0x0006) is cleared to 0.

15.1.3 Block Diagrams

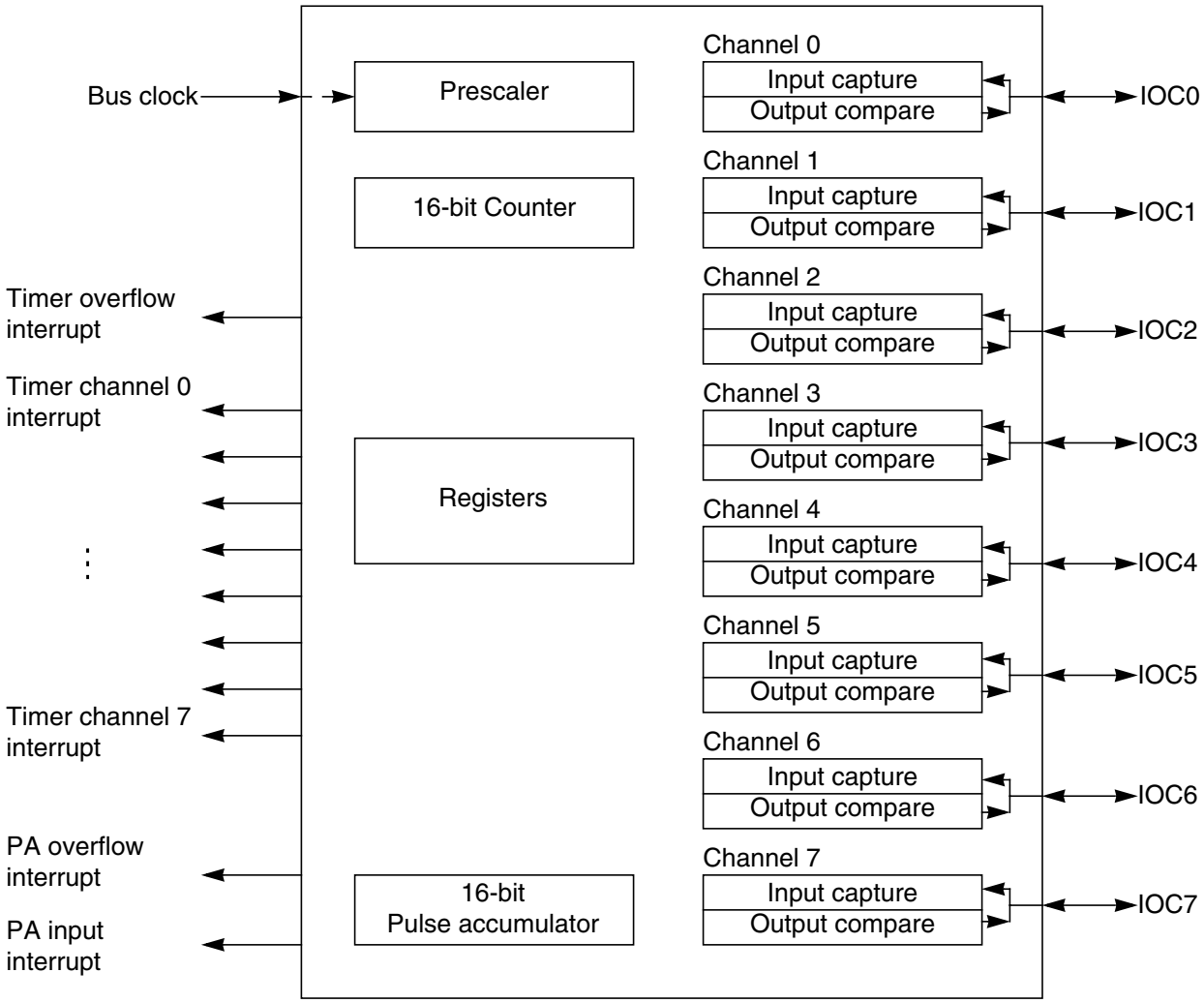

Figure 15-1. TIM16B8CV1 Block Diagram

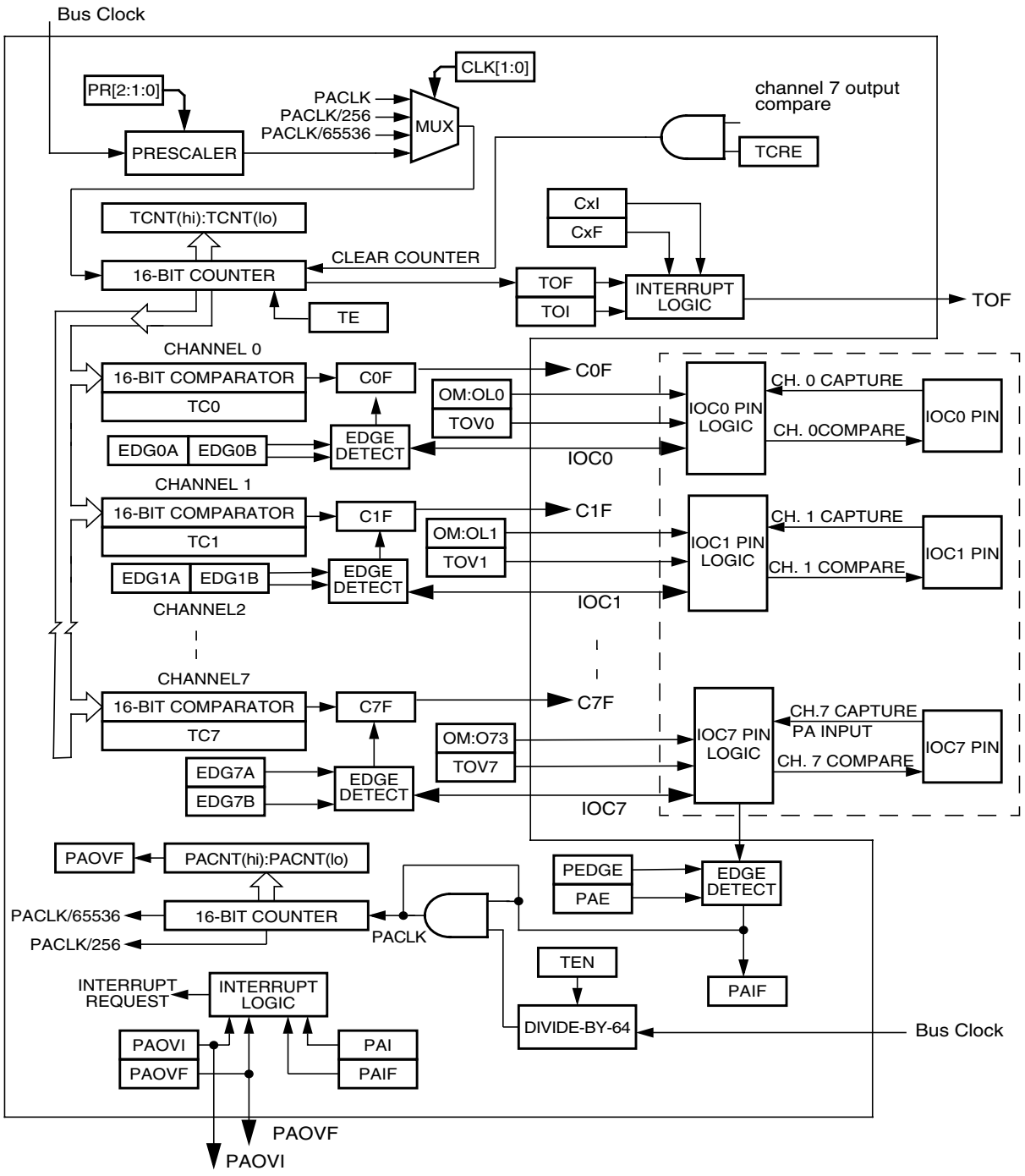

Figure 15-28. Detailed Timer Block Diagram

15.4.1 Prescaler

The prescaler divides the bus clock by 1,2,4,8,16,32,64 or 128. The prescaler select bits, PR[2:0], select the prescaler divisor. PR[2:0] are in timer system control register 2 (TSCR2).

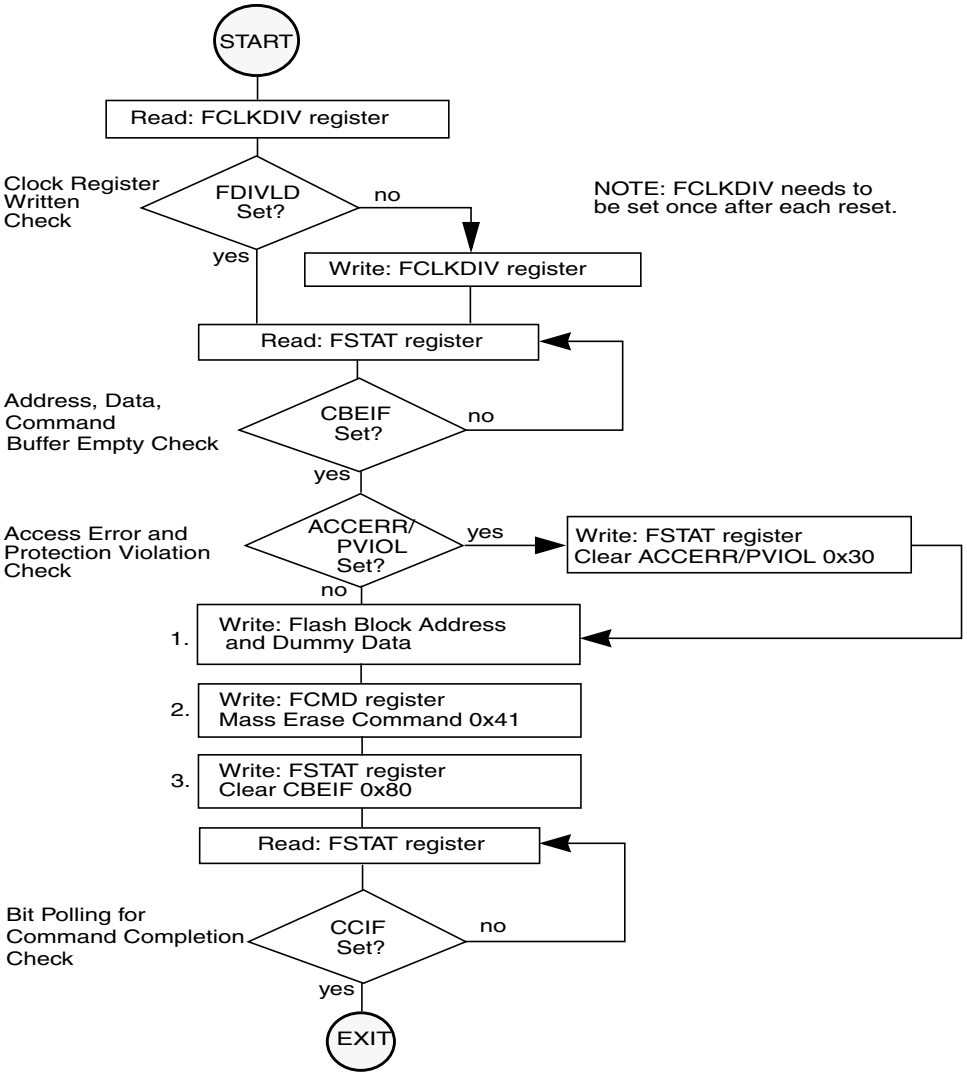

Figure 17-25. Example Mass Erase Command Flow

17.4.4 Flash Reset Sequence

On each reset, the Flash module executes a reset sequence to hold CPU activity while loading the following registers from the Flash array memory according to Table 17-1:

- FPROT — Flash Protection Register (see Section 17.3.2.5)
- FSEC — Flash Security Register (see Section 17.3.2.2)

17.4.4.1 Reset While Flash Command Active

If a reset occurs while any Flash command is in progress, that command will be immediately aborted. The state of the word being programmed or the sector/array being erased is not guaranteed.

17.4.5 Interrupts

The Flash module can generate an interrupt when all Flash commands have completed execution or the Flash address, data, and command buffers are empty.

Table 17-16. Flash Interrupt Sources

Interrupt Source	Interrupt Flag	Local Enable	Global (CCR) Mask
Flash Address, Data, and Command Buffers are empty	CBEIF (FSTAT register)	CBEIE	I Bit
All Flash commands have completed execution	CCIF (FSTAT register)	CCIE	I Bit

NOTE

Vector addresses and their relative interrupt priority are determined at the MCU level.

17.4.5.1 Description of Interrupt Operation

Figure 17-26 shows the logic used for generating interrupts.

The Flash module uses the CBEIF and CCIF flags in combination with the enable bits CBIE and CCIE to discriminate for the generation of interrupts.

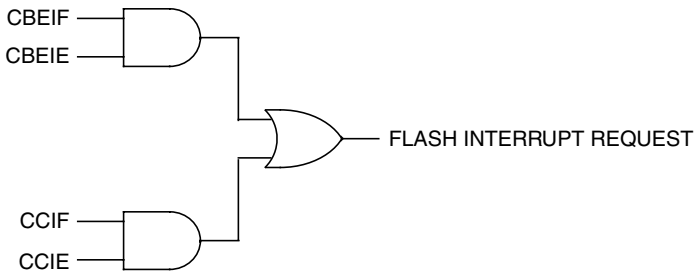

Figure 17-26. Flash Interrupt Implementation

For a detailed description of these register bits, refer to Section 17.3.2.4, “Flash Configuration Register (FCNFG)” and Section 17.3.2.6, “Flash Status Register (FSTAT)”.

20.3.2 Register Descriptions

The Flash module contains a set of 16 control and status registers located between module base + 0x0000 and 0x000F. A summary of the Flash module registers is given in Figure 20-5. Detailed descriptions of each register bit are provided.

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000 FCLKDIV	R	FDIVLD	PRDIV8	FDIV5	FDIV4	FDIV3	FDIV2	FDIV1	FDIV0
	W								
0x0001 FSEC	R	KEYEN1	KEYEN0	NV5	NV4	NV3	NV2	SEC1	SEC0
	W								
0x0002 RESERVED1 (1)	R	0	0	0	0	0	0	0	0
	W								
0x0003 FCNFG	R	CBEIE	CCIE	KEYACC	0	0	0	0	0
	W								
0x0004 FPROT	R	FPOPEN	NV6	FPHDIS	FPHS1	FPHS0	FPLDIS	FPLS1	FPLS0
	W								
0x0005 FSTAT	R	CBEIF	CCIF	PVIOL	ACCERR	0	BLANK	FAIL	DONE
	W								
0x0006 FCMD	R	0	CMDB6	CMDB5	0	0	CMDB2	0	CMDB0
	W								
0x0007 RESERVED2[1]	R	0	0	0	0	0	0	0	0
	W								
0x0008 FADDRHI[1]	R	FABHI							
	W								
0x0009 FADDRLO[1]	R	FABLO							
	W								
0x000A FDATAHI[1]	R	FDHI							
	W								
0x000B FDATALO[1]	R	FDLO							
	W								
0x000C RESERVED3[1]	R	0	0	0	0	0	0	0	0
	W								
0x000D RESERVED4[1]	R	0	0	0	0	0	0	0	0
	W								
0x000E RESERVED5[1]	R	0	0	0	0	0	0	0	0
	W								
0x000F RESERVED6[1]	R	0	0	0	0	0	0	0	0
	W								

= Unimplemented or Reserved

Figure 20-5. Flash Register Summary

1. Intended for factory test purposes only.

Module Base + 0x000C

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 20-19. RESERVED3

All bits read 0 and are not writable.

20.3.2.12 RESERVED4

This register is reserved for factory testing and is not accessible to the user.

Module Base + 0x000D

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 20-20. RESERVED4

All bits read 0 and are not writable.

20.3.2.13 RESERVED5

This register is reserved for factory testing and is not accessible to the user.

Module Base + 0x000E

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 20-21. RESERVED5

All bits read 0 and are not writable.

20.3.2.14 RESERVED6

This register is reserved for factory testing and is not accessible to the user.

20.4.4 Flash Reset Sequence

On each reset, the Flash module executes a reset sequence to hold CPU activity while loading the following registers from the Flash array memory according to Table 20-1:

- FPROT — Flash Protection Register (see Section 20.3.2.5)
- FSEC — Flash Security Register (see Section 20.3.2.2)

20.4.4.1 Reset While Flash Command Active

If a reset occurs while any Flash command is in progress, that command will be immediately aborted. The state of the word being programmed or the sector/array being erased is not guaranteed.

20.4.5 Interrupts

The Flash module can generate an interrupt when all Flash commands have completed execution or the Flash address, data, and command buffers are empty.

Table 20-18. Flash Interrupt Sources

Interrupt Source	Interrupt Flag	Local Enable	Global (CCR) Mask
Flash Address, Data, and Command Buffers are empty	CBEIF (FSTAT register)	CBEIE	I Bit
All Flash commands have completed execution	CCIF (FSTAT register)	CCIE	I Bit

NOTE

Vector addresses and their relative interrupt priority are determined at the MCU level.

20.4.5.1 Description of Interrupt Operation

Figure 20-28 shows the logic used for generating interrupts.

The Flash module uses the CBEIF and CCIF flags in combination with the enable bits CBIE and CCIE to discriminate for the generation of interrupts.

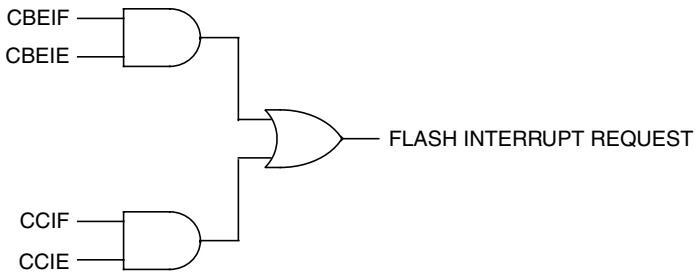

Figure 20-28. Flash Interrupt Implementation

For a detailed description of these register bits, refer to Section 20.3.2.4, “Flash Configuration Register (FCNFG)” and Section 20.3.2.6, “Flash Status Register (FSTAT)”.

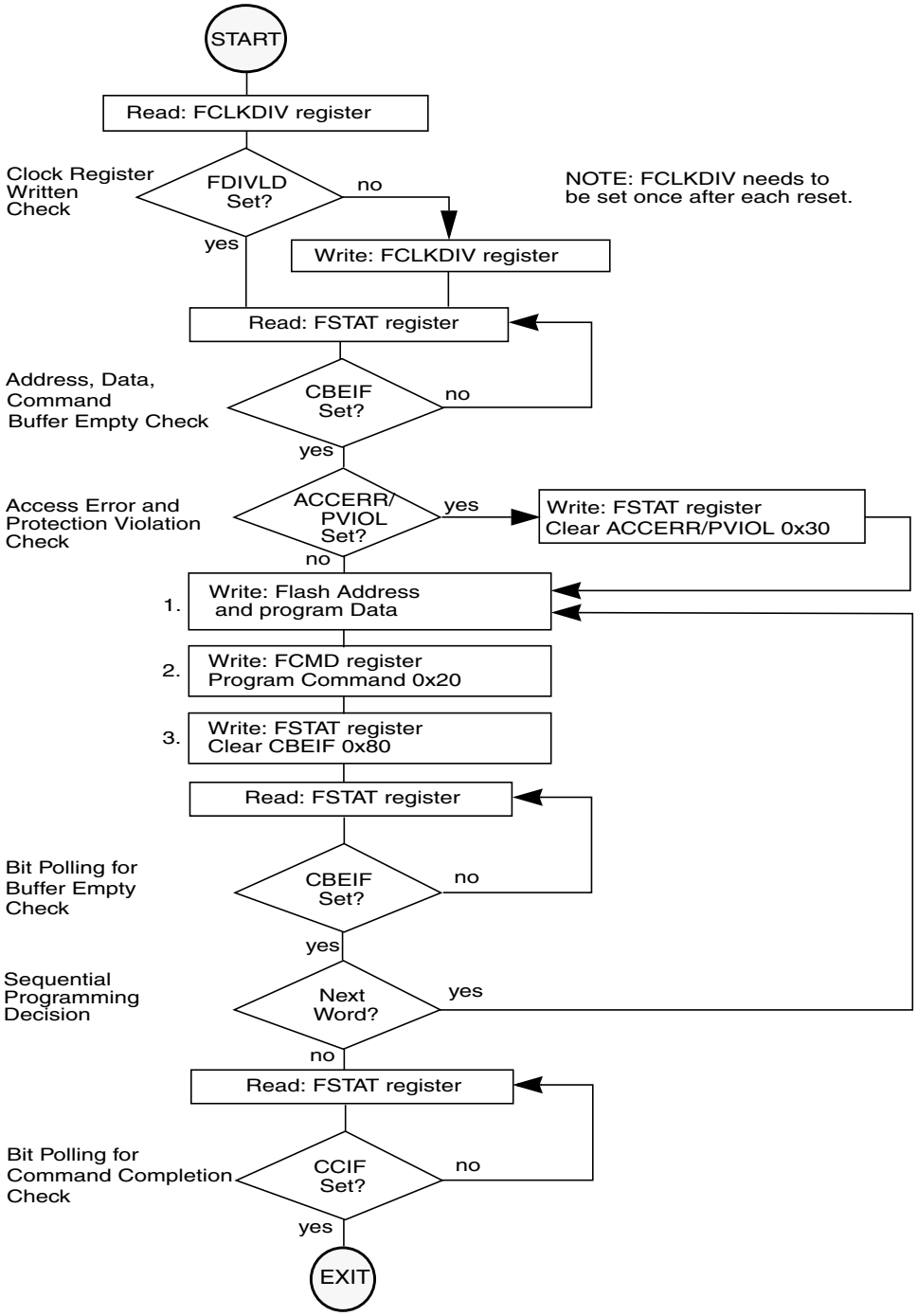

Figure 21-23. Example Program Command Flow

A.5.2 NVM Reliability

The reliability of the NVM blocks is guaranteed by stress test during qualification, constant process monitors and burn-in to screen early life failures. The program/erase cycle count on the sector is incremented every time a sector or mass erase event is executed.

Table A-19. NVM Reliability Characteristics[1]

Conditions are shown in Table A-4. unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Flash Reliability Characteristics							
1	C	Data retention after 10,000 program/erase cycles at an average junction temperature of $T_{Javg} \leq 85°C$	t_{FLRET}	15	100[2]	—	Years
2	C	Data retention with <100 program/erase cycles at an average junction temperature $T_{Javg} \leq 85°C$		20	100[2]	—	
3	C	Number of program/erase cycles ($-40°C \leq T_J \leq 0°C$)	n_{FL}	10,000	—	—	Cycles
4	C	Number of program/erase cycles ($0°C \leq T_J \leq 140°C$)		10,000	100,000[3]	—	

1. T_{Javg} will not exeed 85°C considering a typical temperature profile over the lifetime of a consumer, industrial or automotive application.
2. Typical data retention values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale defines Typical Data Retention, please refer to Engineering Bulletin EB618.
3. Spec table quotes typical endurance evaluated at 25°C for this product family, typical endurance at various temperature can be estimated using the graph below. For additional information on how Freescale defines Typical Endurance, please refer to Engineering Bulletin EB619.

Part Number	Mask[1] set	Temp.	Package	Speed	Die Type	Flash	RAM	I/O[2], [3]
MC9S12C64CFU	XL09S/0M66G	-40˚C, 85˚C	80QFP	25MHz	C128 die	64K	4K	60
MC9S12C64VFA	XL09S/0M66G	-40˚C,105˚C	48LQFP	25MHz	C128 die	64K	4K	31
MC9S12C64VPB	XL09S/0M66G	-40˚C,105˚C	52LQFP	25MHz	C128 die	64K	4K	35
MC9S12C64VFU	XL09S/0M66G	-40˚C, 105˚C	80QFP	25MHz	C128 die	64K	4K	60
MC9S12C64MFA	XL09S/0M66G	-40˚C,125˚C	48LQFP	25MHz	C128 die	64K	4K	31
MC9S12C64MPB	XL09S/0M66G	-40˚C,125˚C	52LQFP	25MHz	C128 die	64K	4K	35
MC9S12C64MFU	XL09S/0M66G	-40˚C, 125˚C	80QFP	25MHz	C128 die	64K	4K	60
MC9S12C32CFA16	xL45J / xM34C	-40˚C, 85˚C	48LQFP	16MHz	C32 die	32K	2K	31
MC9S12C32CPB16	xL45J / xM34C	-40˚C, 85˚C	52LQFP	16MHz	C32 die	32K	2K	35
MC9S12C32CFU16	xL45J / xM34C	-40˚C, 85˚C	80QFP	16MHz	C32 die	32K	2K	60
MC9S12C32VFA16	xL45J / xM34C	-40˚C,105˚C	48LQFP	16MHz	C32 die	32K	2K	31
MC9S12C32VPB16	xL45J / xM34C	-40˚C,105˚C	52LQFP	16MHz	C32 die	32K	2K	35
MC9S12C32VFU16	xL45J / xM34C	-40˚C, 105˚C	80QFP	16MHz	C32 die	32K	2K	60
MC9S12C32MFA16	xL45J / xM34C	-40˚C,125˚C	48LQFP	16MHz	C32 die	32K	2K	31
MC9S12C32MPB16	xL45J / xM34C	-40˚C,125˚C	52LQFP	16MHz	C32 die	32K	2K	35
MC9S12C32MFU16	xL45J / xM34C	-40˚C, 125˚C	80QFP	16MHz	C32 die	32K	2K	60
MC9S12C32CFA25	xL45J / xM34C	-40˚C, 85˚C	48LQFP	25MHz	C32 die	32K	2K	31
MC9S12C32CPB25	xL45J / xM34C	-40˚C, 85˚C	52LQFP	25MHz	C32 die	32K	2K	35
MC9S12C32CFU25	xL45J / xM34C	-40˚C, 85˚C	80QFP	25MHz	C32 die	32K	2K	60
MC9S12C32VFA25	xL45J / xM34C	-40˚C,105˚C	48LQFP	25MHz	C32 die	32K	2K	31
MC9S12C32VPB25	xL45J / xM34C	-40˚C,105˚C	52LQFP	25MHz	C32 die	32K	2K	35
MC9S12C32VFU25	xL45J / xM34C	-40˚C, 105˚C	80QFP	25MHz	C32 die	32K	2K	60
MC9S12C32MFA25	xL45J / xM34C	-40˚C,125˚C	48LQFP	25MHz	C32 die	32K	2K	31
MC9S12C32MPB25	xL45J / xM34C	-40˚C,125˚C	52LQFP	25MHz	C32 die	32K	2K	35
MC9S12C32MFU25	xL45J / xM34C	-40˚C, 125˚C	80QFP	25MHz	C32 die	32K	2K	60

1. XL09S denotes all minor revisions of L09S maskset
   XL45J denotes all minor revisions of L45J maskset
   Maskset dependent errata can be accessed at
   http://e-www.motorola.com/wbapp/sps/site/prod_summary.jsp
2. All C-Family derivatives feature 1 CAN, 1 SCI, 1 SPI, an 8-channel A/D, a 6-channel PWM and an 8 channel timer. The GC-Family members do not have the CAN module
3. I/O is the sum of ports able to act as digital input or output.

Table E-2. MC9S12GC-Family Part Number Coding

Part Number	Mask[1] set	Temp.	Package	Speed	Die Type	Flash	RAM	I/O[2], [3]
MC9S12GC32CFA	xL45J / xM34C	-40˚C, 85˚C	48LQFP	25MHz	C32 die	32K	2K	31
MC9S12GC32CPB	xL45J / xM34C	-40˚C, 85˚C	52LQFP	25MHz	C32 die	32K	2K	35
MC9S12GC32CFU	xL45J / xM34C	-40˚C, 85˚C	80QFP	25MHz	C32 die	32K	2K	60
MC9S12GC32VFA	xL45J / xM34C	-40˚C,105˚C	48LQFP	25MHz	C32 die	32K	2K	31
MC9S12GC32VPB	xL45J / xM34C	-40˚C,105˚C	52LQFP	25MHz	C32 die	32K	2K	35
MC9S12GC32VFU	xL45J / xM34C	-40˚C, 105˚C	80QFP	25MHz	C32 die	32K	2K	60
MC9S12GC32MFA	xL45J / xM34C	-40˚C,125˚C	48LQFP	25MHz	C32 die	32K	2K	31
MC9S12GC32MPB	xL45J / xM34C	-40˚C,125˚C	52LQFP	25MHz	C32 die	32K	2K	35