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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	HCS12
Core Size	16-Bit
Speed	25MHz
Connectivity	EBI/EMI, SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	60
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-QFP
Supplier Device Package	80-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s12gc32cfue

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0048	TCTL1	Read: Write:	OM7	OL7	OM6	OL6	OM5	OL5	OM4	OL4
0x0049	TCTL2	Read: Write:	OM3	OL3	OM2	OL2	OM1	OL1	OM0	OL0
0x004A	TCTL3	Read: Write:	EDG7B	EDG7A	EDG6B	EDG6A	EDG5B	EDG5A	EDG4B	EDG4A
0x004B	TCTL4	Read: Write:	EDG3B	EDG3A	EDG2B	EDG2A	EDG1B	EDG1A	EDG0B	EDG0A
0x004C	TIE	Read: Write:	C7I	C6I	C5I	C4I	C3I	C2I	C1I	C0I
0x004D	TSCR2	Read: Write:	TOI	0	0	0	TCRE	PR2	PR1	PR0
0x004E	TFLG1	Read: Write:	C7F	C6F	C5F	C4F	C3F	C2F	C1F	C0F
0x004F	TFLG2	Read: Write:	TOF	0	0	0	0	0	0	0
0x0050	TC0 (hi)	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
0x0051	TC0 (lo)	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
0x0052	TC1 (hi)	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
0x0053	TC1 (lo)	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
0x0054	TC2 (hi)	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
0x0055	TC2 (lo)	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
0x0056	TC3 (hi)	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
0x0057	TC3 (lo)	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
0x0058	TC4 (hi)	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
0x0059	TC4 (lo)	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
0x005A	TC5 (hi)	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
0x005B	TC5 (lo)	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
0x005C	TC6 (hi)	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
0x005D	TC6 (lo)	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
0x005E	TC7 (hi)	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8

0x00E0–0x00FF PWM (Pulse Width Modulator)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00E0	PWME	Read:	0	0	PWME5	PWME4	PWME3	PWME2	PWME1	PWME0
		Write:								
$00E1	PWMPOL	Read:	0	0	PPOL5	PPOL4	PPOL3	PPOL2	PPOL1	PPOL0
		Write:								
$00E2	PWMCLK	Read:	0	0	PCLK5	PCLK4	PCLK3	PCLK2	PCLK1	PCLK0
		Write:								
$00E3	PWMPRCLK	Read:	0	PCKB2	PCKB1	PCKB0	0	PCKA2	PCKA1	PCKA0
		Write:								
$00E4	PWMCAE	Read:	0	0	CAE5	CAE4	CAE3	CAE2	CAE1	CAE0
		Write:								
$00E5	PWMCTL	Read:	0	CON45	CON23	CON01	PSWAI	PFRZ	0	0
		Write:								
$00E6	PWMTST Test Only	Read:	0	0	0	0	0	0	0	0
		Write:								
$00E7	PWMPRSC	Read:	0	0	0	0	0	0	0	0
		Write:								
$00E8	PWMSCLA	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$00E9	PWMSCLB	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$00EA	PWMSCNTA	Read:	0	0	0	0	0	0	0	0
		Write:								
$00EB	PWMSCNTB	Read:	0	0	0	0	0	0	0	0
		Write:								
$00EC	PWMCNT0	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:	0	0	0	0	0	0	0	0
$00ED	PWMCNT1	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:	0	0	0	0	0	0	0	0
$00EE	PWMCNT2	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:	0	0	0	0	0	0	0	0
$00EF	PWMCNT3	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:	0	0	0	0	0	0	0	0
$00F0	PWMCNT4	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:	0	0	0	0	0	0	0	0
$00F1	PWMCNT5	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:	0	0	0	0	0	0	0	0
$00F2	PWMPER0	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$00F3	PWMPER1	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$00F4	PWMPER2	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$00F5	PWMPER3	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								

1.3.4.27 PS[3:2] — Port S I/O Pins [3:2]

PS3 and PS2 are general purpose input or output pins. These pins are not available in the 48- / 52-pin package versions.

1.3.4.28 PS1 / TXD — Port S I/O Pin 1

PS1 is a general purpose input or output pin and the transmit pin, TXD, of serial communication interface (SCI).

1.3.4.29 PS0 / RXD — Port S I/O Pin 0

PS0 is a general purpose input or output pin and the receive pin, RXD, of serial communication interface (SCI).

1.3.4.30 PT[7:5] / IOC[7:5] — Port T I/O Pins [7:5]

PT7–PT5 are general purpose input or output pins. They can also be configured as the timer system input capture or output compare pins IOC7-IOC5.

1.3.4.31 PT[4:0] / IOC[4:0] / PW[4:0]— Port T I/O Pins [4:0]

PT4–PT0 are general purpose input or output pins. They can also be configured as the timer system input capture or output compare pins IOC[n] or as the PWM outputs PW[n].

1.3.5 Power Supply Pins

1.3.5.1 V_{DDX},V_{SSX} — Power and Ground Pins for I/O Drivers

External power and ground for I/O drivers. Bypass requirements depend on how heavily the MCU pins are loaded.

1.3.5.2 V_{DDR}, V_{SSR} — Power and Ground Pins for I/O Drivers and for Internal Voltage Regulator

External power and ground for the internal voltage regulator. Connecting V_{DDR} to ground disables the internal voltage regulator.

1.3.5.3 V_{DD1}, V_{DD2}, V_{SS1}, V_{SS2} — Internal Logic Power Pins

Power is supplied to the MCU through V_{DD} and V_{SS}. This 2.5V supply is derived from the internal voltage regulator. There is no static load on those pins allowed. The internal voltage regulator is turned off, if V_{DDR} is tied to ground.

Chapter 2
Port Integration Module (PIM9C32) Block Description

2.1 Introduction

The Port Integration Module establishes the interface between the peripheral modules and the I/O pins for all ports.

This chapter covers:

- Port A, B, and E related to the core logic and the multiplexed bus interface
- Port T connected to the TIM module (PWM module can be routed to port T as well)
- Port S connected to the SCI module
- Port M associated to the MSCAN and SPI module
- Port P connected to the PWM module, external interrupt sources available
- Port J pins can be used as external interrupt sources and standard I/O's

The following I/O pin configurations can be selected:

- Available on all I/O pins:
  - Input/output selection
  - Drive strength reduction
  - Enable and select of pull resistors
- Available on all Port P and Port J pins:
  - Interrupt enable and status flags

The implementation of the Port Integration Module is device dependent.

2.1.1 Features

A standard port has the following minimum features:

- Input/output selection
- 5-V output drive with two selectable drive strength
- 5-V digital and analog input
- Input with selectable pull-up or pull-down device

Optional features:

- Open drain for wired-OR connections
- Interrupt inputs with glitch filtering

2.4.2.5 Port P

The PWM module is connected to port P. Port P pins can be used as PWM outputs. Further the Keypad Wake-Up function is implemented on pins PP[7:0]. During reset, port P pins are configured as high-impedance inputs.

Port P offers 8 general purpose I/O pins with edge triggered interrupt capability in wired-or fashion. The interrupt enable as well as the sensitivity to rising or falling edges can be individually configured on per pin basis. All 8 bits/pins share the same interrupt vector. Interrupts can be used with the pins configured as inputs or outputs.

An interrupt is generated when a bit in the port interrupt flag register and its corresponding port interrupt enable bit are both set. This external interrupt feature is capable to wake up the CPU when it is in STOP or WAIT mode.

A digital filter on each pin prevents pulses (Figure 2-48) shorter than a specified time from generating an interrupt. The minimum time varies over process conditions, temperature and voltage (Figure 2-47 and Table 2-38).

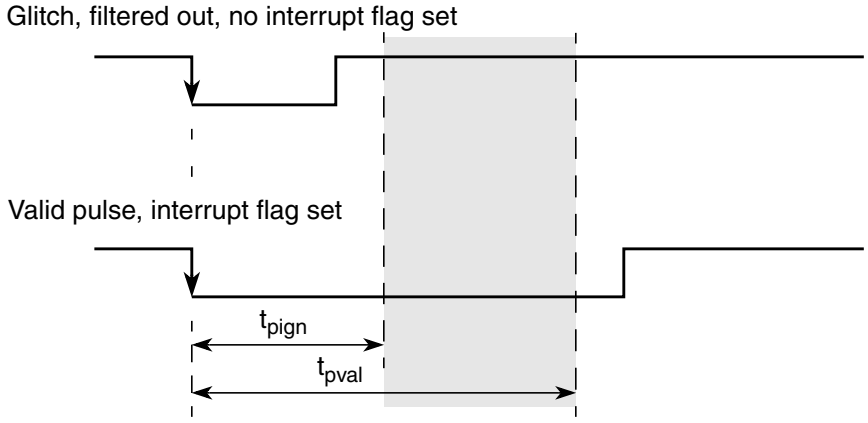


Figure 2-47. Interrupt Glitch Filter on Port P and J (PPS = 0)

Table 2-38. Pulse Detection Criteria

Pulse	$\overline{\text{STOP}}$ Mode		STOP(1) Mode	
	Value	Unit	Value	Unit
Ignored	t_{pign} <= 3	Bus clocks	t_{pign} <= 3.2	µs
Uncertain	3 < t_{pulse} < 4	Bus clocks	3.2 < t_{pulse} < 10	µs
Valid	t_{pval} >= 4	Bus clocks	t_{pval} >= 10	µs

1. These values include the spread of the oscillator frequency over temperature, voltage and process.

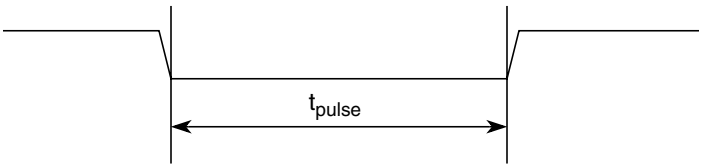


Figure 2-48. Pulse Illustration

Table 3-20. 48K Byte Physical FLASH/ROM Allocated

Address Space	Page Window Access	ROMHM	ECS	XAB19:14
0x0000–0x3FFF	N/A	N/A	1	0x3D
0x4000–0x7FFF	N/A	0	0	0x3E
	N/A	1	1	
0x8000–0xBFFF	External	N/A	1	PIX[5:0]
	Internal	N/A	0	
0xC000–0xFFFF	N/A	N/A	0	0x3F

Table 3-21. 64K Byte Physical FLASH/ROM Allocated

Address Space	Page Window Access	ROMHM	ECS	XAB19:14
0x0000–0x3FFF	N/A	0	0	0x3D
	N/A	1	1	
0x4000–0x7FFF	N/A	0	0	0x3E
	N/A	1	1	
0x8000–0xBFFF	External	N/A	1	PIX[5:0]
	Internal	N/A	0	
0xC000–0xFFFF	N/A	N/A	0	0x3F

A graphical example of a memory paging for a system configured as 1M byte on-chip FLASH/ROM with 64K allocated physical space is given in Figure 3-12.

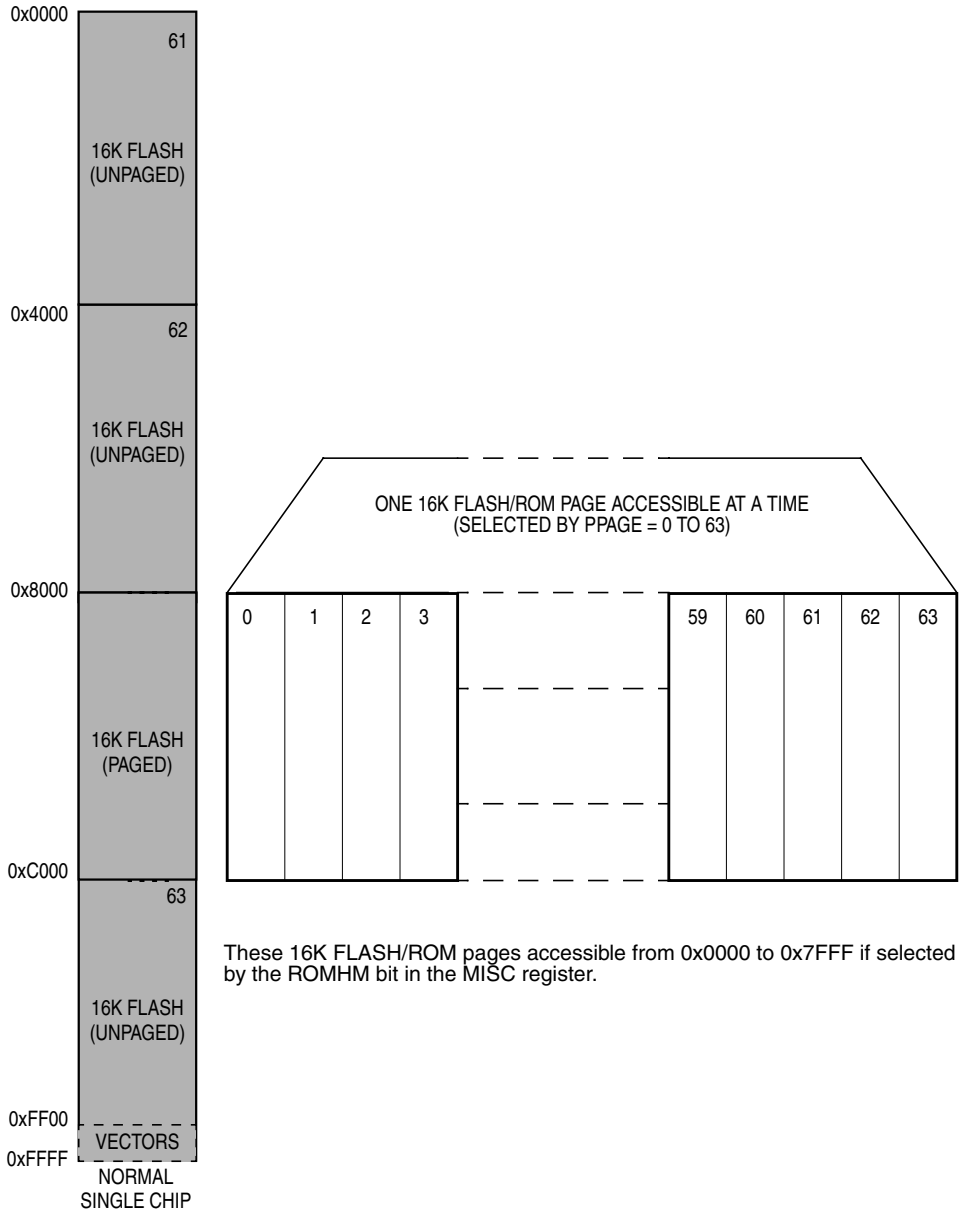


Figure 3-12. Memory Paging Example: 1M Byte On-Chip FLASH/ROM, 64K Allocation

4.3.2.3 Data Direction Register A (DDRA)

Module Base + 0x0002
Starting address location affected by INITRG register setting.

	7	6	5	4	3	2	1	0
R W	Bit 7	6	5	4	3	2	1	Bit 0
Reset	0	0	0	0	0	0	0	0

Figure 4-4. Data Direction Register A (DDRA)

Read: Anytime when register is in the map

Write: Anytime when register is in the map

This register controls the data direction for port A. When port A is operating as a general-purpose I/O port, DDRA determines the primary direction for each port A pin. A 1 causes the associated port pin to be an output and a 0 causes the associated pin to be a high-impedance input. The value in a DDR bit also affects the source of data for reads of the corresponding PORTA register. If the DDR bit is 0 (input) the buffered pin input state is read. If the DDR bit is 1 (output) the associated port data register bit state is read.

This register is not in the on-chip memory map in expanded and special peripheral modes. Therefore, these accesses will be echoed externally. It is reset to 0x00 so the DDR does not override the three-state control signals.

Table 4-3. DDRA Field Descriptions

Field	Description
7:0 DDRA	**Data Direction Port A** 0 Configure the corresponding I/O pin as an input 1 Configure the corresponding I/O pin as an output

8.2 Signal Description

The ATD10B8C has a total of 12 external pins.

8.2.1 AN7 / ETRIG / PAD7

This pin serves as the analog input channel 7. It can be configured to provide an external trigger for the ATD conversion. It can be configured as general-purpose digital I/O.

8.2.2 AN6 / PAD6

This pin serves as the analog input channel 6. It can be configured as general-purpose digital I/O.

8.2.3 AN5 / PAD5

This pin serves as the analog input channel 5. It can be configured as general-purpose digital I/O.

8.2.4 AN4 / PAD4

This pin serves as the analog input channel 4. It can be configured as general-purpose digital I/O.

8.2.5 AN3 / PAD3

This pin serves as the analog input channel 3. It can be configured as general-purpose digital I/O.

8.2.6 AN2 / PAD2

This pin serves as the analog input channel 2. It can be configured as general-purpose digital I/O.

8.2.7 AN1 / PAD1

This pin serves as the analog input channel 1. It can be configured as general-purpose digital I/O.

8.2.8 AN0 / PAD0

This pin serves as the analog input channel 0. It can be configured as general-purpose digital I/O.

8.2.9 V_{RH}, V_{RL}

V_{RH} is the high reference voltage and V_{RL} is the low reference voltage for ATD conversion.

8.2.10 V_{DDA}, V_{SSA}

These pins are the power supplies for the analog circuitry of the ATD10B8C block.

Read: Anytime when TXEx flag is set (see Section 10.3.2.7, "MSCAN Transmitter Flag Register (CANTFLG)") and the corresponding transmit buffer is selected in CANTBSEL (see Section 10.3.2.11, "MSCAN Transmit Buffer Selection Register (CANTBSEL)").

Write: Unimplemented

10.4 Functional Description

10.4.1 General

This section provides a complete functional description of the MSCAN. It describes each of the features and modes listed in the introduction.

10.4.4.3 Emulation Modes

In all emulation modes, the MSCAN module behaves just like normal system operation modes as described within this specification.

10.4.4.4 Listen-Only Mode

In an optional CAN bus monitoring mode (listen-only), the CAN node is able to receive valid data frames and valid remote frames, but it sends only "recessive" bits on the CAN bus. In addition, it cannot start a transmision. If the MAC sub-layer is required to send a "dominant" bit (ACK bit, overload flag, or active error flag), the bit is rerouted internally so that the MAC sub-layer monitors this "dominant" bit, although the CAN bus may remain in recessive state externally.

10.4.4.5 Security Modes

The MSCAN module has no security features.

10.4.5 Low-Power Options

If the MSCAN is disabled (CANE = 0), the MSCAN clocks are stopped for power saving.

If the MSCAN is enabled (CANE = 1), the MSCAN has two additional modes with reduced power consumption, compared to normal mode: sleep and power down mode. In sleep mode, power consumption is reduced by stopping all clocks except those to access the registers from the CPU side. In power down mode, all clocks are stopped and no power is consumed.

Table 10-35 summarizes the combinations of MSCAN and CPU modes. A particular combination of modes is entered by the given settings on the CSWAI and SLPRQ/SLPAK bits.

For all modes, an MSCAN wake-up interrupt can occur only if the MSCAN is in sleep mode (SLPRQ = 1 and SLPAK = 1), wake-up functionality is enabled (WUPE = 1), and the wake-up interrupt is enabled (WUPIE = 1).

10.4.5.5 MSCAN Initialization Mode

In initialization mode, any on-going transmission or reception is immediately aborted and synchronization to the CAN bus is lost, potentially causing CAN protocol violations. To protect the CAN bus system from fatal consequences of violations, the MSCAN immediately drives the TXCAN pin into a recessive state.

NOTE

The user is responsible for ensuring that the MSCAN is not active when initialization mode is entered. The recommended procedure is to bring the MSCAN into sleep mode (SLPRQ = 1 and SLPAK = 1) before setting the INITRQ bit in the CANCTL0 register. Otherwise, the abort of an on-going message can cause an error condition and can impact other CAN bus devices.

In initialization mode, the MSCAN is stopped. However, interface registers remain accessible. This mode is used to reset the CANCTL0, CANRFLG, CANRIER, CANTFLG, CANTIER, CANTARQ, CANTAAK, and CANTBSEL registers to their default values. In addition, the MSCAN enables the configuration of the CANBTR0, CANBTR1 bit timing registers; CANIDAC; and the CANIDAR, CANIDMR message filters. See Section 10.3.2.1, "MSCAN Control Register 0 (CANCTL0)," for a detailed description of the initialization mode.

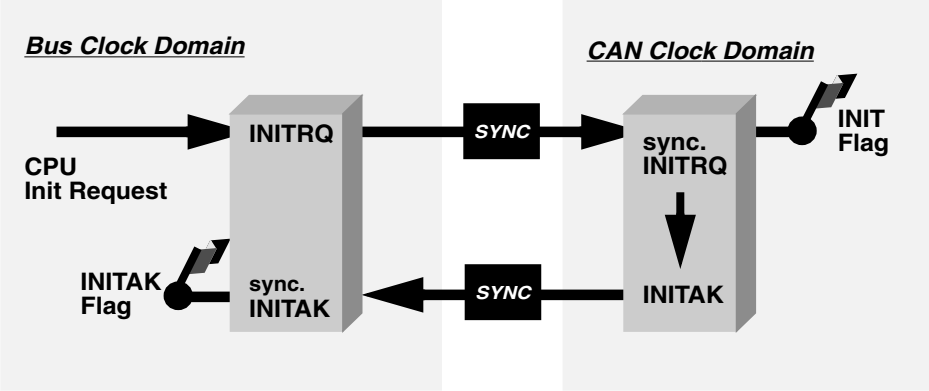


Figure 10-46. Initialization Request/Acknowledge Cycle

Due to independent clock domains within the MSCAN, INITRQ must be synchronized to all domains by using a special handshake mechanism. This handshake causes additional synchronization delay (see Section Figure 10-46., "Initialization Request/Acknowledge Cycle").

If there is no message transfer ongoing on the CAN bus, the minimum delay will be two additional bus clocks and three additional CAN clocks. When all parts of the MSCAN are in initialization mode, the INITAK flag is set. The application software must use INITAK as a handshake indication for the request (INITRQ) to go into initialization mode.

NOTE

The CPU cannot clear INITRQ before initialization mode (INITRQ = 1 and INITAK = 1) is active.

Module Base + 0x000E

	7	6	5	4	3	2	1	0
R	Bit 7	6	5	4	3	2	1	Bit 0
W	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0

Figure 12-17. PWM Channel Counter Registers (PWMCNT2)

Module Base + 0x000F

	7	6	5	4	3	2	1	0
R	Bit 7	6	5	4	3	2	1	Bit 0
W	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0

Figure 12-18. PWM Channel Counter Registers (PWMCNT3)

Module Base + 0x00010

	7	6	5	4	3	2	1	0
R	Bit 7	6	5	4	3	2	1	Bit 0
W	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0

Figure 12-19. PWM Channel Counter Registers (PWMCNT4)

Module Base + 0x00011

	7	6	5	4	3	2	1	0
R	Bit 7	6	5	4	3	2	1	Bit 0
W	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0

Figure 12-20. PWM Channel Counter Registers (PWMCNT5)

Read: anytime

Write: anytime (any value written causes PWM counter to be reset to 0x0000).

12.3.2.13 PWM Channel Period Registers (PWMPERx)

There is a dedicated period register for each channel. The value in this register determines the period of the associated PWM channel.

The period registers for each channel are double buffered so that if they change while the channel is enabled, the change will NOT take effect until one of the following occurs:

- The effective period ends
- The counter is written (counter resets to 0x0000)

12.4.2.1 PWM Enable

Each PWM channel has an enable bit (PWMEx) to start its waveform output. When any of the PWMEx bits are set (PWMEx = 1), the associated PWM output signal is enabled immediately. However, the actual PWM waveform is not available on the associated PWM output until its clock source begins its next cycle due to the synchronization of PWMEx and the clock source. An exception to this is when channels are concatenated. Refer to Section 12.4.2.7, "PWM 16-Bit Functions," for more detail.

NOTE

The first PWM cycle after enabling the channel can be irregular.

On the front end of the PWM timer, the clock is enabled to the PWM circuit by the PWMEx bit being high. There is an edge-synchronizing circuit to guarantee that the clock will only be enabled or disabled at an edge. When the channel is disabled (PWMEx = 0), the counter for the channel does not count.

12.4.2.2 PWM Polarity

Each channel has a polarity bit to allow starting a waveform cycle with a high or low signal. This is shown on the block diagram as a mux select of either the Q output or the $\overline{Q}$ output of the PWM output flip-flop. When one of the bits in the PWMPOL register is set, the associated PWM channel output is high at the beginning of the waveform, then goes low when the duty count is reached. Conversely, if the polarity bit is 0, the output starts low and then goes high when the duty count is reached.

12.4.2.3 PWM Period and Duty

Dedicated period and duty registers exist for each channel and are double buffered so that if they change while the channel is enabled, the change will NOT take effect until one of the following occurs:

- The effective period ends
- The counter is written (counter resets to 0x0000)
- The channel is disabled

In this way, the output of the PWM will always be either the old waveform or the new waveform, not some variation in between. If the channel is not enabled, then writes to the period and duty registers will go directly to the latches as well as the buffer.

A change in duty or period can be forced into effect "immediately" by writing the new value to the duty and/or period registers and then writing to the counter. This forces the counter to reset and the new duty and/or period values to be latched. In addition, because the counter is readable it is possible to know where the count is with respect to the duty value and software can be used to make adjustments.

NOTE

When forcing a new period or duty into effect immediately, an irregular PWM cycle can occur.

Depending on the polarity bit, the duty registers will contain the count of either the high time or the low time.

To change the Flash protection that will be loaded on reset, the upper sector of the Flash array must be unprotected, then the Flash protection byte located at Flash address 0xFF0D must be written to.

A protected Flash sector is disabled by FPHDIS while the size of the protected sector is defined by FPHS[1:0] in the FPROT register.

Trying to alter any of the protected areas will result in a protect violation error and the PVIOL flag will be set in the FSTAT register (see Section 17.3.2.6). A mass erase of the whole Flash array is only possible when protection is fully disabled by setting the FPOPEN and FPHDIS bits. An attempt to mass erase a Flash array while protection is enabled will set the PVIOL flag in the FSTAT register.

Table 17-8. FPROT Field Descriptions

Field	Description
7 FPOPEN	**Protection Function for Program or Erase** — The FPOPEN bit is used to either select an address range to be protected using the FPHDIS and FPHS[1:0] bits or to select the same address range to be unprotected as shown in Table 17-9. 0 The FPHDIS bit allows a Flash address range to be unprotected 1 The FPHDIS bit allows a Flash address range to be protected
6 NV6	**Nonvolatile Flag Bit** — The NV6 bit should remain in the erased state for future enhancements.
5 FPHDIS	**Flash Protection Higher Address Range Disable** — The FPHDIS bit determines whether there is a protected/unprotected area in the higher space of the Flash address map. 0 Protection/unprotection enabled 1 Protection/unprotection disabled
4–3 FPHS[1:0]	**Flash Protection Higher Address Size** — The FPHS[1:0] bits determine the size of the protected/unprotected sector as shown in Table 17-10. The FPHS[1:0] bits can only be written to while the FPHDIS bit is set.
2–0 NV[2:0]	**Nonvolatile Flag Bits** — The NV[2:0] bits should remain in the erased state for future enhancements.

Table 17-9. Flash Protection Function

FPOPEN	FPHDIS	FPHS1	FPHS0	Function(1)
1	1	x	x	No protection
1	0	x	x	Protect high range
0	1	x	x	Full Flash array protected
0	0	x	x	Unprotected high range

1. For range sizes refer to Table 17-10.

Table 17-10. Flash Protection Higher Address Range

FPHS[1:0]	Address Range	Range Size
00	0xF800–0xFFFF	2 Kbytes
01	0xF000–0xFFFF	4 Kbytes
10	0xE000–0xFFFF	8 Kbytes
11	0xC000–0xFFFF	16 Kbytes

Table 20-10. Flash Protection Function

FPOPEN	FPHDIS	FPHS[1]	FPHS[0]	FPLDIS	FPLS[1]	FPLS[0]	Function(1)
1	1	x	x	1	x	x	No protection
1	1	x	x	0	x	x	Protect low range
1	0	x	x	1	x	x	Protect high range
1	0	x	x	0	x	x	Protect high and low ranges
0	1	x	x	1	x	x	Full Flash array protected
0	0	x	x	1	x	x	Unprotected high range
0	1	x	x	0	x	x	Unprotected low range
0	0	x	x	0	x	x	Unprotected high and low ranges

1. For range sizes refer to Table 20-11 and Table 20-12 or .

Table 20-11. Flash Protection Higher Address Range

FPHS[1:0]	Address Range	Range Size
00	0xF800–0xFFFF	2 Kbytes
01	0xF000–0xFFFF	4 Kbytes
10	0xE000–0xFFFF	8 Kbytes
11	0xC000–0xFFFF	16 Kbytes

Table 20-12. Flash Protection Lower Address Range

FPLS[1:0]	Address Range	Range Size
00	0x4000–0x43FF	1 Kbyte
01	0x4000–0x47FF	2 Kbytes
10	0x4000–0x4FFF	4 Kbytes
11	0x4000–0x5FFF	8 Kbytes

Figure 20-11 illustrates all possible protection scenarios. Although the protection scheme is loaded from the Flash array after reset, it is allowed to change in normal modes. This protection scheme can be used by applications requiring re-programming in single chip mode while providing as much protection as possible if no re-programming is required.

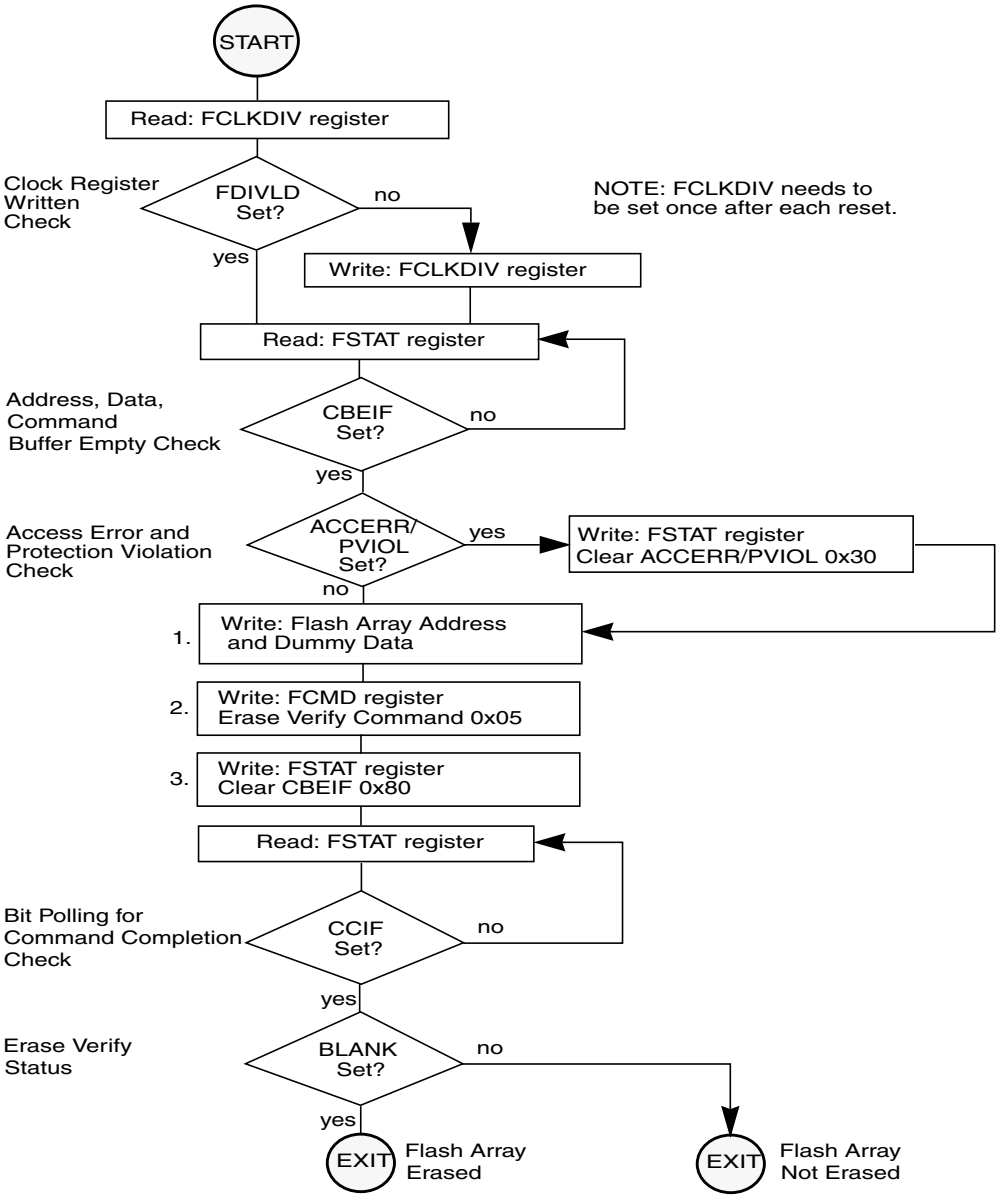


Figure 20-24. Example Erase Verify Command Flow

A.4.1.3 SRAM Data Retention

Provided an appropriate external reset signal is applied to the MCU, preventing the CPU from executing code when V_{DD5} is out of specification limits, the SRAM contents integrity is guaranteed if after the reset the PORF bit in the CRG Flags Register has not been set.

A.4.1.4 External Reset

When external reset is asserted for a time greater than PW_{RSTL} the CRG module generates an internal reset, and the CPU starts fetching the reset vector without doing a clock quality check, if there was an oscillation before reset.

A.4.1.5 Stop Recovery

Out of STOP the controller can be woken up by an external interrupt. A clock quality check as after POR is performed before releasing the clocks to the system.

A.4.1.6 Pseudo Stop and Wait Recovery

The recovery from Pseudo STOP and Wait are essentially the same since the oscillator was not stopped in both modes. In Pseudo Stop Mode the voltage regulator is switched to reduced performance mode to reduce power consumption. The returning out of pseudo stop to full performance takes t_{vup}. The controller can be woken up by internal or external interrupts.After t_{wrs} in Wait or $t_{vup} + t_{wrs}$ in Pseudo Stop the CPU starts fetching the interrupt vector.

A.4.2 Oscillator

The device features an internal Colpitts and Pierce oscillator. The selection of Colpitts oscillator or Pierce oscillator/external clock depends on the XCLKS signal which is sampled during reset. Pierce oscillator/external clock mode allows the input of a square wave. Before asserting the oscillator to the internal system clocks the quality of the oscillation is checked for each start from either power-on, STOP or oscillator fail. t_{CQOUT} specifies the maximum time before switching to the internal self clock mode after POR or STOP if a proper oscillation is not detected. The quality check also determines the minimum oscillator start-up time t_{UPOSC}. The device also features a clock monitor. A Clock Monitor Failure is asserted if the frequency of the incoming clock signal is below the Assert Frequency $f_{CMFA.}$

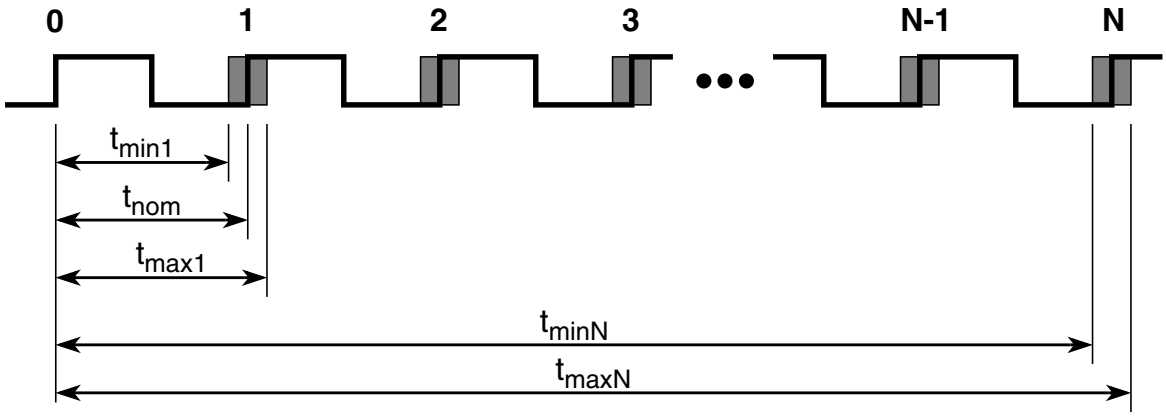


Figure A-3. Jitter Definitions

The relative deviation of t_{nom} is at its maximum for one clock period, and decreases towards zero for larger number of clock periods (N).

Defining the jitter as:

$$J(N) = \max\left(\left|1 - \frac{t_{max}(N)}{N \cdot t_{nom}}\right|, \left|1 - \frac{t_{min}(N)}{N \cdot t_{nom}}\right|\right)$$

For N < 100, the following equation is a good fit for the maximum jitter:

$$J(N) = \frac{j_1}{\sqrt{N}} + j_2$$

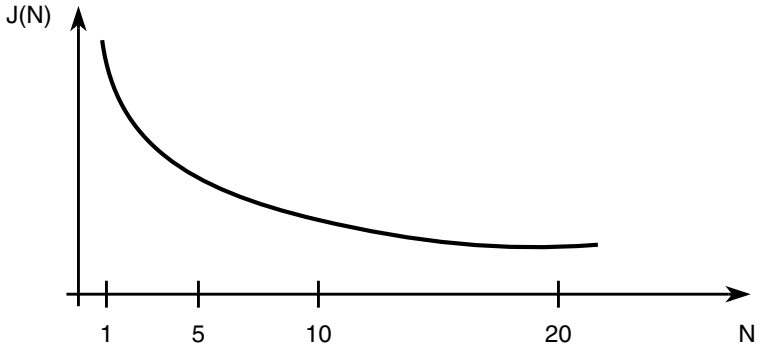
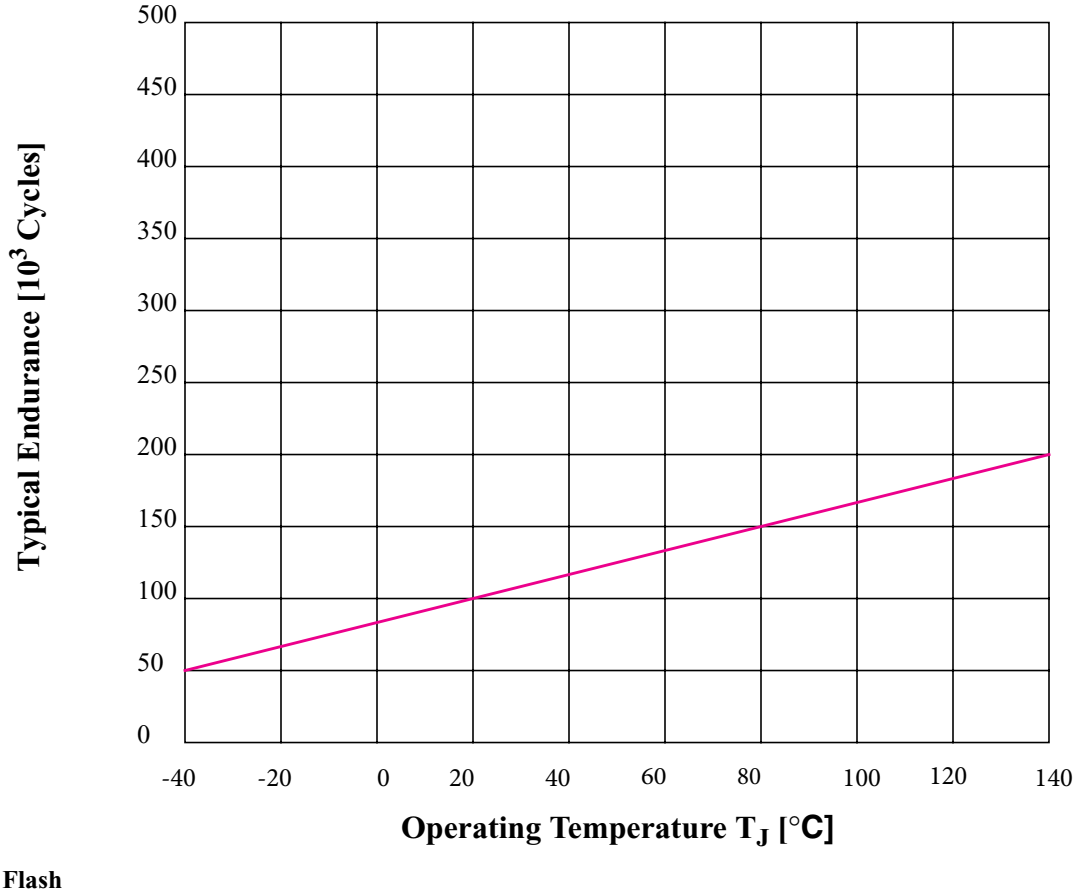


Figure A-4. Maximum Bus Clock Jitter Approximation

This is very important to notice with respect to timers, serial modules where a pre-scaler will eliminate the effect of the jitter to a large extent.

Figure A-5. Typical Endurance vs Temperature



A.6 SPI

This section provides electrical parametrics and ratings for the SPI.

In Table A-20 the measurement conditions are listed.

Table A-20. Measurement Conditions

Description	Value	Unit
Drive mode	Full drive mode	—
Load capacitance $C_{LOAD,}$ on all outputs	50	pF
Thresholds for delay measurement points	(20% / 80%) V_{DDX}	V

A.6.1 Master Mode

In Figure A-6 the timing diagram for master mode with transmission format CPHA=0 is depicted.