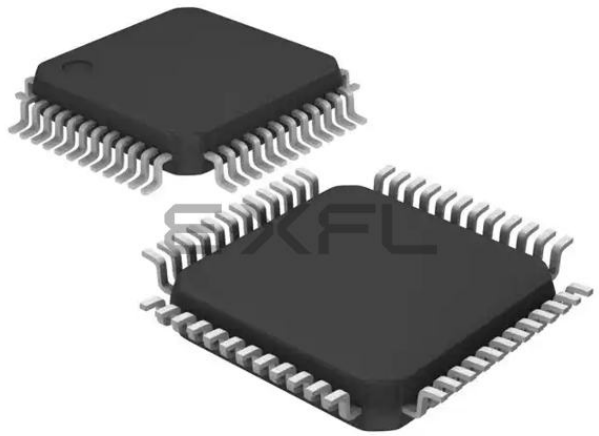

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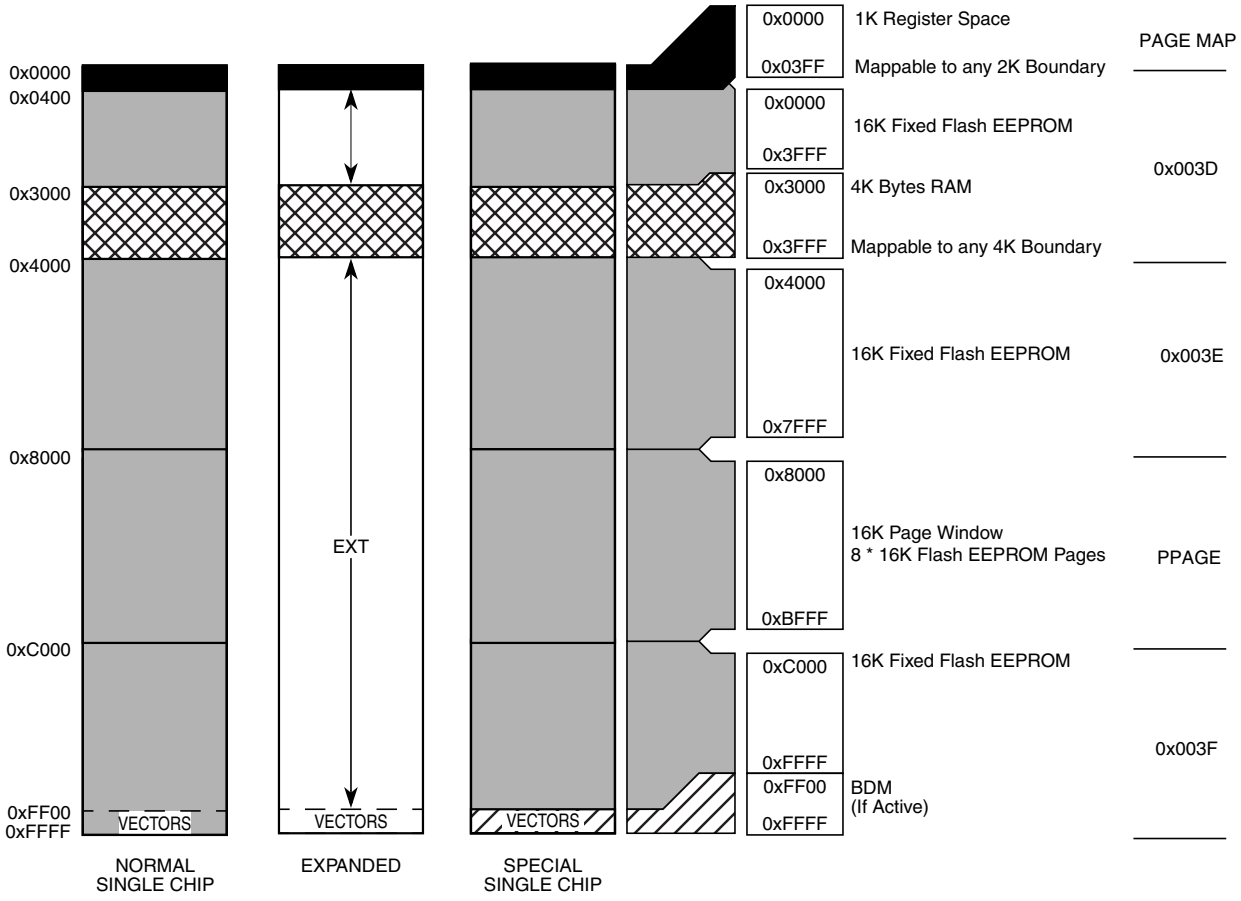
Details	
Product Status	Active
Core Processor	HCS12
Core Size	16-Bit
Speed	25MHz
Connectivity	EBI/EMI, SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	31
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s12gc64mfae



The figure shows a useful map, which is not the map out of reset. After reset the map is:

0x0000–0x03FF: Register Space
0x0000–0x0FFF: 4K RAM (only 3K visible 0x0400–0x0FFF)

Flash erase sector size is 1024 bytes

Figure 1-2. MC9S12C128 and MC9S12GC128 User Configurable Memory Map

0x0180–0x023F Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0180–0x023F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

0x0240–0x027F PIM (Port Interface Module) (Sheet 1 of 3)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0240	PTT	Read:	PTT7	PTT6	PTT5	PTT4	PTT3	PTT2	PTT1	PTT0
		Write:								
0x0241	PTIT	Read:	PTIT7	PTIT6	PTIT5	PTIT4	PTIT3	PTIT2	PTIT1	PTIT0
		Write:								
0x0242	DDRT	Read:	DDRT7	DDRT7	DDRT5	DDRT4	DDRT3	DDRT2	DDRT1	DDRT0
		Write:								
0x0243	RDRT	Read:	RDRT7	RDRT6	RDRT5	RDRT4	RDRT3	RDRT2	RDRT1	RDRT0
		Write:								
0x0244	PERT	Read:	PERT7	PERT6	PERT5	PERT4	PERT3	PERT2	PERT1	PERT0
		Write:								
0x0245	PPST	Read:	PPST7	PPST6	PPST5	PPST4	PPST3	PPST2	PPST1	PPST0
		Write:								
0x0246	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
0x0247	MODRR	Read:	0	0	0	MODRR4	MODRR3	MODRR2	MODRR1	MODRR0
		Write:								
0x0248	PTS	Read:	0	0	0	0	PTS3	PTS2	PTS1	PTS0
		Write:								
0x0249	PTIS	Read:	0	0	0	0	PTIS3	PTIS2	PTIS1	PTIS0
		Write:								
0x024A	DDRS	Read:	0	0	0	0	DDRS3	DDRS2	DDRS1	DDRS0
		Write:								
0x024B	RDRS	Read:	0	0	0	0	RDRS3	RDRS2	RDRS1	RDRS0
		Write:								
0x024C	PERS	Read:	0	0	0	0	PERS3	PERS2	PERS1	PERS0
		Write:								
0x024D	PPSS	Read:	0	0	0	0	PPSS3	PPSS2	PPSS1	PPSS0
		Write:								
0x024E	WOMS	Read:	0	0	0	0	WOMS3	WOMS2	WOMS1	WOMS0
		Write:								
0x024F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
0x0250	PTM	Read:	0	0	PTM5	PTM4	PTM3	PTM2	PTM1	PTM0
		Write:								
0x0251	PTIM	Read:	0	0	PTIM5	PTIM4	PTIM3	PTIM2	PTIM1	PTIM0
		Write:								
0x0252	DDRM	Read:	0	0	DDRM5	DDRM4	DDRM3	DDRM2	DDRM1	DDRM0
		Write:								

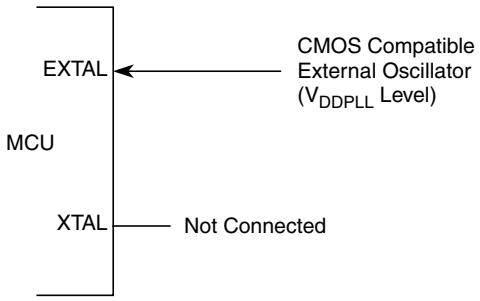


Figure 1-13. External Clock Connections (PE7 = 0)

1.3.4.9 PE6 / MODB / IPIPE1 — Port E I/O Pin 6

PE6 is a general purpose input or output pin. It is used as a MCU operating mode select pin during reset. The state of this pin is latched to the MODB bit at the rising edge of $\overline{\text{RESET}}$. This pin is shared with the instruction queue tracking signal IPIPE1. This pin is an input with a pull-down device which is only active when $\overline{\text{RESET}}$ is low. PE[6] is not available in the 48- / 52-pin package versions.

1.3.4.10 PE5 / MODA / IPIPE0 — Port E I/O Pin 5

PE5 is a general purpose input or output pin. It is used as a MCU operating mode select pin during reset. The state of this pin is latched to the MODA bit at the rising edge of $\overline{\text{RESET}}$. This pin is shared with the instruction queue tracking signal IPIPE0. This pin is an input with a pull-down device which is only active when $\overline{\text{RESET}}$ is low. This pin is not available in the 48- / 52-pin package versions.

1.3.4.11 PE4 / ECLK— Port E I/O Pin [4] / E-Clock Output

ECLK is the output connection for the internal bus clock. It is used to demultiplex the address and data in expanded modes and is used as a timing reference. ECLK frequency is equal to 1/2 the crystal frequency out of reset. The ECLK pin is initially configured as ECLK output with stretch in all expanded modes. The E clock output function depends upon the settings of the NECLK bit in the PEAR register, the IVIS bit in the MODE register and the ESTR bit in the EBICTL register. All clocks, including the E clock, are halted when the MCU is in stop mode. It is possible to configure the MCU to interface to slow external memory. ECLK can be stretched for such accesses. Reference the MISC register (EXSTR[1:0] bits) for more information. In normal expanded narrow mode, the E clock is available for use in external select decode logic or as a constant speed clock for use in the external application system. Alternatively PE4 can be used as a general purpose input or output pin.

1.3.4.12 PE3 / $\overline{\text{LSTRB}}$ — Port E I/O Pin [3] / Low-Byte Strobe ($\overline{\text{LSTRB}}$)

In all modes this pin can be used as a general-purpose I/O and is an input with an active pull-up out of reset. If the strobe function is required, it should be enabled by setting the LSTRE bit in the PEAR register. This signal is used in write operations. Therefore external low byte writes will not be possible until this function is enabled. This pin is also used as $\overline{\text{TAGLO}}$ in special expanded modes and is multiplexed with the $\overline{\text{LSTRB}}$ function. This pin is not available in the 48- / 52-pin package versions.

the Flash EEPROM memory in the memory map (ROMCTL). At the rising edge of $\overline{\text{RESET}}$, the state of this pin is latched to the ROMON bit.

- PP6 = 1 in emulation modes equates to ROMON = 0 (ROM space externally mapped)
- PP6 = 0 in expanded modes equates to ROMON = 0 (ROM space externally mapped)

1.3.4.19 PP[5:0] / KWP[5:0] / PW[5:0] — Port P I/O Pins [5:0]

PP[5:0] are general purpose input or output pins, shared with the keypad interrupt function. When configured as inputs, they can generate interrupts causing the MCU to exit stop or wait mode.

PP[5:0] are also shared with the PWM output signals, PW[5:0]. Pins PP[2:0] are only available in the 80-pin package version. Pins PP[4:3] are not available in the 48-pin package version.

1.3.4.20 PJ[7:6] / KWJ[7:6] — Port J I/O Pins [7:6]

PJ[7:6] are general purpose input or output pins, shared with the keypad interrupt function. When configured as inputs, they can generate interrupts causing the MCU to exit stop or wait mode. These pins are not available in the 48-pin package version nor in the 52-pin package version.

1.3.4.21 PM5 / SCK — Port M I/O Pin 5

PM5 is a general purpose input or output pin and also the serial clock pin SCK for the serial peripheral interface (SPI).

1.3.4.22 PM4 / MOSI — Port M I/O Pin 4

PM4 is a general purpose input or output pin and also the master output (during master mode) or slave input (during slave mode) pin for the serial peripheral interface (SPI).

1.3.4.23 PM3 / $\overline{\text{SS}}$ — Port M I/O Pin 3

PM3 is a general purpose input or output pin and also the slave select pin $\overline{\text{SS}}$ for the serial peripheral interface (SPI).

1.3.4.24 PM2 / MISO — Port M I/O Pin 2

PM2 is a general purpose input or output pin and also the master input (during master mode) or slave output (during slave mode) pin for the serial peripheral interface (SPI).

1.3.4.25 PM1 / TXCAN — Port M I/O Pin 1

PM1 is a general purpose input or output pin and the transmit pin, TXCAN, of the CAN module if available.

1.3.4.26 PM0 / RXCAN — Port M I/O Pin 0

PM0 is a general purpose input or output pin and the receive pin, RXCAN, of the CAN module if available.

2.3.2.1.2 Port T Input Register (PTIT)

Module Base + 0x0001

	7	6	5	4	3	2	1	0
R	PTIT7	PTIT6	PTIT5	PTIT4	PTIT3	PTIT2	PTIT1	PTIT0
W								
Reset	—	—	—	—	—	—	—	—

= Unimplemented or Reserved

Figure 2-4. Port T Input Register (PTIT)

Read: Anytime.

Write: Never, writes to this register have no effect.

Table 2-4. PTIT Field Descriptions

Field	Description
7–0 PTIT[7:0]	**Port T Input Register** — This register always reads back the status of the associated pins. This can also be used to detect overload or short circuit conditions on output pins.

2.3.2.1.3 Port T Data Direction Register (DDRT)

Module Base + 0x0002

	7	6	5	4	3	2	1	0
R W	DDRT7	DDRT6	DDRT5	DDRT4	DDRT3	DDRT2	DDRT1	DDRT0
Reset	0	0	0	0	0	0	0	0

Figure 2-5. Port T Data Direction Register (DDRT)

Read: Anytime.

Write: Anytime.

Table 2-5. DDRT Field Descriptions

Field	Description
7–0 DDRT[7:0]	**Data Direction Port T** — This register configures each port T pin as either input or output. The standard TIM / PWM modules forces the I/O state to be an output for each standard TIM / PWM module port associated with an enabled output compare. In these cases the data direction bits will not change. The DDRT bits revert to controlling the I/O direction of a pin when the associated timer output compare is disabled. The timer input capture always monitors the state of the pin. 0 Associated pin is configured as input. 1 Associated pin is configured as output. **Note:** Due to internal synchronization circuits, it can take up to 2 bus cycles until the correct value is read on PTT or PTIT registers, when changing the DDRT register.

7.3.2.2 Debug Status and Control Register (DBGSC)

Module Base + 0x0021
Starting address location affected by INITRG register setting.

	7	6	5	4	3	2	1	0
R	AF	BF	CF	0	TRG			
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 7-5. Debug Status and Control Register (DBGSC)

Table 7-5. DBGSC Field Descriptions

Field	Description
7 AF	**Trigger A Match Flag** — The AF bit indicates if trigger A match condition was met since arming. This bit is cleared when ARM in DBGC1 is written to a 1 or on any write to this register. 0 Trigger A did not match 1 Trigger A match
6 BF	**Trigger B Match Flag** — The BF bit indicates if trigger B match condition was met since arming.This bit is cleared when ARM in DBGC1 is written to a 1 or on any write to this register. 0 Trigger B did not match 1 Trigger B match
5 CF	**Comparator C Match Flag** — The CF bit indicates if comparator C match condition was met since arming.This bit is cleared when ARM in DBGC1 is written to a 1 or on any write to this register. 0 Comparator C did not match 1 Comparator C match
3:0 TRG	**Trigger Mode Bits** — The TRG bits select the trigger mode of the DBG module as shown Table 7-6. See Section 7.4.2.5, “Trigger Modes,” for more detail.

Table 7-6. Trigger Mode Encoding

TRG Value	Meaning
0000	A only
0001	A or B
0010	A then B
0011	Event only B
0100	A then event only B
0101	A and B (full mode)
0110	A and Not B (full mode)
0111	Inside range
1000	Outside range
1001 ↓ 1111	Reserved (Defaults to A only)

10.3.2.10 MSCAN Transmitter Message Abort Acknowledge Register (CANTAAK)

The CANTAAK register indicates the successful abort of a queued message, if requested by the appropriate bits in the CANTARQ register.

Module Base + 0x0009

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	ABTAK2	ABTAK1	ABTAK0
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 10-13. MSCAN Transmitter Message Abort Acknowledge Register (CANTAAK)

NOTE

The CANTAAK register is held in the reset state when the initialization mode is active (INITRQ = 1 and INITAK = 1).

Read: Anytime
Write: Unimplemented for ABTAKx flags

Table 10-14. CANTAAK Register Field Descriptions

Field	Description
2:0 ABTAK[2:0]	**Abort Acknowledge** — This flag acknowledges that a message was aborted due to a pending abort request from the CPU. After a particular message buffer is flagged empty, this flag can be used by the application software to identify whether the message was aborted successfully or was sent anyway. The ABTAKx flag is cleared whenever the corresponding TXE flag is cleared. 0 The message was not aborted. 1 The message was aborted.

NOTE

Reading this register when in any other mode other than sleep or initialization mode may return an incorrect value. For MCUs with dual CPUs, this may result in a CPU fault condition.

Writing to this register when in special modes can alter the MSCAN functionality.

10.3.2.15 MSCAN Transmit Error Counter (CANTXERR)

This register reflects the status of the MSCAN transmit error counter.

Module Base + 0x000F

	7	6	5	4	3	2	1	0
R	TXERR7	TXERR6	TXERR5	TXERR4	TXERR3	TXERR2	TXERR1	TXERR0
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 10-18. MSCAN Transmit Error Counter (CANTXERR)

Read: Only when in sleep mode (SLPRQ = 1 and SLPAK = 1) or initialization mode (INITRQ = 1 and INITAK = 1)

Write: Unimplemented

NOTE

Reading this register when in any other mode other than sleep or initialization mode, may return an incorrect value. For MCUs with dual CPUs, this may result in a CPU fault condition.

Writing to this register when in special modes can alter the MSCAN functionality.

Module Base + 0x0018 (CANIDAR4)
0x0019 (CANIDAR5)
0x001A (CANIDAR6)
0x001B (CANIDAR7)

	7	6	5	4	3	2	1	0
R W	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
Reset	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
R W	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
Reset	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
R W	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
Reset	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
R W	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
Reset	0	0	0	0	0	0	0	0

Figure 10-20. MSCAN Identifier Acceptance Registers (Second Bank) — CANIDAR4–CANIDAR7

Read: Anytime

Write: Anytime in initialization mode (INITRQ = 1 and INITAK = 1)

Table 10-20. CANIDAR4–CANIDAR7 Register Field Descriptions

Field	Description
7:0 AC[7:0]	**Acceptance Code Bits** — AC[7:0] comprise a user-defined sequence of bits with which the corresponding bits of the related identifier register (IDRn) of the receive message buffer are compared. The result of this comparison is then masked with the corresponding identifier mask register.

15.3.2.9 Timer Control Register 3/Timer Control Register 4 (TCTL3 and TCTL4)

Module Base + 0x000A

	7	6	5	4	3	2	1	0
R W	EDG7B	EDG7A	EDG6B	EDG6A	EDG5B	EDG5A	EDG4B	EDG4A
Reset	0	0	0	0	0	0	0	0

Figure 15-16. Timer Control Register 3 (TCTL3)

Module Base + 0x000B

	7	6	5	4	3	2	1	0
R W	EDG3B	EDG3A	EDG2B	EDG2A	EDG1B	EDG1A	EDG0B	EDG0A
Reset	0	0	0	0	0	0	0	0

Figure 15-17. Timer Control Register 4 (TCTL4)

Read: Anytime

Write: Anytime.

Table 15-12. TCTL3/TCTL4 Field Descriptions

Field	Description
7:0 EDGnB EDGnA	**Input Capture Edge Control** — These eight pairs of control bits configure the input capture edge detector circuits.

Table 15-13. Edge Detector Circuit Configuration

EDGnB	EDGnA	Configuration
0	0	Capture disabled
0	1	Capture on rising edges only
1	0	Capture on falling edges only
1	1	Capture on any edge (rising or falling)

15.4.2 Input Capture

Clearing the I/O (input/output) select bit, IOSx, configures channel x as an input capture channel. The input capture function captures the time at which an external event occurs. When an active edge occurs on the pin of an input capture channel, the timer transfers the value in the timer counter into the timer channel registers, TCx.

The minimum pulse width for the input capture input is greater than two bus clocks.

An input capture on channel x sets the CxF flag. The CxI bit enables the CxF flag to generate interrupt requests. Timer module must stay enabled (TEN bit of TSCR1 must be set to one) while clearing CxF (writing one to CxF).

15.4.3 Output Compare

Setting the I/O select bit, IOSx, configures channel x as an output compare channel. The output compare function can generate a periodic pulse with a programmable polarity, duration, and frequency. When the timer counter reaches the value in the channel registers of an output compare channel, the timer can set, clear, or toggle the channel pin. An output compare on channel x sets the CxF flag. The CxI bit enables the CxF flag to generate interrupt requests. Timer module must stay enabled (TEN bit of TSCR1 register must be set to one) while clearing CxF (writing one to CxF).

The output mode and level bits, OMx and OLx, select set, clear, toggle on output compare. Clearing both OMx and OLx disconnects the pin from the output logic.

Setting a force output compare bit, FOCx, causes an output compare on channel x. A forced output compare does not set the channel flag.

A successful output compare on channel 7 overrides output compares on all other output compare channels. The output compare 7 mask register masks the bits in the output compare 7 data register. The timer counter reset enable bit, TCRE, enables channel 7 output compares to reset the timer counter. A channel 7 output compare can reset the timer counter even if the IOC7 pin is being used as the pulse accumulator input.

Writing to the timer port bit of an output compare pin does not affect the pin state. The value written is stored in an internal latch. When the pin becomes available for general-purpose output, the last value written to the bit appears at the pin.

When TCRE is set and TC7 is not equal to 0, then TCNT will cycle from 0 to TC7. When TCNT reaches TC7 value, it will last only one bus cycle then reset to 0.

16.1.3 Block Diagram

Figure 16-1 shows the function principle of VREG3V3V2 by means of a block diagram. The regulator core REG consists of two parallel sub-blocks, REG1 and REG2, providing two independent output voltages.

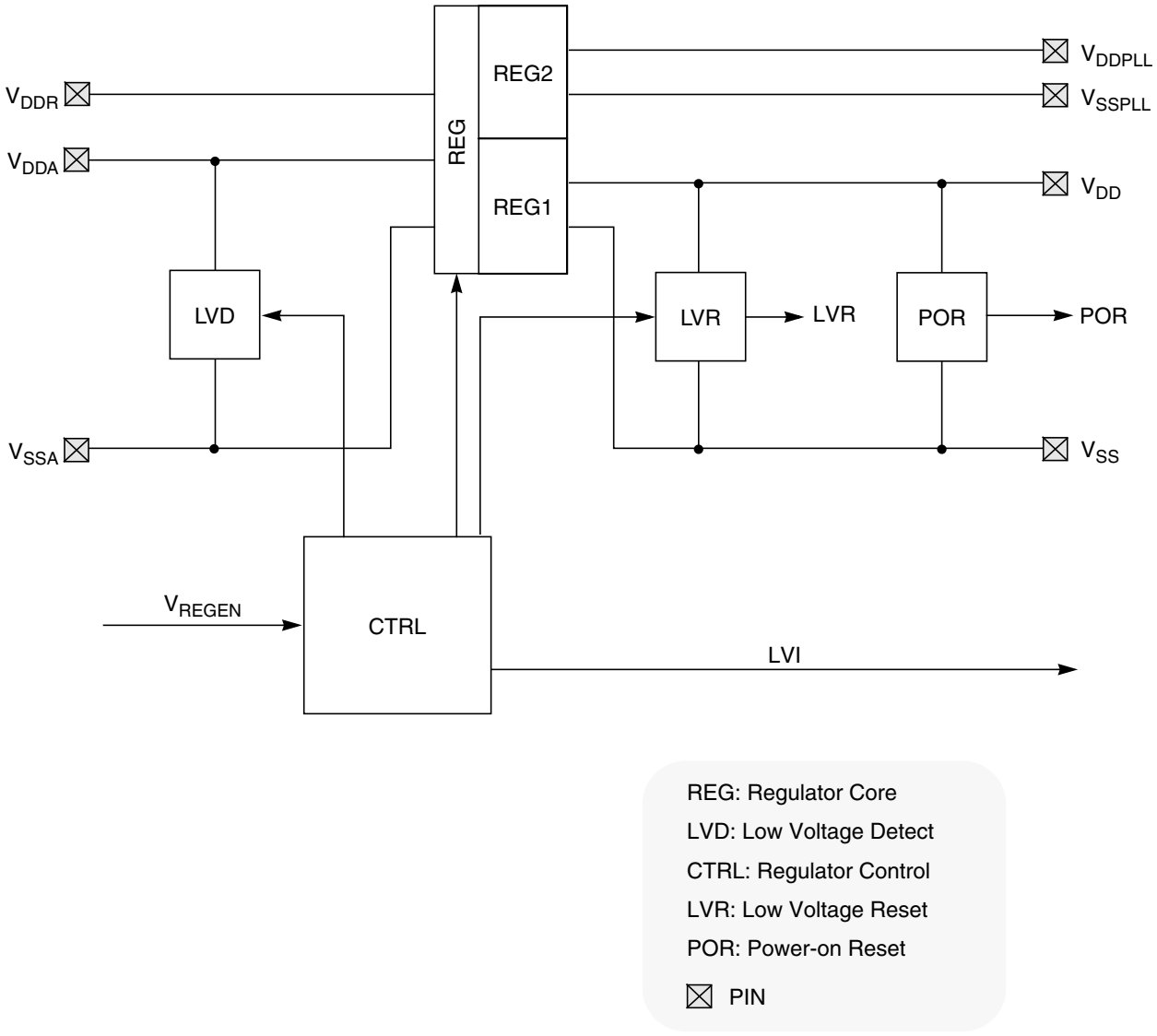


Figure 16-1. VREG3V3 Block Diagram

To change the Flash protection that will be loaded on reset, the upper sector of the Flash array must be unprotected, then the Flash protection byte located at Flash address 0xFF0D must be written to.

A protected Flash sector is disabled by FPHDIS while the size of the protected sector is defined by FPHS[1:0] in the FPROT register.

Trying to alter any of the protected areas will result in a protect violation error and the PVIOL flag will be set in the FSTAT register (see Section 17.3.2.6). A mass erase of the whole Flash array is only possible when protection is fully disabled by setting the FPOPEN and FPHDIS bits. An attempt to mass erase a Flash array while protection is enabled will set the PVIOL flag in the FSTAT register.

Table 17-8. FPROT Field Descriptions

Field	Description
7 FPOPEN	**Protection Function for Program or Erase** — The FPOPEN bit is used to either select an address range to be protected using the FPHDIS and FPHS[1:0] bits or to select the same address range to be unprotected as shown in Table 17-9. 0 The FPHDIS bit allows a Flash address range to be unprotected 1 The FPHDIS bit allows a Flash address range to be protected
6 NV6	**Nonvolatile Flag Bit** — The NV6 bit should remain in the erased state for future enhancements.
5 FPHDIS	**Flash Protection Higher Address Range Disable** — The FPHDIS bit determines whether there is a protected/unprotected area in the higher space of the Flash address map. 0 Protection/unprotection enabled 1 Protection/unprotection disabled
4–3 FPHS[1:0]	**Flash Protection Higher Address Size** — The FPHS[1:0] bits determine the size of the protected/unprotected sector as shown in Table 17-10. The FPHS[1:0] bits can only be written to while the FPHDIS bit is set.
2–0 NV[2:0]	**Nonvolatile Flag Bits** — The NV[2:0] bits should remain in the erased state for future enhancements.

Table 17-9. Flash Protection Function

FPOPEN	FPHDIS	FPHS1	FPHS0	Function(1)
1	1	x	x	No protection
1	0	x	x	Protect high range
0	1	x	x	Full Flash array protected
0	0	x	x	Unprotected high range

1. For range sizes refer to Table 17-10.

Table 17-10. Flash Protection Higher Address Range

FPHS[1:0]	Address Range	Range Size
00	0xF800–0xFFFF	2 Kbytes
01	0xF000–0xFFFF	4 Kbytes
10	0xE000–0xFFFF	8 Kbytes
11	0xC000–0xFFFF	16 Kbytes

Module Base + 0x0009

	7	6	5	4	3	2	1	0
R W	FABLO							
Reset	0	0	0	0	0	0	0	0

Figure 17-14. Flash Address Low Register (FADDRLO)

In normal modes, all FABHI and FABLO bits read 0 and are not writable. In special modes, the FABHI and FABLO bits are readable and writable. For sector erase, the MCU address bits [8:0] are ignored. For mass erase, any address within the Flash array is valid to start the command.

17.3.2.10 Flash Data Register (FDATA)

FDATAHI and FDATALO are the Flash data registers.

Module Base + 0x000A

	7	6	5	4	3	2	1	0
R W	FDHI							
Reset	0	0	0	0	0	0	0	0

Figure 17-15. Flash Data High Register (FDATAHI)

Module Base + 0x000B

	7	6	5	4	3	2	1	0
R W	FDLO							
Reset	0	0	0	0	0	0	0	0

Figure 17-16. Flash Data Low Register (FDATALO)

In normal modes, all FDATAHI and FDATALO bits read 0 and are not writable. In special modes, all FDATAHI and FDATALO bits are readable and writable when writing to an address within the Flash address range.

17.3.2.11 RESERVED3

This register is reserved for factory testing and is not accessible to the user.

18.4.1.3.2 Program Command

The program operation will program a previously erased word in the Flash array using an embedded algorithm.

An example flow to execute the program operation is shown in Figure 18-23. The program command write sequence is as follows:

1. Write to a Flash array address to start the command write sequence for the program command. The data written will be programmed to the Flash array address written.
2. Write the program command, 0x20, to the FCMD register.
3. Clear the CBEIF flag in the FSTAT register by writing a 1 to CBEIF to launch the program command.

If a word to be programmed is in a protected area of the Flash array, the PVIOL flag in the FSTAT register will set and the program command will not launch. Once the program command has successfully launched, the CCIF flag in the FSTAT register will set after the program operation has completed unless a new command write sequence has been buffered. By executing a new program command write sequence on sequential words after the CBEIF flag in the FSTAT register has been set, up to 55% faster programming time per word can be effectively achieved than by waiting for the CCIF flag to set after each program operation.

Table 19-3. Flash Array Memory Map Summary

MCU Address Range	PPAGE	Protectable Low Range	Protectable High Range	Array Relative Address[1]
0x0000–0x3FFF[2]	Unpaged (0x3D)	N.A.	N.A.	0x14000–0x17FFF
0x4000–0x7FFF	Unpaged (0x3E)	0x4000–0x43FF 0x4000–0x47FF 0x4000–0x4FFF 0x4000–0x5FFF	N.A.	0x18000–0x1BFFF
0x8000–0xBFFF	0x3C	N.A.	N.A.	0x10000–0x13FFF
	0x3D	N.A.	N.A.	0x14000–0x17FFF
	0x3E	0x8000–0x83FF 0x8000–0x87FF 0x8000–0x8FFF 0x8000–0x9FFF	N.A.	0x18000–0x1BFFF
	0x3F	N.A.	0xB800–0xBFFF 0xB000–0xBFFF 0xA000–0xBFFF 0x8000–0xBFFF	0x1C000–0x1FFFF
0xC000–0xFFFF	Unpaged (0x3F)	N.A.	0xF800–0xFFFF 0xF000–0xFFFF 0xE000–0xFFFF 0xC000–0xFFFF	0x1C000–0x1FFFF

1. Inside Flash block.
2. If allowed by MCU.

Module Base + 0x000C

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 21-17. RESERVED3

All bits read 0 and are not writable.

21.3.2.12 RESERVED4

This register is reserved for factory testing and is not accessible to the user.

Module Base + 0x000D

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 21-18. RESERVED4

All bits read 0 and are not writable.

21.3.2.13 RESERVED5

This register is reserved for factory testing and is not accessible to the user.

Module Base + 0x000E

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 21-19. RESERVED5

All bits read 0 and are not writable.

21.3.2.14 RESERVED6

This register is reserved for factory testing and is not accessible to the user.

Table A-5. Thermal Package Characteristics[1]

Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	T	Thermal Resistance LQFP48, single layer PCB[2]	θ_{JA}	—	—	69	°C/W
2	T	Thermal Resistance LQFP48, double sided PCB with 2 internal planes[3]	θ_{JA}	—	—	53	°C/W
3	T	Junction to Board LQFP48	θ_{JB}	—	—	30	°C/W
4	T	Junction to Case LQFP48	θ_{JC}	—	—	20	°C/W
5	T	Junction to Package Top LQFP48	Ψ_{JT}	—	—	4	°C/W
6	T	Thermal Resistance LQFP52, single sided PCB	θ_{JA}	—	—	65	°C/W
7	T	Thermal Resistance LQFP52, double sided PCB with 2 internal planes	θ_{JA}	—	—	49	°C/W
8	T	Junction to Board LQFP52	θ_{JB}	—	—	31	°C/W
9	T	Junction to Case LQFP52	θ_{JC}	—	—	17	°C/W
10	T	Junction to Package Top LQFP52	Ψ_{JT}	—	—	3	°C/W
11	T	Thermal Resistance QFP 80, single sided PCB	θ_{JA}	—	—	52	°C/W
12	T	Thermal Resistance QFP 80, double sided PCB with 2 internal planes	θ_{JA}	—	—	42	°C/W
13	T	Junction to Board QFP80	θ_{JB}	—	—	28	°C/W
14	T	Junction to Case QFP80	θ_{JC}	—	—	18	°C/W
15	T	Junction to Package Top QFP80	Ψ_{JT}	—	—	4	°C/W

1. The values for thermal resistance are achieved by package simulations
2. PC Board according to EIA/JEDEC Standard 51-2
3. PC Board according to EIA/JEDEC Standard 51-7

A.1.10.2 Additional Remarks

In expanded modes the currents flowing in the system are highly dependent on the load at the address, data and control signals as well as on the duty cycle of those signals. No generally applicable numbers can be given. A very good estimate is to take the single chip currents and add the currents due to the external loads.

Table A-8. Supply Current Characteristics for MC9S12CG16 MC9S12C32

Conditions are shown in Table A-4 with internal regulator enabled unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Run Supply Current Single Chip	I_{DD5}	—	—	35	mA
2		Wait Supply current	I_{DDW}				mA
	P	All modules enabled		—		30	
	P	V_{DDR}<4.9V, only RTI enabled[2]		—	3.5	8	
	C	V_{DDR}>4.9V, only RTI enabled		—	2.5		
3		Pseudo Stop Current (RTI and COP disabled)[2 3]	I_{DDPS}[(1)]				µA
	C	–40°C		—	340	—	
	P	27°C		—	360	450	
	C	85°C		—	500	—	
	P	"C" Temp Option 100˚C		—	550	1450	
	C	105°C		—	590	—	
	P	"V" Temp Option 120˚C		—	720	1900	
	C	125°C		—	780	—	
	P	"M" Temp Option 140°C		—	1100	4500	
4		Pseudo Stop Current (RTI and COP enabled)[(2) (3)]	I_{DDPS}[1]				µA
	C	–40°C		—	540	—	
	C	27°C		—	700	—	
	C	85°C		—	750	—	
	C	105°C		—	880	—	
	C	125°C		—	1300	—	
5		Stop Current [3]	I_{DDS}[1]				µA
	C	–40°C		—	10	—	
	P	27°C		—	20	80	
	C	85°C		—	100	—	
	P	"C" Temp Option 100˚C		—	140	1000	
	C	105°C		—	170	—	
	P	"V" Temp Option 120˚C		—	300	1400	
	C	125°C		—	350	—	
	P	"M" Temp Option 140°C		—	520	4000	

1. STOP current measured in production test at increased junction temperature, hence for Temp Option "C" the test is carried out at 100˚C although the Temperature specification is 85˚C. Similarly for "v" and "M" options the temperature used in test lies 15˚C above the temperature option specification.
2. PLL off
3. At those low power dissipation levels $T_J = T_A$ can be assumed

A.7 Voltage Regulator

A.7.1 Voltage Regulator Operating Conditions

Table A-23. Voltage Regulator Electrical Parameters

Num	C	Characteristic	Symbol	Min	Typ	Max	Unit
1	P	Input Voltages	$V_{VDDR, A}$	2.97	—	5.5	V
3	P	Output Voltage Core Full Performance Mode	V_{DD}	2.35	2.5	2.75	V
4	P	Low Voltage Interrupt[1] Assert Level (xL45J mask set) Assert Level (other mask sets) Deassert Level (xL45J mask set) Deassert Level (other mask sets)	 V_{LVIA} V_{LVIA} V_{LVID} V_{LVID}	 4.30 4.00 4.42 4.15	 4.53 4.37 4.65 4.52	 4.77 4.66 4.89 4.77	 V V V V
5	P	Low Voltage Reset[2],[3] Assert Level (xL45J mask set) Assert Level (other mask sets)	V_{LVRA}	 2.25 2.25	 2.3 2.35	 — —	V
7	C	Power-on Reset[4] Assert Level Deassert Level	 V_{PORA} V_{PORD}	 0.97 —	 — —	 — 2.05	 V V

1. Monitors V_{DDA}, active only in Full Performance Mode. Indicates I/O & ADC performance degradation due to low supply voltage.
2. Monitors V_{DD}, active only in Full Performance Mode. MCU is monitored by the POR in RPM (see Figure A-10)
3. Digital functionality is guaranteed in the range between V_{DD}(min) and V_{LVRA}(min).
4. Monitors V_{DD}. Active in all modes.

A.7.2 Chip Power-up and LVI/LVR Graphical Explanation

Voltage regulator sub modules LVI (low voltage interrupt), POR (power-on reset) and LVR (low voltage reset) handle chip power-up or drops of the supply voltage. Their function is described in Figure A-10.