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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HCS12
Core Size	16-Bit
Speed	25MHz
Connectivity	EBI/EMI, SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	60
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	80-QFP
Supplier Device Package	80-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcs12gc64mfue

- Operating frequency:
  - 32MHz equivalent to 16MHz bus speed for single chip
  - 32MHz equivalent to 16MHz bus speed in expanded bus modes
  - Option of 9S12C Family: 50MHz equivalent to 25MHz bus speed
  - All 9S12GC Family members allow a 50MHz operating frequency.
- Internal 2.5V regulator:
  - Supports an input voltage range from 2.97V to 5.5V
  - Low power mode capability
  - Includes low voltage reset (LVR) circuitry
  - Includes low voltage interrupt (LVI) circuitry
- 48-pin LQFP, 52-pin LQFP, or 80-pin QFP package:
  - Up to 58 I/O lines with 5V input and drive capability (80-pin package)
  - Up to 2 dedicated 5V input only lines (IRQ, XIRQ)
  - 5V 8 A/D converter inputs and 5V I/O
- Development support:
  - Single-wire background debug™ mode (BDM)
  - On-chip hardware breakpoints
  - Enhanced DBG12 debug features

1.1.2 Modes of Operation

User modes (expanded modes are only available in the 80-pin package version).

- Normal and emulation operating modes:
  - Normal single-chip mode
  - Normal expanded wide mode
  - Normal expanded narrow mode
  - Emulation expanded wide mode
  - Emulation expanded narrow mode
- Special operating modes:
  - Special single-chip mode with active background debug mode
  - Special test mode **(Freescale use only)**
  - Special peripheral mode **(Freescale use only)**
- Low power modes:
  - Stop mode
  - Pseudo stop mode
  - Wait mode

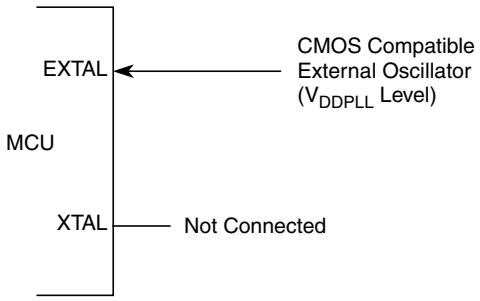


Figure 1-13. External Clock Connections (PE7 = 0)

1.3.4.9 PE6 / MODB / IPIPE1 — Port E I/O Pin 6

PE6 is a general purpose input or output pin. It is used as a MCU operating mode select pin during reset. The state of this pin is latched to the MODB bit at the rising edge of $\overline{\text{RESET}}$. This pin is shared with the instruction queue tracking signal IPIPE1. This pin is an input with a pull-down device which is only active when $\overline{\text{RESET}}$ is low. PE[6] is not available in the 48- / 52-pin package versions.

1.3.4.10 PE5 / MODA / IPIPE0 — Port E I/O Pin 5

PE5 is a general purpose input or output pin. It is used as a MCU operating mode select pin during reset. The state of this pin is latched to the MODA bit at the rising edge of $\overline{\text{RESET}}$. This pin is shared with the instruction queue tracking signal IPIPE0. This pin is an input with a pull-down device which is only active when $\overline{\text{RESET}}$ is low. This pin is not available in the 48- / 52-pin package versions.

1.3.4.11 PE4 / ECLK— Port E I/O Pin [4] / E-Clock Output

ECLK is the output connection for the internal bus clock. It is used to demultiplex the address and data in expanded modes and is used as a timing reference. ECLK frequency is equal to 1/2 the crystal frequency out of reset. The ECLK pin is initially configured as ECLK output with stretch in all expanded modes. The E clock output function depends upon the settings of the NECLK bit in the PEAR register, the IVIS bit in the MODE register and the ESTR bit in the EBICTL register. All clocks, including the E clock, are halted when the MCU is in stop mode. It is possible to configure the MCU to interface to slow external memory. ECLK can be stretched for such accesses. Reference the MISC register (EXSTR[1:0] bits) for more information. In normal expanded narrow mode, the E clock is available for use in external select decode logic or as a constant speed clock for use in the external application system. Alternatively PE4 can be used as a general purpose input or output pin.

1.3.4.12 PE3 / $\overline{\text{LSTRB}}$ — Port E I/O Pin [3] / Low-Byte Strobe ($\overline{\text{LSTRB}}$)

In all modes this pin can be used as a general-purpose I/O and is an input with an active pull-up out of reset. If the strobe function is required, it should be enabled by setting the LSTRE bit in the PEAR register. This signal is used in write operations. Therefore external low byte writes will not be possible until this function is enabled. This pin is also used as $\overline{\text{TAGLO}}$ in special expanded modes and is multiplexed with the $\overline{\text{LSTRB}}$ function. This pin is not available in the 48- / 52-pin package versions.

1.3.4.13 PE2 / R/$\overline{W}$ — Port E I/O Pin [2] / Read/Write

In all modes this pin can be used as a general-purpose I/O and is an input with an active pull-up out of reset. If the read/write function is required it should be enabled by setting the RDWE bit in the PEAR register. External writes will not be possible until enabled. This pin is not available in the 48- / 52-pin package versions.

1.3.4.14 PE1 / $\overline{IRQ}$ — Port E Input Pin [1] / Maskable Interrupt Pin

The $\overline{IRQ}$ input provides a means of applying asynchronous interrupt requests to the MCU. Either falling edge-sensitive triggering or level-sensitive triggering is program selectable (INTCR register). $\overline{IRQ}$ is always enabled and configured to level-sensitive triggering out of reset. It can be disabled by clearing IRQEN bit (INTCR register). When the MCU is reset the $\overline{IRQ}$ function is masked in the condition code register. This pin is always an input and can always be read. There is an active pull-up on this pin while in reset and immediately out of reset. The pull-up can be turned off by clearing PUPEE in the PUCR register.

1.3.4.15 PE0 / $\overline{XIRQ}$ — Port E input Pin [0] / Non Maskable Interrupt Pin

The $\overline{XIRQ}$ input provides a means of requesting a non-maskable interrupt after reset initialization. During reset, the X bit in the condition code register (CCR) is set and any interrupt is masked until MCU software enables it. Because the $\overline{XIRQ}$ input is level sensitive, it can be connected to a multiple-source wired-OR network. This pin is always an input and can always be read. There is an active pull-up on this pin while in reset and immediately out of reset. The pull-up can be turned off by clearing PUPEE in the PUCR register.

1.3.4.16 PAD[7:0] / AN[7:0] — Port AD I/O Pins [7:0]

PAD7–PAD0 are general purpose I/O pins and also analog inputs for the analog to digital converter. In order to use a PAD pin as a standard input, the corresponding ATDDIEN register bit must be set. These bits are cleared out of reset to configure the PAD pins for A/D operation.

When the A/D converter is active in multi-channel mode, port inputs are scanned and converted irrespective of Port AD configuration. Thus Port AD pins that are configured as digital inputs or digital outputs are also converted in the A/D conversion sequence.

1.3.4.17 PP[7] / KWP[7] — Port P I/O Pin [7]

PP7 is a general purpose input or output pin, shared with the keypad interrupt function. When configured as an input, it can generate interrupts causing the MCU to exit stop or wait mode. This pin is not available in the 48- / 52-pin package versions.

1.3.4.18 PP[6] / KWP[6]/ROMCTL — Port P I/O Pin [6]

PP6 is a general purpose input or output pin, shared with the keypad interrupt function. When configured as an input, it can generate interrupts causing the MCU to exit stop or wait mode. This pin is not available in the 48- / 52-pin package versions. During MCU expanded modes of operation, this pin is used to enable

1.6.2 Resets

Resets are a subset of the interrupts featured in Table 1-9. The different sources capable of generating a system reset are summarized in Table 1-10. When a reset occurs, MCU registers and control bits are changed to known start-up states. Refer to the respective module Block User Guides for register reset states.

1.6.2.1 Reset Summary Table

Table 1-10. Reset Summary

Reset	Priority	Source	Vector
Power-on Reset	1	CRG module	0xFFFE, 0xFFFF
External Reset	1	$\overline{\text{RESET}}$ pin	0xFFFE, 0xFFFF
Low Voltage Reset	1	VREG module	0xFFFE, 0xFFFF
Clock Monitor Reset	2	CRG module	0xFFFC, 0xFFFD
COP Watchdog Reset	3	CRG module	0xFFFA, 0xFFFB

1.6.2.2 Effects of Reset

When a reset occurs, MCU registers and control bits are changed to known start-up states. Refer to the respective module Block User Guides for register reset states. Refer to the HCS12 Multiplexed External Bus Interface (MEBI) Block Guide for mode dependent pin configuration of port A, B and E out of reset.

Refer to the PIM Block User Guide for reset configurations of all peripheral module ports.

Refer to Figure 1-2 to Figure 1-6 footnotes for locations of the memories depending on the operating mode after reset.

The RAM array is not automatically initialized out of reset.

NOTE

For devices assembled in 48-pin or 52-pin LQFP packages all non-bonded out pins should be configured as outputs after reset in order to avoid current drawn from floating inputs. Refer to Table 1-5 for affected pins.

1.7 Device Specific Information and Module Dependencies

1.7.1 PPAGE

External paging is not supported on these devices. In order to access the 16K flash blocks in the address range 0x8000–0xBFFF the PPAGE register must be loaded with the corresponding value for this range. Refer to Table 1-11 for device specific page mapping.

For all devices Flash Page 3F is visible in the 0xC000–0xFFFF range if ROMON is set. For all devices (except MC9S12GC16) Page 3E is also visible in the 0x4000–0x7FFF range if ROMHM is cleared and ROMON is set. For all devices apart from MC9S12C32 Flash Page 3D is visible in the 0x0000–0x3FFF range if ROMON is set...

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0006	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0007	MODRR	R	0	0	0	MODRR4	MODRR3	MODRR2	MODRR1	MODRR0
		W								
0x0008	PTS	R	0	0	0	0	PTS3	PTS2	PTS1	PTS0
		W								
		SCI	—	—	—	—	—	—	TXD	RXD
0x0009	PTIS	R	0	0	0	0	PTIS3	PTIS2	PTIS1	PTIS0
		W								
0x000A	DDRS	R	0	0	0	0	DDRS3	DDRS2	DDRS1	DDRS0
		W								
0x000B	RDRS	R	0	0	0	0	RDRS3	RDRS2	RDRS1	RDRS0
		W								
0x000C	PERS	R	0	0	0	0	PERS3	PERS2	PERS1	PERS0
		W								
0x000D	PPSS	R	0	0	0	0	PPSS3	PPSS2	PPSS1	PPSS0
		W								
0x000E	WOMS	R	0	0	0	0	WOMS3	WOMS2	WOMS1	WOMS0
		W								
0x000F	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0010	PTM	R	0	0	PTM5	PTM4	PTM3	PTM2	PTM1	PTM0
		W								
		MSCAN / SPI	—	—	SCK	MOSI	$\overline{SS}$	MISO	TXCAN	RXCAN
0x0011	PTIM	R	0	0	PTIM5	PTIM4	PTIM3	PTIM2	PTIM1	PTIM0
		W								
0x0012	DDRM	R	0	0	DDRM5	DDRM4	DDRM3	DDRM2	DDRM1	DDRM0
		W								
0x0013	RDRM	R	0	0	RDRM5	RDRM4	RDRM3	RDRM2	RDRM1	RDRM0
		W								
0x0014	PERM	R	0	0	PERM5	PERM4	PERM3	PERM2	PERM1	PERM0
		W								
0x0015	PPSM	R	0	0	PPSM5	PPSM4	PPSM3	PPSM2	PPSM1	PPSM0
		W								
0x0016	WOMM	R	0	0	WOMM5	WOMM4	WOMM3	WOMM2	WOMM1	WOMM0
		W								
0x0017	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0018	PTP	R	PTP7	PTP6	PTP5	PTP4	PTP3	PTP2	PTP1	PTP0
		W								
		PWM	—	—	PWM5	PWM4	PWM3	PWM2	PWM1	PWM0
0x0019	PTIP	R	PTIP7	PTIP6	PTIP5	PTIP4	PTIP3	PTIP2	PTIP1	PTIP0
		W								

= Unimplemented or Reserved

Figure 2-2. Quick Reference to PIM Registers (Sheet 2 of 3)

2.3.2.2.4 Port S Reduced Drive Register (RDRS)

Module Base + 0x000B

	7	6	5	4	3	2	1	0
R	0	0	0	0	RDRS3	RDRS2	RDRS1	RDRS0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 2-13. Port S Reduced Drive Register (RDRS)

Read: Anytime.

Write: Anytime.

Table 2-12. RDRS Field Descriptions

Field	Description
3–0 RDRS[3:0]	**Reduced Drive Port S** — This register configures the drive strength of each port S output pin as either full or reduced. If the port is used as input this bit is ignored. 0 Full drive strength at output. 1 Associated pin drives at about 1/3 of the full drive strength.

2.3.2.2.5 Port S Pull Device Enable Register (PERS)

Module Base + 0x000C

	7	6	5	4	3	2	1	0
R	0	0	0	0	PERS3	PERS2	PERS1	PERS0
W								
Reset	0	0	0	0	1	1	1	1

= Unimplemented or Reserved

Figure 2-14. Port S Pull Device Enable Register (PERS)

Read: Anytime.

Write: Anytime.

Table 2-13. PERS Field Descriptions

Field	Description
3–0 PERS[3:0]	**Reduced Drive Port S** — This register configures whether a pull-up or a pull-down device is activated, if the port is used as input or as output in wired-or (open drain) mode. This bit has no effect if the port is used as push-pull output. Out of reset a pull-up device is enabled. 0 Pull-up or pull-down device is disabled. 1 Either a pull-up or pull-down device is enabled.

NOTE

16-bit misaligned reads and writes are not allowed. If attempted, the BDM will ignore the least significant bit of the address and will assume an even address from the remaining bits.

For hardware data read commands, the external host must wait 150 bus clock cycles after sending the address before attempting to obtain the read data. This is to be certain that valid data is available in the BDM shift register, ready to be shifted out. For hardware write commands, the external host must wait 150 bus clock cycles after sending the data to be written before attempting to send a new command. This is to avoid disturbing the BDM shift register before the write has been completed. The 150 bus clock cycle delay in both cases includes the maximum 128 cycle delay that can be incurred as the BDM waits for a free cycle before stealing a cycle.

For firmware read commands, the external host should wait 44 bus clock cycles after sending the command opcode and before attempting to obtain the read data. This includes the potential of an extra 7 cycles when the access is external with a narrow bus access (+1 cycle) and / or a stretch (+1, 2, or 3 cycles), (7 cycles could be needed if both occur). The 44 cycle wait allows enough time for the requested data to be made available in the BDM shift register, ready to be shifted out.

NOTE

This timing has increased from previous BDM modules due to the new capability in which the BDM serial interface can potentially run faster than the bus. On previous BDM modules this extra time could be hidden within the serial time.

For firmware write commands, the external host must wait 32 bus clock cycles after sending the data to be written before attempting to send a new command. This is to avoid disturbing the BDM shift register before the write has been completed.

The external host should wait 64 bus clock cycles after a TRACE1 or GO command before starting any new serial command. This is to allow the CPU to exit gracefully from the standard BDM firmware lookup table and resume execution of the user code. Disturbing the BDM shift register prematurely may adversely affect the exit from the standard BDM firmware lookup table.

NOTE

If the bus rate of the target processor is unknown or could be changing, it is recommended that the ACK (acknowledge function) be used to indicate when an operation is complete. When using ACK, the delay times are automated.

Figure 6-6 represents the BDM command structure. The command blocks illustrate a series of eight bit times starting with a falling edge. The bar across the top of the blocks indicates that the BKGD line idles in the high state. The time for an 8-bit command is 8×16 target clock cycles.[1]

1. Target clock cycles are cycles measured using the target MCU's serial clock rate. See Section 6.4.6, "BDM Serial Interface," and Section 6.3.2.1, "BDM Status Register (BDMSTS)," for information on how serial clock rate is selected.

8.2 Signal Description

The ATD10B8C has a total of 12 external pins.

8.2.1 AN7 / ETRIG / PAD7

This pin serves as the analog input channel 7. It can be configured to provide an external trigger for the ATD conversion. It can be configured as general-purpose digital I/O.

8.2.2 AN6 / PAD6

This pin serves as the analog input channel 6. It can be configured as general-purpose digital I/O.

8.2.3 AN5 / PAD5

This pin serves as the analog input channel 5. It can be configured as general-purpose digital I/O.

8.2.4 AN4 / PAD4

This pin serves as the analog input channel 4. It can be configured as general-purpose digital I/O.

8.2.5 AN3 / PAD3

This pin serves as the analog input channel 3. It can be configured as general-purpose digital I/O.

8.2.6 AN2 / PAD2

This pin serves as the analog input channel 2. It can be configured as general-purpose digital I/O.

8.2.7 AN1 / PAD1

This pin serves as the analog input channel 1. It can be configured as general-purpose digital I/O.

8.2.8 AN0 / PAD0

This pin serves as the analog input channel 0. It can be configured as general-purpose digital I/O.

8.2.9 V_{RH}, V_{RL}

V_{RH} is the high reference voltage and V_{RL} is the low reference voltage for ATD conversion.

8.2.10 V_{DDA}, V_{SSA}

These pins are the power supplies for the analog circuitry of the ATD10B8C block.

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
Left Justified Result Data										
0x0010	ATDDR0H	R	BIT 9 MSB BIT 7 MSB	BIT 8 BIT 6	BIT 7 BIT 5	BIT 6 BIT 4	BIT 5 BIT 3	BIT 4 BIT 2	BIT 3 BIT 1	BIT 2 BIT 0
		W								
0x0011	ATDDR0L	R	BIT 1 u	BIT 0 u	0 0	0 0	0 0	0 0	0 0	0 0
		W								
0x0012	ATDDR1H	R	BIT 9 MSB BIT 7 MSB	BIT 8 BIT 6	BIT 7 BIT 5	BIT 6 BIT 4	BIT 5 BIT 3	BIT 4 BIT 2	BIT 3 BIT 1	BIT 2 BIT 0
		W								
0x0013	ATDDR1L	R	BIT 1 u	BIT 0 u	0 0	0 0	0 0	0 0	0 0	0 0
		W								
0x0014	ATDDR2H	R	BIT 9 MSB BIT 7 MSB	BIT 8 BIT 6	BIT 7 BIT 5	BIT 6 BIT 4	BIT 5 BIT 3	BIT 4 BIT 2	BIT 3 BIT 1	BIT 2 BIT 0
		W								
0x0015	ATDDR2L	R	BIT 1 u	BIT 0 u	0 0	0 0	0 0	0 0	0 0	0 0
		W								
0x0016	ATDDR3H	R	BIT 9 MSB BIT 7 MSB	BIT 8 BIT 6	BIT 7 BIT 5	BIT 6 BIT 4	BIT 5 BIT 3	BIT 4 BIT 2	BIT 3 BIT 1	BIT 2 BIT 0
		W								
0x0017	ATDDR3L	R	BIT 1 u	BIT 0 u	0 0	0 0	0 0	0 0	0 0	0 0
		W								
0x0018	ATDDR4H	R	BIT 9 MSB BIT 7 MSB	BIT 8 BIT 6	BIT 7 BIT 5	BIT 6 BIT 4	BIT 5 BIT 3	BIT 4 BIT 2	BIT 3 BIT 1	BIT 2 BIT 0
		W								
0x0019	ATDDR4L	R	BIT 1 u	BIT 0 u	0 0	0 0	0 0	0 0	0 0	0 0
		W								
0x001A	ATDDR5H	R	BIT 9 MSB BIT 7 MSB	BIT 8 BIT 6	BIT 7 BIT 5	BIT 6 BIT 4	BIT 5 BIT 3	BIT 4 BIT 2	BIT 3 BIT 1	BIT 2 BIT 0
		W								
0x001B	ATDDR5L	R	BIT 1 u	BIT 0 u	0 0	0 0	0 0	0 0	0 0	0 0
		W								
0x001C	ATDDR6H	R	BIT 9 MSB BIT 7 MSB	BIT 8 BIT 6	BIT 7 BIT 5	BIT 6 BIT 4	BIT 5 BIT 3	BIT 4 BIT 2	BIT 3 BIT 1	BIT 2 BIT 0
		W								
0x001D	ATDDR6L	R	BIT 1 u	BIT 0 u	0 0	0 0	0 0	0 0	0 0	0 0
		W								

= Unimplemented or Reserved

Figure 8-2. ATD Register Summary (Sheet 2 of 4)

9.3.2.10 Reserved Register (FORBYP)

NOTE

This reserved register is designed for factory test purposes only, and is not intended for general user access. Writing to this register when in special modes can alter the CRG's functionality.

Module Base + 0x0009

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 9-13. Reserved Register (FORBYP)

Read: always read 0x0000 except in special modes

Write: only in special modes

9.3.2.11 Reserved Register (CTCTL)

NOTE

This reserved register is designed for factory test purposes only, and is not intended for general user access. Writing to this register when in special test modes can alter the CRG's functionality.

Module Base + 0x000A

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 9-14. Reserved Register (CTCTL)

Read: always read 0x0080 except in special modes

Write: only in special modes

13.4.1 Data Format

The SCI uses the standard NRZ mark/space data format illustrated in Figure 13-10 below.

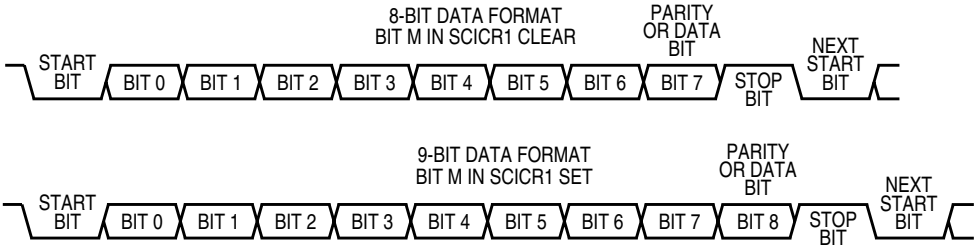


Figure 13-10. SCI Data Formats

Each data character is contained in a frame that includes a start bit, eight or nine data bits, and a stop bit. Clearing the M bit in SCI control register 1 configures the SCI for 8-bit data characters.A frame with eight data bits has a total of 10 bits. Setting the M bit configures the SCI for nine-bit data characters. A frame with nine data bits has a total of 11 bits

Table 13-8. Example of 8-Bit Data Formats

Start Bit	Data Bits	Address Bits	Parity Bits	Stop Bit
1	8	0	0	1
1	7	0	1	1
1	7	1[(1)]	0	1

1. The address bit identifies the frame as an address character. See Section 13.4.4.6, “Receiver Wakeup”.

When the SCI is configured for 9-bit data characters, the ninth data bit is the T8 bit in SCI data register high (SCIDRH). It remains unchanged after transmission and can be used repeatedly without rewriting it. A frame with nine data bits has a total of 11 bits.

Table 13-9. Example of 9-Bit Data Formats

Start Bit	Data Bits	Address Bits	Parity Bits	Stop Bit
1	9	0	0	1
1	8	0	1	1
1	8	1[(1)]	0	1

1. The address bit identifies the frame as an address character. See Section 13.4.4.6, “Receiver Wakeup”.

13.4.4.2 Character Reception

During an SCI reception, the receive shift register shifts a frame in from the **Rx input** signal. The SCI data register is the read-only buffer between the internal data bus and the receive shift register.

After a complete frame shifts into the receive shift register, the data portion of the frame transfers to the SCI data register. The receive data register full flag, RDRF, in SCI status register 1 (SCISR1) becomes set, indicating that the received byte can be read. If the receive interrupt enable bit, RIE, in SCI control register 2 (SCICR2) is also set, the RDRF flag generates an RDRF interrupt request.

13.4.4.3 Data Sampling

The receiver samples the **Rx input** signal at the RT clock rate. The RT clock is an internal signal with a frequency 16 times the baud rate. To adjust for baud rate mismatch, the RT clock (see Figure 13-13) is re-synchronized:

- After every start bit
- After the receiver detects a data bit change from logic 1 to logic 0 (after the majority of data bit samples at RT8, RT9, and RT10 returns a valid logic 1 and the majority of the next RT8, RT9, and RT10 samples returns a valid logic 0)

To locate the start bit, data recovery logic does an asynchronous search for a logic 0 preceded by three logic 1s.When the falling edge of a possible start bit occurs, the RT clock begins to count to 16.

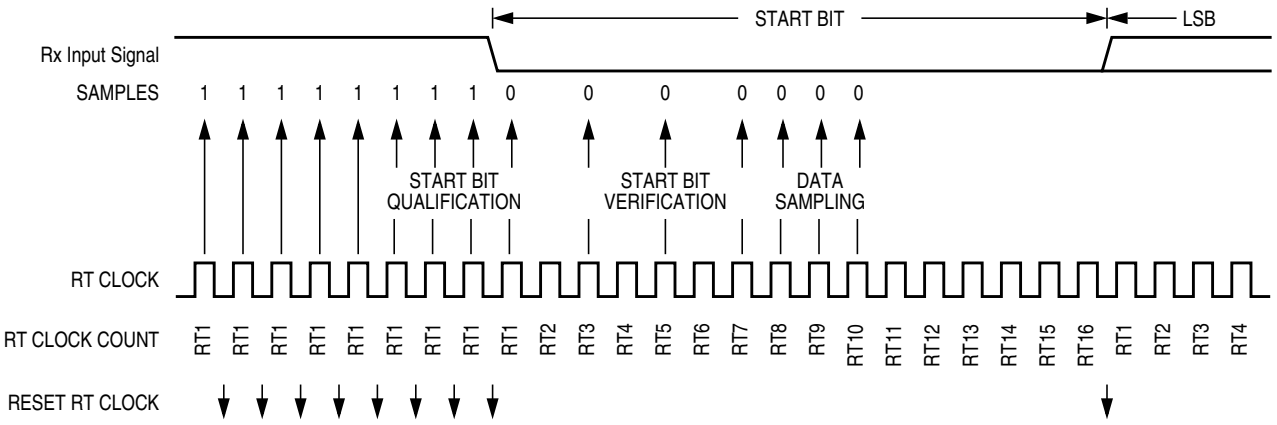


Figure 13-13. Receiver Data Sampling

To verify the start bit and to detect noise, data recovery logic takes samples at RT3, RT5, and RT7. Table 13-11 summarizes the results of the start bit verification samples.

Table 13-11. Start Bit Verification

RT3, RT5, and RT7 Samples	Start Bit Verification	Noise Flag
000	Yes	0
001	Yes	1
010	Yes	1
011	No	0

Figure 13-18 shows a burst of noise near the beginning of the start bit that resets the RT clock. The sample after the reset is low but is not preceded by three high samples that would qualify as a falling edge. Depending on the timing of the start bit search and on the data, the frame may be missed entirely or it may set the framing error flag.

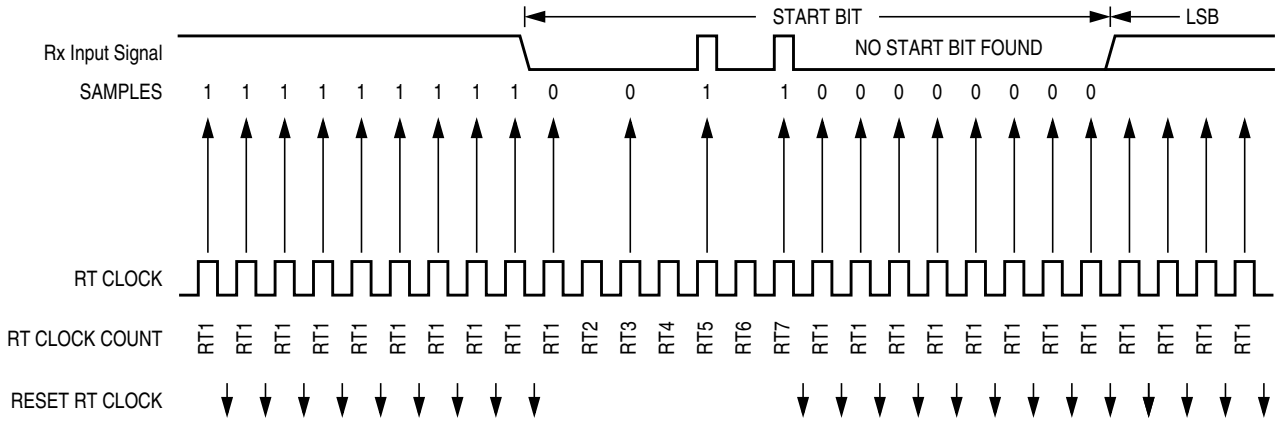


Figure 13-18. Start Bit Search Example 5

In Figure 13-19, a noise burst makes the majority of data samples RT8, RT9, and RT10 high. This sets the noise flag but does not reset the RT clock. In start bits only, the RT8, RT9, and RT10 data samples are ignored.

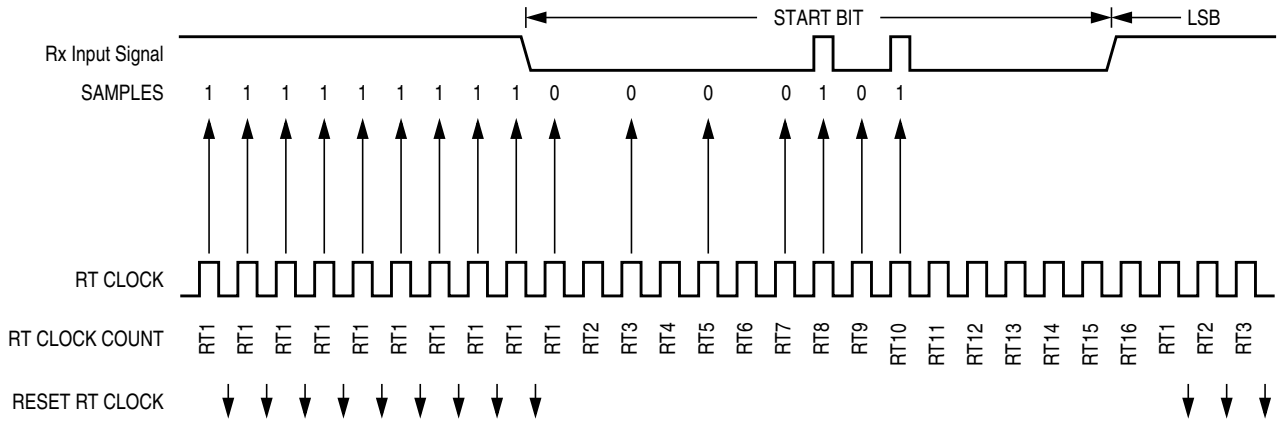


Figure 13-19. Start Bit Search Example 6

14.3.2.4 SPI Status Register (SPISR)

Module Base 0x0003

	7	6	5	4	3	2	1	0
R	SPIF	0	SPTEF	MODF	0	0	0	0
W								
Reset	0	0	1	0	0	0	0	0

= Unimplemented or Reserved

Figure 14-6. SPI Status Register (SPISR)

Read: anytime

Write: has no effect

Table 14-8. SPISR Field Descriptions

Field	Description
7 SPIF	**SPIF Interrupt Flag** — This bit is set after a received data byte has been transferred into the SPI Data Register. This bit is cleared by reading the SPISR register (with SPIF set) followed by a read access to the SPI Data Register. 0 Transfer not yet complete 1 New data copied to SPIDR
5 SPTEF	**SPI Transmit Empty Interrupt Flag** — If set, this bit indicates that the transmit data register is empty. To clear this bit and place data into the transmit data register, SPISR has to be read with SPTEF = 1, followed by a write to SPIDR. Any write to the SPI Data Register without reading SPTEF = 1, is effectively ignored. 0 SPI Data register not empty 1 SPI Data register empty
4 MODF	**Mode Fault Flag** — This bit is set if the $\overline{SS}$ input becomes low while the SPI is configured as a master and mode fault detection is enabled, MODFEN bit of SPICR2 register is set. Refer to MODFEN bit description in Section 14.3.2.2, “SPI Control Register 2 (SPICR2).” The flag is cleared automatically by a read of the SPI Status Register (with MODF set) followed by a write to the SPI Control Register 1. 0 Mode fault has not occurred. 1 Mode fault has occurred.

14.3.2.5 SPI Data Register (SPIDR)

Module Base 0x0005

	7	6	5	4	3	2	1	0
R W	Bit 7	6	5	4	3	2	2	Bit 0
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 14-7. SPI Data Register (SPIDR)

Read: anytime; normally read only after SPIF is set

16.3.2 Register Descriptions

The following paragraphs describe, in address order, all the VREG3V3V2 registers and their individual bits.

16.3.2.1 VREG3V3V2 — Control Register (VREGCTRL)

The VREGCTRL register allows to separately enable features of VREG3V3V2.

Module Base + 0x0000

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	LVDS	LVIE	LVIF
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 16-2. VREG3V3 — Control Register (VREGCTRL)

Table 16-3. MCCTL1 Field Descriptions

Field	Description
2 LVDS	**Low-Voltage Detect Status Bit** — This read-only status bit reflects the input voltage. Writes have no effect. 0 Input voltage V_{DDA} is above level V_{LVID} or RPM or shutdown mode. 1 Input voltage V_{DDA} is below level V_{LVIA} and FPM.
1 LVIE	**Low-Voltage Interrupt Enable Bit** 0 Interrupt request is disabled. 1 Interrupt will be requested whenever LVIF is set.
0 LVIF	**Low-Voltage Interrupt Flag** — LVIF is set to 1 when LVDS status bit changes. This flag can only be cleared by writing a 1. Writing a 0 has no effect. If enabled (LVIE = 1), LVIF causes an interrupt request. 0 No change in LVDS bit. 1 LVDS bit has changed.

NOTE

On entering the Reduced Power Mode the LVIF is not cleared by the VREG3V3V2.

16.4 Functional Description

Block VREG3V3V2 is a voltage regulator as depicted in Figure 16-1. The regulator functional elements are the regulator core (REG), a low-voltage detect module (LVD), a power-on reset module (POR) and a low-voltage reset module (LVR). There is also the regulator control block (CTRL) which represents the interface to the digital core logic but also manages the operating modes of VREG3V3V2.

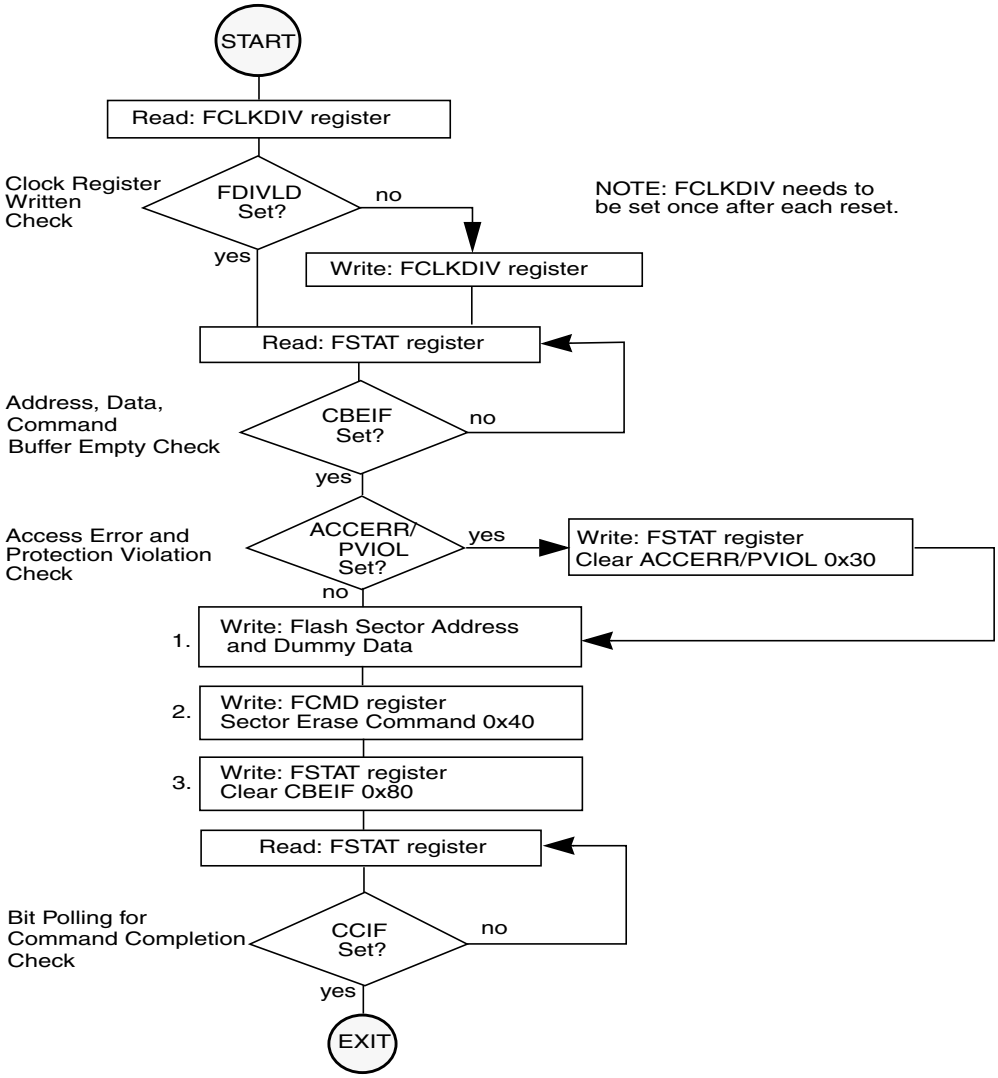


Figure 17-24. Example Sector Erase Command Flow

18.3.2.4 Flash Configuration Register (FCNFG)

The FCNFG register enables the Flash interrupts and gates the security backdoor key writes.

Module Base + 0x0003

	7	6	5	4	3	2	1	0
R	CBEIE	CCIE	KEYACC	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 18-7. Flash Configuration Register (FCNFG)

CBEIE, CCIE, and KEYACC are readable and writable while remaining bits read 0 and are not writable. KEYACC is only writable if the KEYEN bit in the FSEC register is set to the enabled state (see Section 18.3.2.2).

Table 18-7. FCNFG Field Descriptions

Field	Description
7 CBEIE	**Command Buffer Empty Interrupt Enable** — The CBEIE bit enables the interrupts in case of an empty command buffer in the Flash module. 0 Command Buffer Empty interrupts disabled 1 An interrupt will be requested whenever the CBEIF flag is set (see Section 18.3.2.6)
6 CCIE	**Command Complete Interrupt Enable** — The CCIE bit enables the interrupts in case of all commands being completed in the Flash module. 0 Command Complete interrupts disabled 1 An interrupt will be requested whenever the CCIF flag is set (see Section 18.3.2.6)
5 KEYACC	**Enable Security Key Writing**. 0 Flash writes are interpreted as the start of a command write sequence 1 Writes to the Flash array are interpreted as a backdoor key while reads of the Flash array return invalid data

18.3.2.5 Flash Protection Register (FPROT)

The FPROT register defines which Flash sectors are protected against program or erase.

Module Base + 0x0004

	7	6	5	4	3	2	1	0
R	FPOPEN	NV6	FPHDIS	FPHS1	FPHS0	FPLDIS	FPLS1	FPLS0
W								
Reset	F	F	F	F	F	F	F	F

Figure 18-8. Flash Protection Register (FPROT)

The FPROT register is readable in normal and special modes. FPOPEN can only be written from a 1 to a 0. FPLS[1:0] can be written anytime until FPLDIS is cleared. FPHS[1:0] can be written anytime until

18.4.1.3.3 Sector Erase Command

The sector erase operation will erase all addresses in a 512 byte sector of the Flash array using an embedded algorithm.

An example flow to execute the sector erase operation is shown in Figure 18-24. The sector erase command write sequence is as follows:

1. Write to a Flash array address to start the command write sequence for the sector erase command. The Flash address written determines the sector to be erased while MCU address bits [8:0] and the data written are ignored.
2. Write the sector erase command, 0x40, to the FCMD register.
3. Clear the CBEIF flag in the FSTAT register by writing a 1 to CBEIF to launch the sector erase command.

If a Flash sector to be erased is in a protected area of the Flash array, the PVIOL flag in the FSTAT register will set and the sector erase command will not launch. Once the sector erase command has successfully launched, the CCIF flag in the FSTAT register will set after the sector erase operation has completed unless a new command write sequence has been buffered.

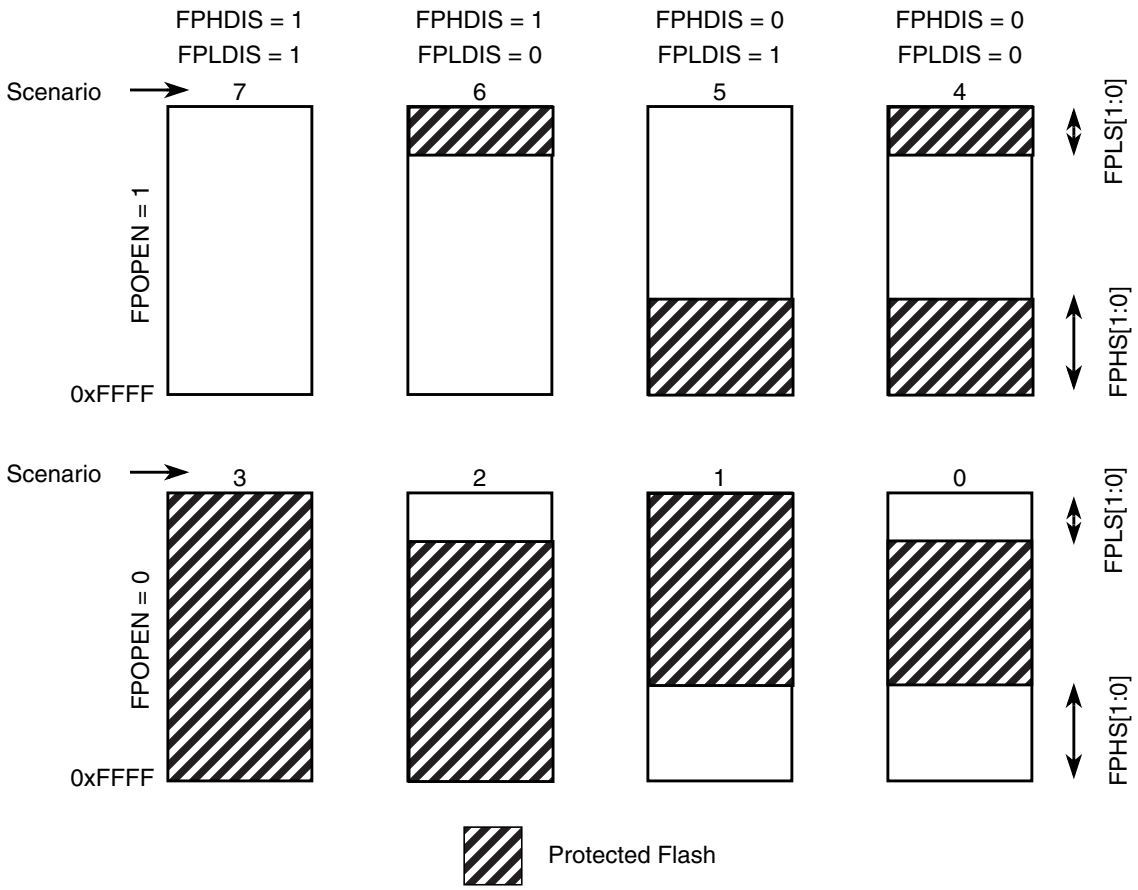


Figure 20-11. Flash Protection Scenarios

20.3.2.5.1 Flash Protection Restrictions

The general guideline is that protection can only be added, not removed. All valid transitions between Flash protection scenarios are specified in Table 20-13. Any attempt to write an invalid scenario to the FPROT register will be ignored and the FPROT register will remain unchanged. The contents of the FPROT register reflect the active protection scenario.

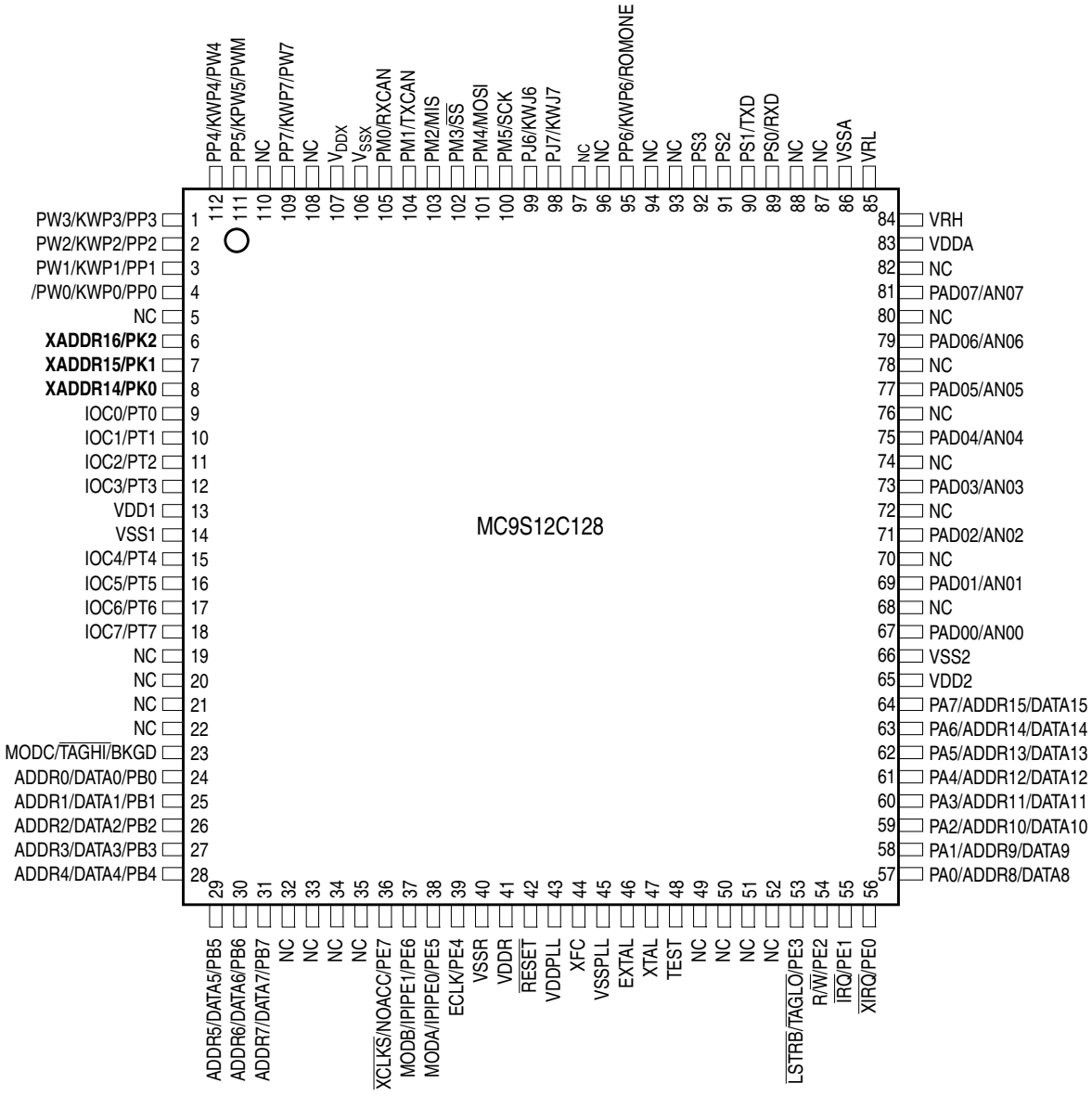
Table 20-13. Flash Protection Scenario Transitions

From Protection Scenario	To Protection Scenario[1]							
	0	1	2	3	4	5	6	7
0	X	X	X	X				
1		X		X				
2			X	X				
3				X				
4				X	X			
5			X	X	X	X		

Appendix B
Emulation Information

B.1 General

For emulation, external addressing of a 128K memory map is required. This is provided in a 112 LQFP package version of the MC9S12C128 which includes the 3 necessary extra external address bus signals via Port K. This package version is for emulation only and not provided as a general production package.



Signals shown in **Bold** are available only in the 112 Pin Package. Pins marked "NC" are not connected

Figure B-1. Pin Assignments in 112-Pin LQFP