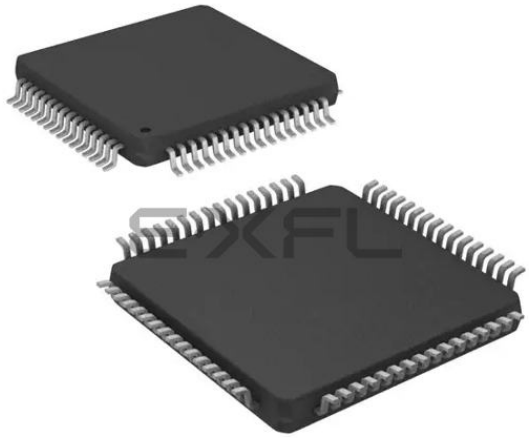

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

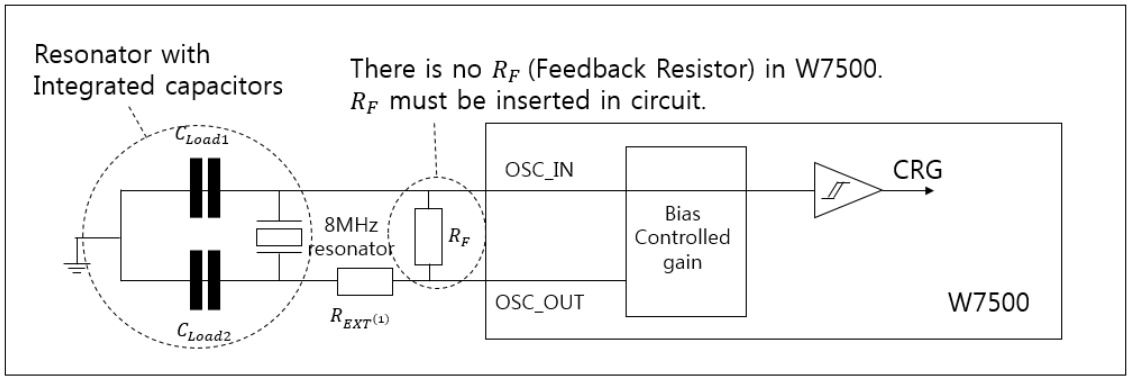
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	Ethernet/TCP/IP, I²C, SSP, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	34
Program Memory Size	128KB (32K x 32)
Program Memory Type	FLASH
EEPROM Size	6K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 9x12b
Oscillator Type	External, Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/wiznet/w7500p-s2e

Table of Contents

3.6.1 External Oscillator Clock

The External oscillator clock (OCLK) can be supplied with a 8 to 24 MHz crystal/ceramic resonator oscillator. In the Typical application, Figure 3, R_F must be inserted in External oscillator clock circuit. In W7500x, there is no supported R_F for External oscillator clock (see Figure 3).
For C_{Load1} and C_{Load2}, it is recommended to use external ceramic capacitors in the 5 pF to 25 pF range(typ.) and are usually the same size, designed for application, and selected to match the requirements of the crystal or resonator (see Figure 3).
Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).



[1] R_{EXT} value depends on the crystal characteristics

Figure 3 Typical application with an 8 MHz crystal

3.6.2 RC oscillator clock

RC oscillator clock (RCLK) signal is generated from an internal 8MHz RC oscillator.
RC oscillator has the advantage of providing a clock source at low cost (no external components). However the RC oscillator is less accurate than the external crystal or ceramic resonator.

Accuracy : 1% at T_A= 25ºC (User don't need to calibration)

3.6.3 PLL

The internal PLL can be used to multiply the External Oscillator Clock (OCLK) or RC Oscillator Clock (RCLK). PLL input can be selected by register.

PLL output clock can be generated by following the equations below.

- FOUT = FIN x M / N x 1 / OD
-

Where:

- M = M[5] x 2^5 + M[4] x 2^4 + M[3] x 2^3 + M[2] x 2^2 + M[1] x 2 + M[0] x 1
- N = N[5] x 2^5 + N[4] x 2^4 + N[3] x 2^3 + N[2] x 2^2 + N[1] x 2 + N[0] x 1
- OD = $2^{(2 \times OD[1])} \times 2^{(1 \times OD[0])}$

3.6.4 Generated clock

Each generated clock source can be selected among 3 clock source as independent by each clock source select register.

- PLL output clock (MCLK)
- Internal 8MHz RC oscillator clock (RCLK)
- External oscillator clock (8MHz ~ 24MHz) (OCLK)

[1] R_{EXT} value depends on the crystal characteristics

- Each generated clock has own prescaler which can be selected individually by each prescale value register.
- FCLK, ADCCLK, SSPCLK, UARTCLK : 1/1, 1/2, 1/4, 1/8
- TIMCLK0, TIMCLK1, PWMCLK0 – PWMCLK7, RTCCLK, WDOGCLK : 1/1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128

3.7 Interrupts and events

3.7.1 Nested vectored interrupt controller (NVIC)

The W7500x family embeds a nested vectored interrupt controller able to handle up to 32 maskable interrupt channels (not including the 16 interrupt lines of Cortex®-M0) and 4 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

3.7.2 Event controller

The W7500x family is able to handle internal events in order to wake up the core(WFE).
The wakeup event can be generated by

- When after DMA process finished (DMA_DONE)

3.8 Tcp/ip offload engine (TOE)

The TCP/IP Core Offload Engine (TOE) is a Hardwired TCP/IP embedded Ethernet controller that provides easier Internet connection to embedded systems. TOE enables users to have Internet connectivity in their applications by using the TCP/IP stack.

WIZnet's Hardwired TCP/IP is the market-proven technology that supports TCP, UDP, IPv4, ICMP, ARP, IGMP, and PPPoE protocols. TOE embeds the 32Kbyte internal memory buffer for the Ethernet packet processing. Using TOE allows users to implement the Ethernet application by adding the simple socket program. It's faster and easier than using any other Embedded Ethernet solutions. 8 independent hardware sockets can be used simultaneously.

TOE also provides WOL (Wake on LAN) to reduce power consumption of the system.

- Supports Hardwired TCP/IP Protocols : TCP, UDP, ICMP, IPv4, ARP, IGMP, PPPoE
- Supports 8 independent sockets simultaneously
- Supports Power down mode
- Supports Wake on LAN over UDP
- Internal 32Kbytes Memory for TX/RX Buffers
- Not supports IP Fragmentation

3.9 General-purpose inputs/outputs (GPIOs)

The GPIO(General-Purpose I/O Port) is composed of three physical GPIO blocks, each corresponding to an individual GPIO port(PORT A, PORT B and PORT C). The GPIO supports up to 34 programmable input/output pins, depending on the peripherals being used.

- The GPIO peripheral consists the following features.
- GPIO_DATAOUT can SET/CLEAR by the SET register and CLEAR register. (1 for set and 0 for clear)
- Mask registers allow treating sets of port bits as a group leaving other bits unchanged.
- Up to 34 GPIOs depending on configuration
- Programmable control for GPIO interrupts
- Interrupt generation masking
- Edge-triggered on rising, falling~~, or both~~

Refer to 'Reference Manual' for more details about each register.

3.10 Pad controller (PADCON)

Pads of W7500x are controllable. User can control pad's characteristic.

W7500x has digital I/O pads and digital/analog mux I/O pads
Controllable characteristics of pads are pull-up, pull-down, driving strength, input enable, and CMOS/Schmitt trigger input buffer
Each pad can be controlled individually by register.

Figure 4 shows the function schematic of digital I/O pad of W7500x.

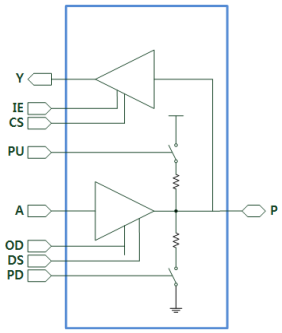


Figure 4. function schematic of digital I/O pad

Figure 5 shows the function schematic of digital/analog mux IO pad of W7500x

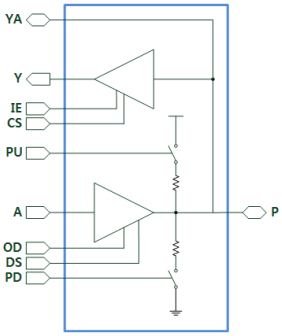


Figure 5. function schematic of digital/analog mux IO pad

3.12 External interrupt (EXTI)

Each functional pads are connected to the external interrupt(EXTINT) source.

- All functional pads can be used as an external interrupt source regardless of any set of pad function.
- External Interrupt controller has the following functions and can be controlled by registers.
- Interrupt mask (enable or disable, default : disable)
- Interrupt polarity (rising or falling, default : rising)

All pads are connected to the control register individually. (External interrupt mask register and External Interrupt polarity register)

External interrupt working as following expression:
- Each pad interrupt = Interrupt mask & (Interrupt polarity ^ Pad input)
- EXTINT = any Each pad interrupt

Figure 6 shows the External Interrupt diagram.

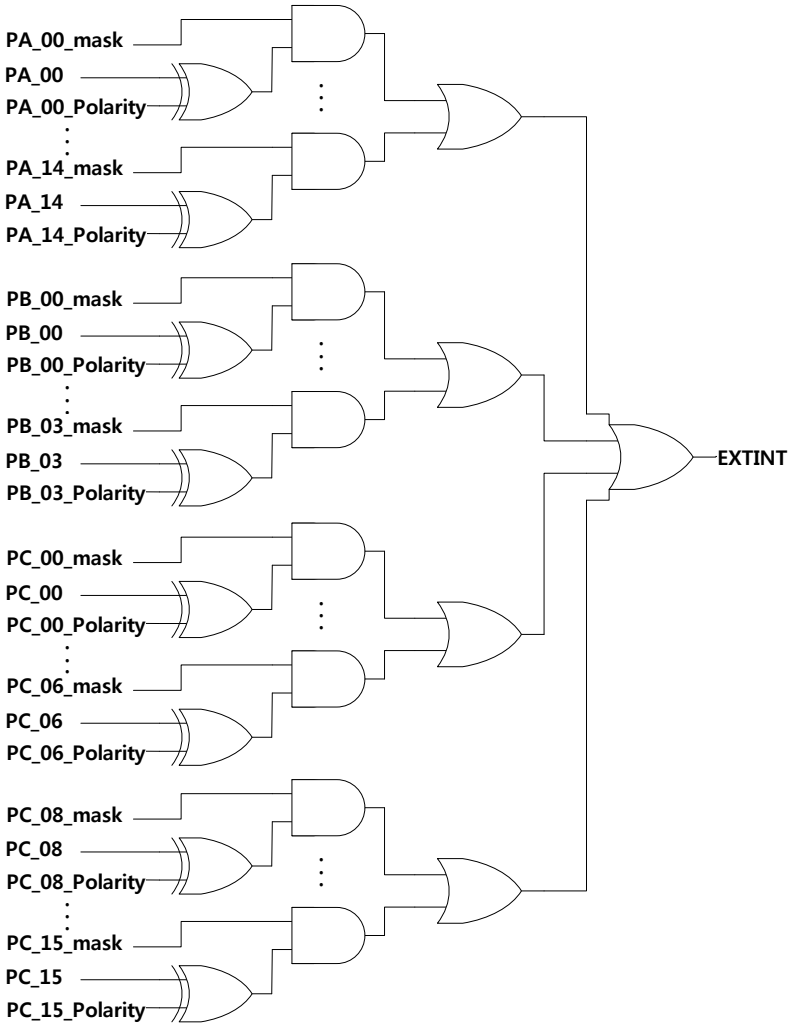


Figure 6. External Interrupt diagram

3.13 Direct memory access controller (DMA)

Direct memory access (DMA) is used in order to provide high-speed data transfer between peripherals and memory as well as memory to memory. Data can be quickly moved by DMA without any CPU actions. This keeps CPU resources free for other operations.
The DMA controller has up to 6 channels in total, each dedicated to managing memory access requests from one or more peripherals. It has an arbiter for handling the priority between DMA requests. For more details, refer to “PrimeCell® µDMA Controller (PL230)” from the Technical Reference Manual

- 6 channels
- Each channel is connected to dedicated hardware DMA requests and software trigger is also supported on each channel.
- Priorities between requests from the DMA channels are software programmable (2 levels consisting of high, default)
- Memory-to-memory transfer (software request only)
- TCP/IP-to-memory transfer (software request only)
- SPI/UART-to-memory transfer (hardware request and software request)
- Access to Flash, SRAM, APB and AHB peripherals as source and destination

DMA request mapping
The hardware requests from the peripherals (UART0, UART1, SSP0, SSP1) are simply connected to the DMA. Refer to Table 5 which lists the DMA requests for each channel.

Table 5 Summary of the DMA requests for each channel

	Channel 1	Channel 2	Channel 3	Channel 4	Channel 5	Channel 6
Hardware Request	SSP0_TX SSP0_RX	SSP1_TX SSP1_RX	UART0_TX UART0_RX	UART1_TX UART1_RX	NONE	NONE
Software Request(1)	Support	Support	Support	Support	Support	Support

Software request is the only way to use DMA for memory-to-memory or TCP/IP-to-memory.

3.14 Analog to digital converter (ADC)

ADC is a 12bit analog-to-digital converter. It has up to 9 multiplexed channels allowing it to measure signals from 8 externals and 1 internal source.
ADC of various channels can be performed in single mode. The result of the ADC is stored in 12 bit register.

- 12bit configuration resolution
- Conversion time : Max 10MHz (Sampling time can be programmable)
- 8 channel for external analog inputs
- 1 channel for internal LDO(1.5v) voltage
- Start of conversion can be initiated by software.
- Convert selected inputs once per trigger.
- Interrupt generation at the end of conversion.

3.15 Timers and watchdogs

3.15.1 System tick timer

System tick timer(SysTick) is part of the ARM Cortex-M0 core

- Simple 24bit timer.
- Clocked internally by the system clock or the system clock/2.

The SysTick timer is an integral part of Cortex-M0. The SysTick timer is intended to generated a fixed 10 millisecond interrupt for use by an operating system or other system management software.

Since the SysTick timer is a part of the Cortex-M0, it facilitates porting of software by providing a standard timer that is available on Cortex-M0 based devices.

The SysTick timer can be used for :

- An RTOS tick timer which fires at a programmable rate (for example 100 Hz) and invokes a SysTick routine.
- A high-speed alarm timer using the core clock.
- A simple counter. Software can use this to measure time to completion and time used.
- An internal clock source control based on missing/meeting durations. The COUNTFLAG bit-field in the control and status register can be used to determine if an action completed within a set duration, as part of a dynamic clock management control loop.

3.15.2 Pulse-Width Modulation (PWM)

The PWM consists a 8-channel 32-bit Timer/Counter driven by a programmable prescaler. The function of the PWM is based on the basic Timer. Each timer and counter runs independently.

The PWM can be used to control the width of the pulse, formally the pulse duration, to generate output waveform or to count the counter triggered by external input.

- Counter or Timer operation can use the peripheral clock, external clock source, or one of the capture inputs as the clock source.
- Eight independent 32-bit Timer/Counter driven by a programmable 6 bits prescaler runs as the PWM or standard timer if the PWM mode is not enabled.
- Eight PWM output waveforms.
- Each of Timer/Counter can have different or same clock source.
- Counter or timer operation.
- Eight capture registers that can take the timer value when an external input signal. A capture event can generate an interrupt signal optionally.
- 32-bit match register and limit register.

3.15.3 Dual timers

The dual timer consists two programmable 32-bit or 16-bit Free-running counters(FRCs) that can generate interrupts when they reach 0. There are two dual timers and 4 FRCs. One dual timers has one interrupt handler, resulting in two interrupts of timers. Also one dual timer has one clock but two clock enable signals. Users can select one repetition modes one-shot or wrapping mode, and wrapping mode consists free-running and periodic mode. Two FRCs are one set so two FRCs has one clock, reset, and interrupt but each FRC has an individual clock enable.

- One dual timer has two Free-Running Counters(FRCs).
- One dual timer has one interrupt handler and one clock.

3.17 Universal asynchronous receiver/transmitter (UART)

The device embeds three universal asynchronous receivers/transmitters (UART0, UART1, UART2) which communicate at speeds of up to 3 Mbit/s.
The UART supports synchronous one-way communication, half-duplex single wire communication, and UART0,1 supports multiprocessor communications(CTS/RTS) but UART2 unsupported multiprocessor communications UART2 is called the SUART(Simple UART).

- Serial-to-parallel conversion on data received from a peripheral device
- Parallel-to-serial conversion on data transmitted to the peripheral device
- Data size of 5,6,7 and 8 its
- One or two stop bits
- Even, odd, stick, or no-parity bit generation and detection
- Support of hardware flow control
- Programmable FIFO disabling for 1-byte depth.
- Programmable use of UART or IrDA SIR input/output
- False start bit detection

UART bidirectional communication requires a minimum of two pins: RX, TX
The frame are comprised of:

- An Idle Line prior to transmission or reception
- A start bit
- A data word (8 or 9 bits) least significant bit first
- 1, 1.5, 2 Stop bits indicating that the frame is complete
- The USART interface uses a baud rate generator
- A status register (UART1_RISR)
- data registers (UART1DR)
- A baud rate register (UART1_IBRD,UART1_FBRD)

3.18 Synchronous Serial Port (SSP)

The SSP block is an IP provided by ARM (PL022 “PrimeCell® Synchronous Serial Port”).
Additional details about its functional blocks may be found in “ARM PrimeCell® Synchronous Serial Port (PL022) Technical Reference Manual”.

- The SSP is a master or slave interface that enables synchronous serial communication with slave or master peripherals having one of the following:
- A MOTOROLA SPI-compatible interface
- A TEXAS INSTRUMENTS synchronous serial interface
- A National Semiconductor MICROWIRE® interface.

- The SPI interface operates as a master or slave interface. It supports bit rates up to 20 MHz in master mode and up to 4 MHz in slave mode.
- Parallel-to-serial conversion on data written to an internal 16-bit wide, 8-location deep transmit FIFO
- Serial-to-parallel conversion on received data, buffering it in a 16-bit wide, 8-location deep receive FIFO
- Programmable data frame size from 4 to 16 bits
- Programmable clock bit rate and prescaler. The input clock may be divided by a factor of 2 to 254 in steps of two to provide the serial output clock
- Programmable clock phase and polarity.

3.19 Random number generator (RNG)

RNG is a 32bit random number generator. RNG generates power on random number when power on reset. RNG can run/stop by software. RNG seed value and polynomial of RNG can be modified by software.

- 32bit pseudo random number generator
- Formula of pseudo random number generator (polynomial) can be modified.
- Seed value of random generator can be modified.
- Support power on reset random value.
- Random value can be obtains by control start/stop by software.

4 Pinout and descriptions

4.1 Pin layout

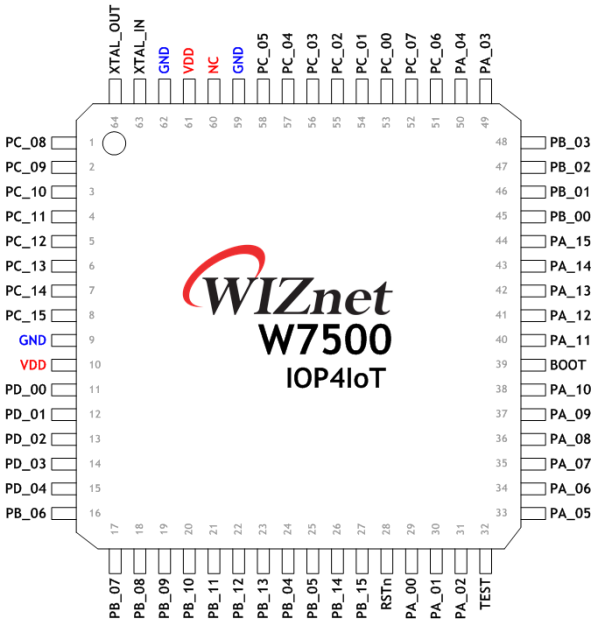


Figure 7 W7500 pin layout

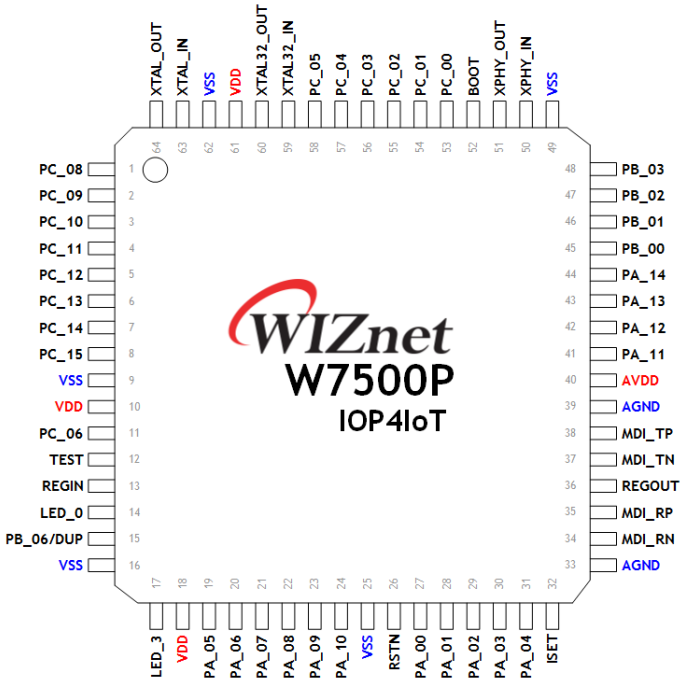


Figure 8 W7500P pin layout

PIN No	Symbol	Type	Function			
			Main Function	2nd Function	3rd Function	4th Function
48	PB_03	IO	MOSI1	GPIO2_3	U_RXD0	
49	PA_03	IO	SWCLK	GPIO1_3		PWM0/CAP0
50	PA_04	IO	SWDIO	GPIO1_4		PWM1/CAP1
51	PC_06	IO	GPIO3_6	GPIO3_6	U_TXD2	
52	PC_07	IO	GPIO3_7	GPIO3_7	U_RXD2	
53	PC_00	IO	U_CTS1	GPIO3_0	PWM0/CAP0	
54	PC_01	IO	U_RTS1	GPIO3_1	PWM1/CAP1	
55	PC_02	IO	U_TXD1	GPIO3_2	PWM2/CAP2	
56	PC_03	IO	U_RXD1	GPIO3_3	PWM3/CAP3	
57	PC_04	IO	SCL1	GPIO3_4	PWM4/CAP4	
58	PC_05	IO	SDA1	GPIO3_5	PWM5/CAP5	
59	GND	GND	GND			
60	NC	NC	NC			
61	VDD	PWR	VDD			
62	GND	GND	GND			
63	XTAL_IN	I	Xtal in			
64	XTAL_OUT	O	Xtal out			

5 Electrical characteristics

5.1 Absolute maximum ratings

These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

5.2 Voltage Characteristics

Table 9 shows the voltage characteristics of W7500x.

Table 9 Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD}-V_{SS}	Main supply voltage (VDD)	-0.3	3.6	V
V_{IN}	Input voltage on IO pins	VSS – 0.3	3.6	V
S_{VDDH}	I/O Power on slope	5V/Sec	1V/uSec	-
ΔV_{DD}	Variations between difference VDD power pins		50	mV
ΔV_{SS}	Variations between different ground pins		50	mV

5.3 Current Characteristics

Table 10 shows the current characteristics of W7500x.

Table 10 Current characteristics

Symbol	Ratings	Max	Unit
I_{VDD_SUM}	Total current into sum of all VDD power lines (source)	100	mA
I_{VDD}	Maximum current into each ADD power pin (source)	90	mA
I_{IO_PAD}	Total output current sunk by sum of all IOs and control pins	75	mA
I_{INJ_PAD}	Single pin input injected current	±10	mA
I_{INJ_SUM}	Sum of all input injected current	±50	mA

5.6 Supply Current Characteristics

Normal operation

Table 13 shows the Normal operation supply current.

Table 13 Normal operation supply current

Symbol	Parameter	Conditions1	Condition2	Typ	Unit
I_{DD_NOR}	Supply current	Active mode; code While(1) {} Executed from flash memory	System clock = 10MHz	6.14 (52.14) (1) (22.14) (2)	mA
			System clock = 20MHz	8.82 (54.82) (1) (24.82) (2)	mA
			System clock = 40MHz	14.09 (60.09) (1) (30.09) (2)	mA

(1) When PHY Normal mode, W7500P Internal PHY power consumption is 46mA MAX.

(2) When PHY Power down mode, W7500P Internal PHY power consumption is 16mA MAX.

Sleep mode

Table 14 shows the Normal operation supply current.

Table 14 Sleep mode supply current

Symbol	Parameter	Conditions1	Condition2	Typ	Unit
I_{DD_SLP}	Supply current	After enter sleep mode All peripheral clocks ON (same as system clock)	System clock = 10MHz	3.51 (49.51) (1) (19.51) (2)	mA
			System clock = 20MHz	5.65 (51.65) (1) (21.65) (2)	mA
			System clock = 40MHz	9.61 (55.61) (1) (25.61) (2)	mA

(3) When PHY Normal mode, W7500P Internal PHY power consumption is 46mA MAX.

(4) When PHY Power down mode, W7500P Internal PHY power consumption is 16mA MAX.

Deep sleep mode

Table 15 shows the deep sleep mode operation supply current.

Table 15 Deep sleep mode supply current

Symbol	Parameter	Conditions1	Condition2	Typ	Unit
I_{DD_DSLP}	Supply current	After enter deep sleep mode All peripheral clocks OFF	-	2.49 (48.49) (1) (18.49) (2)	mA

(5) When PHY Normal mode, W7500P Internal PHY power consumption is 46mA MAX.

(6) When PHY Power down mode, W7500P Internal PHY power consumption is 16mA MAX.

5.7 I/O PAD Characteristics

DC Specification
Table 16 shows the DC specification of W7500x I/O PAD.

Table 16 DC specification of PAD

Symbol	Parameter	Conditions	Min	Max	Unit
VIH	I/O Input high voltage		2.145		V
VIL	I/O Input low voltage			1.155	V
V_{HYS}	Schmitt trigger hysteresis		0.33		V
IIH	I/O Input high current			1	uA
IIL	I/O Input low current		-1		uA
VOH	I/O Output high voltage	High driving strength Iload = 6mA Low driving strength Iload = 3mA	2.5		V
VOL	I/O Output low voltage	High driving strength Iload = 6mA Low driving strength Iload = 3mA		0.5	V
R_{pup} R_{pdn}	Pull-up /Pull-down resistor		20	100	KOhm

Flash memory
Table 17 shows the flash memory reliability characteristics of W7500x

Table 17 Flash memory Reliability Characteristics

Symbol	Parameter	Min	Unit
N_{END}	Sector Endurance	10,000	Cycles
T_{DR}	Data Retention	10	Years

5.8 Electrical Sensitivity Characteristics

Electostatic discharge (ESD)
Table 18 shows the ESD information of W7500x

Table 18 Electrostatic discharge (ESD)

Symbol	Parameter	Test Method	Min	Max	Unit
$V_{ESD(HBM)}$	Electostatic discharge (Human body model)	AEC-Q100-002	±2000	-	V
$V_{ESD(CDM)}$	Electostatic discharge (Charge device model)	AEC-Q100-011	±500	-	V

Static latch-up
Table 19 shows the Static latch-up information of W7500x

Table 19 Static latch-up

Symbol	Parameter	Test Method	Min	Max	Unit
I_{LAT}	Latch up current at 125℃ ambient temperature	AEC-Q100-004	±100	-	V

5.9 Reset & PLL Characteristics

PLL Electrical characteristics
Table 20 shows the PLL characteristics of W7500x

Table 20 PLL electrical characteristics

Symbol	Parameter	Min	Max	Unit
t_d	RSTn to PD delay time	5	-	us
t_{rst}	Reset pulse width	2	-	us
t_{lock}	Lock time	-	0.2	ms

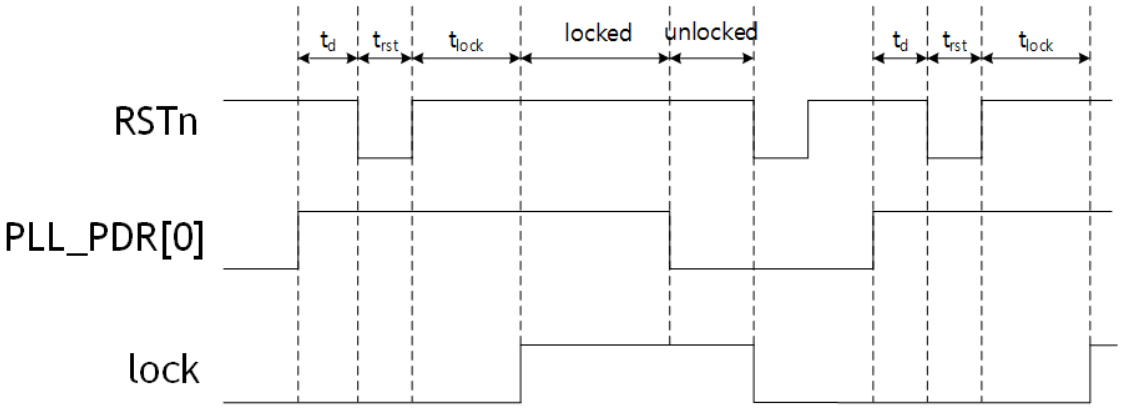


Figure 9 Power Down operation Timing Sequence for PLL

Notice:

PLL_PDR[0] is LSB of PLL_PDR. please refer from Reference Manual.

lock signal is internal signal.

1, t_d is the RSTn to PLL_PDR[0] delay time, which need larger than 5us.

2, t_{rst} is the reset pulse width, which need larger than 2us.

3, t_{lock} is the lock time, which is less than 0.2ms.

4, When PLL_PDR[0] changes from “1” to “0”, the lock signal stays in “1” until a reset pulse comes. But the PLL is in unlocked state during this period.

5.10 ADC Characteristics

ADC Electrical characteristics
Table 21 shows the ADC electrical characteristics of W7500x

Table 21 ADC electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
IN[15:0]	Analog input channel		V_{SS}	-	VREFP	V
VREFP	Reference voltage of REFP			V_{DD}		V
RES	Resolution			12		Bits
Offset error			-3.0	±1.5	3.0	LSB
INL	Integral non-linearity error		-2.0	±1.0	2.0	LSB
DNL	Differential non-linearity error		-1.0	±0.8	1.5	LSB
Fclk	Clock frequency				16	MHz
SPS	Sampling rate		30	500	1000	K
TS	Sampling time		$4/F_{clk}$			
TC	Conversion time			12		$1/F_{clk}$
SNDR	Signal-noise plus distortion ratio	At 10KHz		64		dB
THD	Total harmonic distortion	At 10Khz		-65		dB
SFDR	Spurious-free dynamic range	At 10KHz		64		dB

ADC Transform function description
Figure 10. ADC transform function shows the ADC transform function of W7500x.

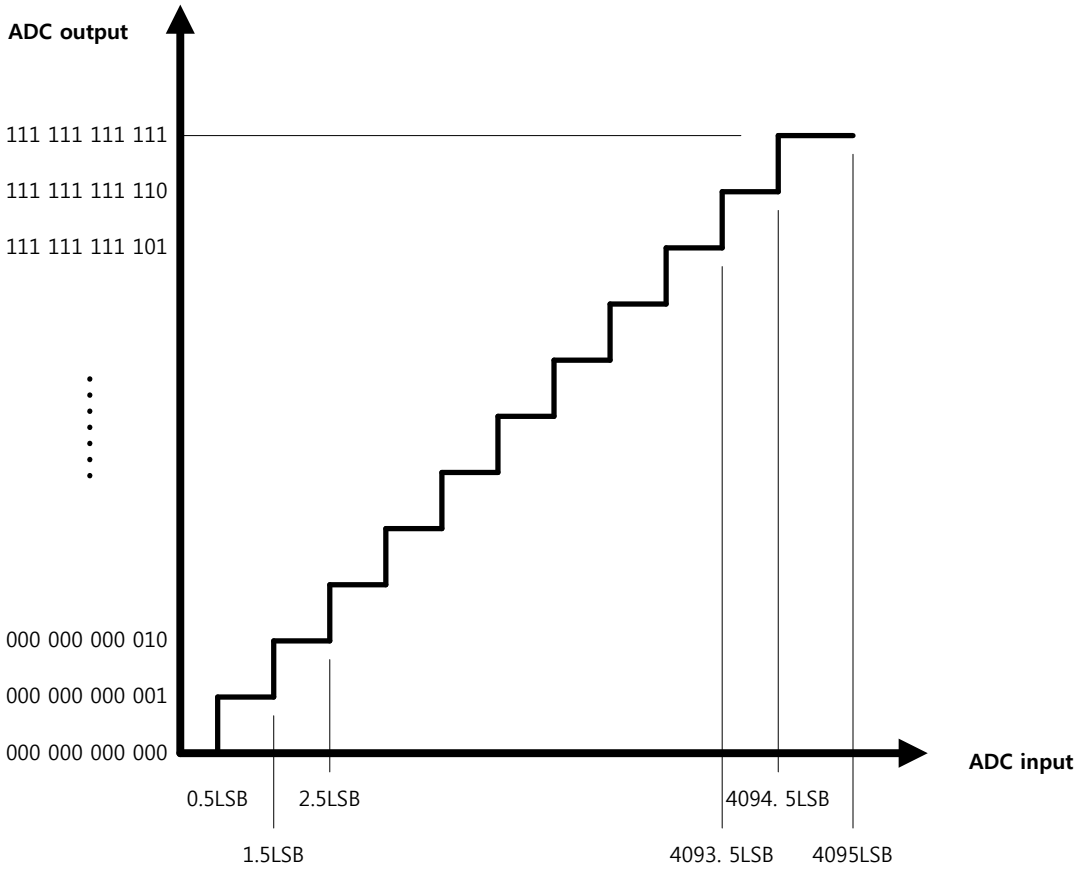


Figure 10. ADC transform function

5.11 SSP Interface Characteristics

The maximum SSP speed is 20 Mbit/s in master mode or 4 Mbit/s in slave mode. In slave mode, the maximum SSP clock rate must be 1/12 of the SSP PCLK clock rate.
Table 22 shows the SSP characteristics of W7500x.

Table 22 SSP characteristics

Symbol	Parameter	Min	Nom	Max	Unit
t_{clk_per}	SSPCLK cycle time	2		65024	System clocks
t_{clk_high}	SSPCLK high time	-	0.5		t clk_per
t_{clk_low}	SSPCLK low time	-	0.5		t clk_per
t_{clkrf}	SSPCLK rise/fall time	-	6	10	
t_{DMd}	Data from master valid delay time	0	-	1	System clocks
t_{DMs}	Data from master setup time	1	-	-	System clocks
t_{DMh}	Data from master hold time	2	-	-	System clocks
t_{DSs}	Data from slave setup time	1	-	-	System clocks
t_{DSh}	Data from slave hold time	2	-	-	System clocks

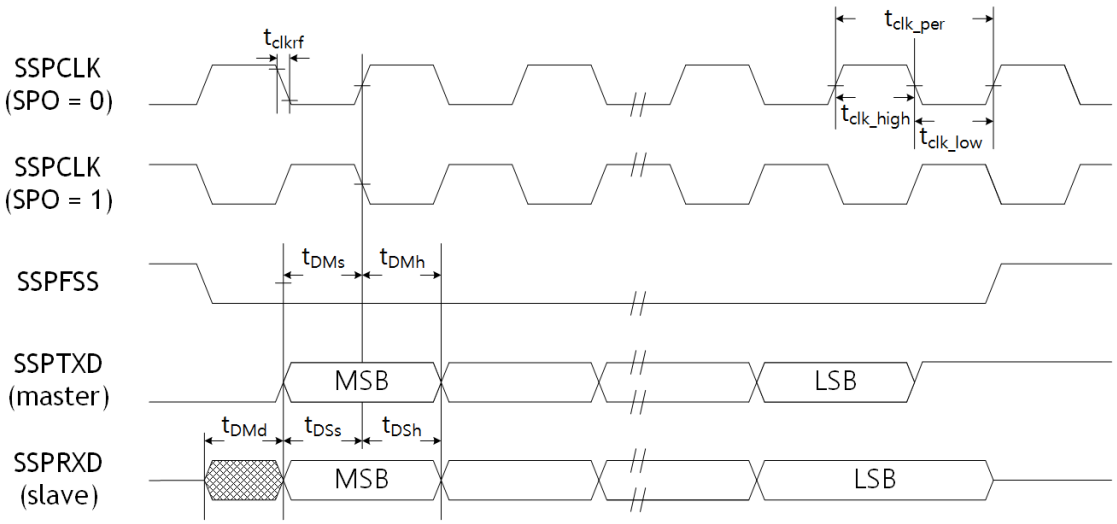


Figure 11. SSP Timing for SPI Frame format, with SPH =1

6 Package Information

6.1 Package dimension information

Figure 12 shows the package dimension information.

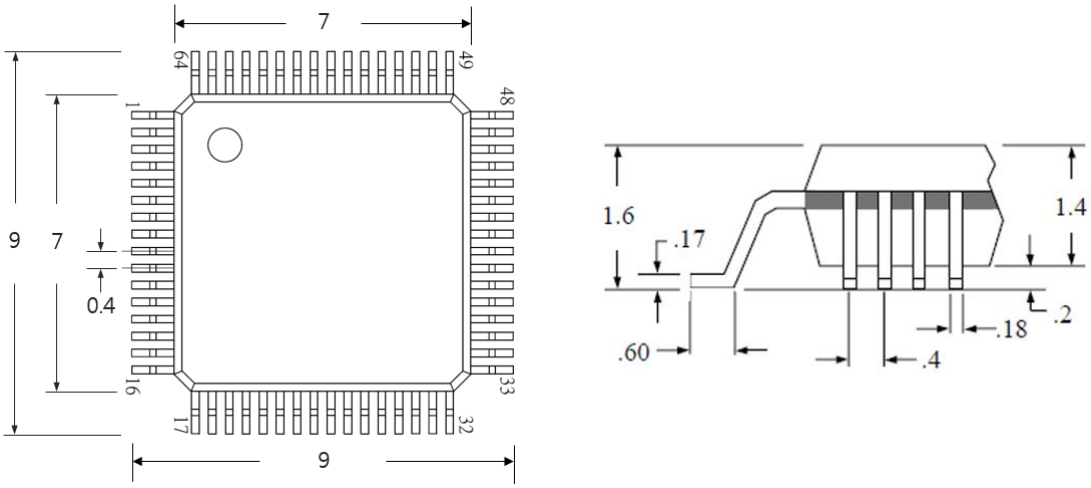


Figure 12. Package Dimension Information