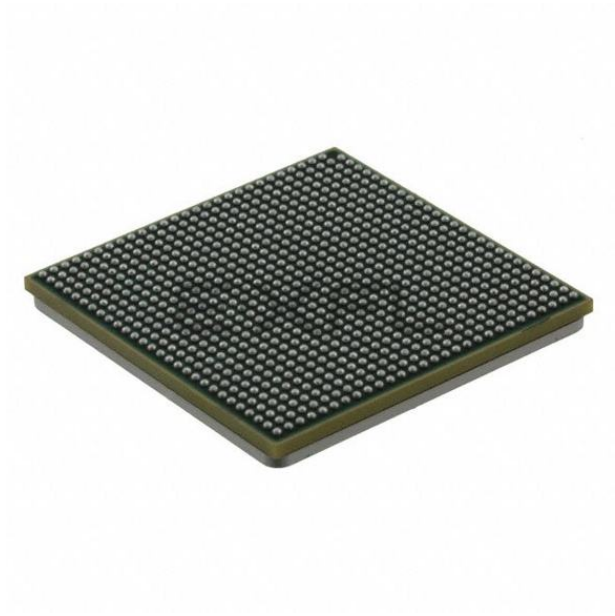


Welcome to E-XFL.COM

Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	SC3850 Six Core
Interface	Ethernet, I²C, PCI, RGMII, Serial RapidIO, SGMII, SPI, UART/USART
Clock Rate	1GHz
Non-Volatile Memory	ROM (96kB)
On-Chip RAM	576kB
Voltage - I/O	2.50V
Voltage - Core	1.00V
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=msc8156tvt1000b

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
B9	M2A13	O	GVDD2
B10	VSS	Ground	N/A
B11	GVDD2	Power	N/A
B12	$\overline{\text{M2CS1}}$	O	GVDD2
B13	VSS	Ground	N/A
B14	GVDD2	Power	N/A
B15	M2DQ35	I/O	GVDD2
B16	VSS	Ground	N/A
B17	GVDD2	Power	N/A
B18	M2DQ51	I/O	GVDD2
B19	VSS	Ground	N/A
B20	GVDD2	Power	N/A
B21	Reserved	NC	—
B22	Reserved	NC	—
B23	SR1_TXD0	O	SXPVDD1
B24	$\overline{\text{SR1\_TXD0}}$	O	SXPVDD1
B25	SXCVDD1	Power	N/A
B26	SXCVSS1	Ground	N/A
B27	$\overline{\text{SR1\_RXD0}}$	I	SXCVDD1
B28	SR1_RXD0	I	SXCVDD1
C1	M2DQ28	I/O	GVDD2
C2	M2DM3	O	GVDD2
C3	M2DQ26	I/O	GVDD2
C4	M2ECC4	I/O	GVDD2
C5	M2DM8	O	GVDD2
C6	M2ECC2	I/O	GVDD2
C7	M2CKE1	O	GVDD2
C8	M2CK0	O	GVDD2
C9	$\overline{\text{M2CK0}}$	O	GVDD2
C10	M2BA1	O	GVDD2
C11	M2A1	O	GVDD2
C12	$\overline{\text{M2WE}}$	O	GVDD2
C13	M2DQ37	I/O	GVDD2
C14	M2DM4	O	GVDD2
C15	M2DQ36	I/O	GVDD2
C16	M2DQ32	I/O	GVDD2
C17	M2DQ55	I/O	GVDD2
C18	M2DM6	O	GVDD2
C19	M2DQ53	I/O	GVDD2
C20	M2DQ52	I/O	GVDD2
C21	Reserved	NC	—
C22	SR1_IMP_CAL_RX	I	SXCVDD1
C23	SXPVSS1	Ground	N/A
C24	SXPVDD1	Power	N/A
C25	SR1_REF_CLK	I	SXCVDD1
C26	$\overline{\text{SR1\_REF\_CLK}}$	I	SXCVDD1

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
M5	M2DQ1	I/O	GVDD2
M6	VSS	Ground	N/.A
M7	GVDD2	Power	N/A
M8	M2DQ7	I/O	GVDD2
M9	M2DQ6	I/O	GVDD2
M10	VSS	Ground	N/A
M11	VDD	Power	N/A
M12	VSS	Ground	N/A
M13	VDD	Power	N/A
M14	VSS	Ground	N/A
M15	VDD	Power	N/A
M16	VSS	Ground	N/A
M17	VDD	Power	N/A
M18	VSS	Ground	N/A
M19	VDD	Power	N/A
M20	Reserved	NC	—
M21	Reserved	NC	—
M22	Reserved	NC	—
M23	SXPVSS2	Ground	N/A
M24	SXPVDD2	Power	N/A
M25	SR2_IMP_CAL_TX	I	SXCVDD2
M26	SXCVSS2	Ground	N/A
M27	Reserved	NC	—
M28	Reserved	NC	—
N1	VSS	Ground	N/A
N2	$\overline{\text{TRST}}$[7]	I	QVDD
N3	$\overline{\text{PORESET}}$[7]	I	QVDD
N4	VSS	Ground	N/A
N5	TMS[7]	I	QVDD
N6	CLKOUT	O	QVDD
N7	VSS	Ground	N/A
N8	VSS	Ground	N/A
N9	VSS	Ground	N/A
N10	VDD	Power	N/A
N11	VSS	Ground	N/A
N12	M3VDD	Power	N/A
N13	VSS	Ground	N/A
N14	VDD	Power	N/A
N15	VSS	Ground	N/A
N16	VDD	Power	N/A
N17	VSS	Ground	N/A
N18	VDD	Power	N/A
N19	VSS	Ground	N/A
N20	Reserved	NC	—
N21	SXPVDD2	Power	N/A
N22	SXPVSS2	Ground	N/A

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
N23	SR2_TXD2/PE_TXD2/SG1_TX[4]	O	SXPVDD2
N24	$\overline{\text{SR2\_TXD2}}$/$\overline{\text{PE\_TXD2}}$/$\overline{\text{SG1\_TX}}$[4]	O	SXPVDD2
N25	SXCVDD2	Power	N/A
N26	SXCVSS2	Ground	N/A
N27	$\overline{\text{SR2\_RXD2}}$/$\overline{\text{PE\_RXD2}}$/$\overline{\text{SG1\_RX}}$[4]	I	SXCVDD2
N28	SR2_RXD2/PE_RXD2/SG1_RX[4]	I	SXCVDD2
P1	CLKIN	I	QVDD
P2	EE0	I	QVDD
P3	QVDD	Power	N/A
P4	VSS	Ground	N/A
P5	STOP_BS	I	QVDD
P6	QVDD	Power	N/A
P7	VSS	Ground	N/A
P8	PLL0_AVDD[9]	Power	VDD
P9	PLL2_AVDD[9]	Power	VDD
P10	VSS	Ground	N/A
P11	VDD	Power	N/A
P12	VSS	Ground	N/A
P13	VDD	Power	N/A
P14	VSS	Ground	N/A
P15	MVDD	Power	N/A
P16	VSS	Ground	N/A
P17	MVDD	Power	N/A
P18	VSS	Ground	N/A
P19	VDD	Power	N/A
P20	Reserved	NC	—
P21	Reserved	NC	—
P22	Reserved	NC	—
P23	SXPVDD2	Power	N/A
P24	SXPVSS2	Ground	N/A
P25	SR2_PLL_AGND[9]	Ground	SXCVSS2
P26	SR2_PLL_AVDD[9]	Power	SXCVDD2
P27	SXCVSS2	Ground	N/A
P28	SXCVDD2	Power	N/A
R1	VSS	Ground	N/A
R2	$\overline{\text{NMI}}$	I	QVDD
R3	$\overline{\text{NMI\_OUT}}$[6]	O	QVDD
R4	$\overline{\text{HRESET}}$[6,7]	I/O	QVDD
R5	$\overline{\text{INT\_OUT}}$[6]	O	QVDD
R6	EE1	O	QVDD
R7	VSS	Ground	N/A
R8	PLL1_AVDD[9]	Power	VDD
R9	VSS	Ground	N/A
R10	VDD	Power	N/A
R11	VSS	Non-user	N/A
R12	VDD	Power	N/A

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
AC19	VSS	Ground	N/A
AC20	GVDD1	Power	N/A
AC21	VSS	Ground	N/A
AC22	NVDD	Power	N/A
AC23	GPIO30/I2C_SCL[5,8]	I/O	NVDD
AC24	GPIO26/TMR3[5,8]	I/O	NVDD
AC25	VSS	Ground	N/A
AC26	NVDD	Power	N/A
AC27	GPIO23/TMR0[5,8]	I/O	NVDD
AC28	GPIO22[5,8]	I/O	NVDD
AD1	M1DQ31	I/O	GVDD1
AD2	M1DQ30	I/O	GVDD1
AD3	M1DQ27	I/O	GVDD1
AD4	M1ECC7	I/O	GVDD1
AD5	M1ECC6	I/O	GVDD1
AD6	M1ECC3	I/O	GVDD1
AD7	M1A9	O	GVDD1
AD8	M1A6	O	GVDD1
AD9	M1A3	O	GVDD1
AD10	M1A10	O	GVDD1
AD11	$\overline{\text{M1RAS}}$	O	GVDD1
AD12	M1A2	O	GVDD1
AD13	M1DQ38	I/O	GVDD1
AD14	$\overline{\text{M1DQS}}$5	I/O	GVDD1
AD15	M1DQS5	I/O	GVDD1
AD16	M1DQ33	I/O	GVDD1
AD17	M1DQ56	I/O	GVDD1
AD18	M1DQ57	I/O	GVDD1
AD19	$\overline{\text{M1DQS7}}$	I/O	GVDD1
AD20	M1DQS7	I/O	GVDD1
AD21	VSS	Ground	N/A
AD22	GE2_TX_CTL	O	NVDD
AD23	GPIO15/DDN0/$\overline{\text{IRQ15}}$/RC15[5,8]	I/O	NVDD
AD24	GPIO13/$\overline{\text{IRQ13}}$/RC13[5,8]	I/O	NVDD
AD25	GE_MDC	O	NVDD
AD26	GE_MDIO	I/O	NVDD
AD27	TDM2TCK/GE1_TD3[3]	I/O	NVDD
AD28	TDM2RCK/GE1_TD0[3]	I/O	NVDD
AE1	GVDD1	Power	N/A
AE2	VSS	Ground	N/A
AE3	M1DQ29	I/O	GVDD1
AE4	GVDD1	Power	N/A
AE5	VSS	Ground	N/A
AE6	M1ECC5	I/O	GVDD1
AE7	GVDD1	Power	N/A
AE8	VSS	Ground	N/A

2.2 Recommended Operating Conditions

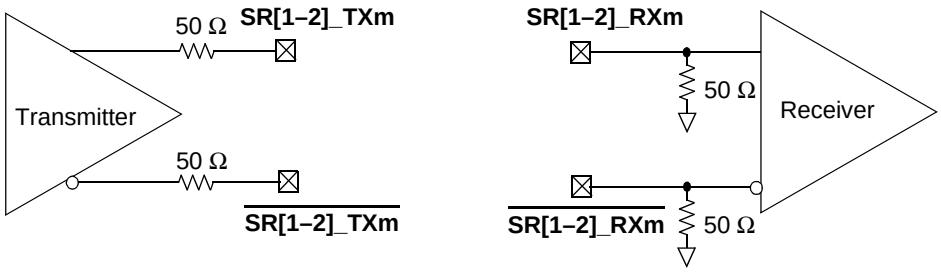
Table 3 lists recommended operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 3. Recommended Operating Conditions

Rating	Symbol	Min	Nominal	Max	Unit
Core supply voltage	V_{DD}	0.97	1.0	1.05	V
M3 memory supply voltage	V_{DDM3}	0.97	1.0	1.05	V
MAPLE-B supply voltage	V_{DDM}	0.97	1.0	1.05	V
DDR memory supply voltage • DDR2 mode • DDR3 mode DDR reference voltage	V_{DDDDR} MV_{REF}	 1.7 1.425 $0.49 \times V_{DDDDR}$	 1.8 1.5 $0.5 \times V_{DDDDR}$	 1.9 1.575 $0.51 \times V_{DDDDR}$	 V V V
I/O voltage excluding DDR and RapidIO lines	V_{DDIO}	2.375	2.5	2.625	V
Rapid I/O pad voltage	V_{DDSXP}	0.97	1.0	1.05	V
Rapid I/O core voltage	V_{DDSXC}	0.97	1.0	1.05	V
Operating temperature range: • Standard • Higher • Extended	 T_J T_J T_A T_J	 0 0 –40 —		 90 105 — 105	 °C °C °C

2.5.2.3 SerDes Transmitter and Receiver Reference Circuits

Figure 6 shows the reference circuits for SerDes data lane transmitter and receiver.



Note: The [1–2] indicates the specific SerDes Interface (1 or 2) and the m indicates the specific channel within that interface (0,1,2,3). Actual signals are assigned by the HRCW assignments at reset (see **Chapter 5**, *Reset* in the reference manual for details)

Figure 6. SerDes Transmitter and Receiver Reference Circuits

2.5.3 DC-Level Requirements for SerDes Interfaces

The following subsections define the DC-level requirements for the SerDes reference clocks, the PCI Express data lines, the Serial RapidIO data lines, and the SGMII data lines.

2.5.3.1 DC-Level Requirements for SerDes Reference Clocks

The DC-level requirement for the SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs, as described below:

- Differential Mode
  - The input amplitude of the differential clock must be between 400 mV and 1600 mV differential peak-peak (or between 200 mV and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing of less than 800 mV and greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.
  - For an external DC-coupled connection, the maximum average current requirements sets the requirement for average voltage (common mode voltage) as between 100 mV and 400 mV. Figure 7 shows the SerDes reference clock input requirement for DC-coupled connection scheme.

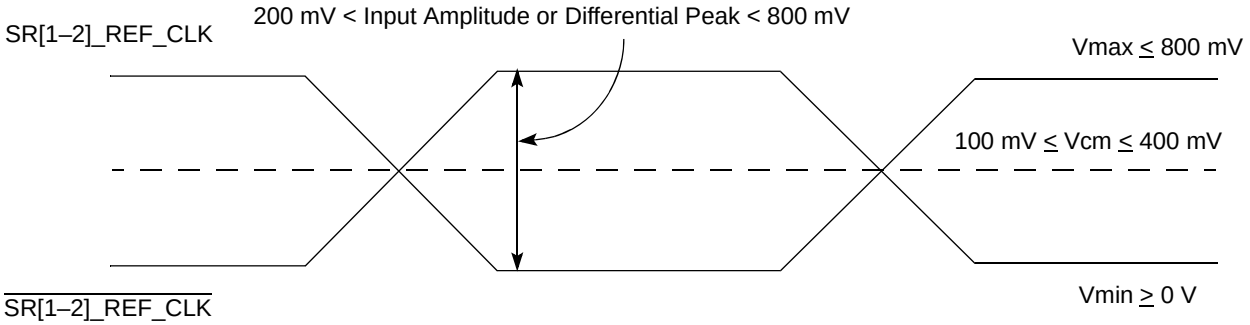


Figure 7. Differential Reference Clock Input DC Requirements (External DC-Coupled)

— For an external AC-coupled connection, there is no common mode voltage requirement for the clock driver. Because the external AC-coupling capacitor blocks the DC-level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to GND_{SXC}. Each signal wire of the differential inputs is allowed to swing below and above the command mode voltage GND_{SXC}. Figure 8 shows the SerDes reference clock input requirement for AC-coupled connection scheme.

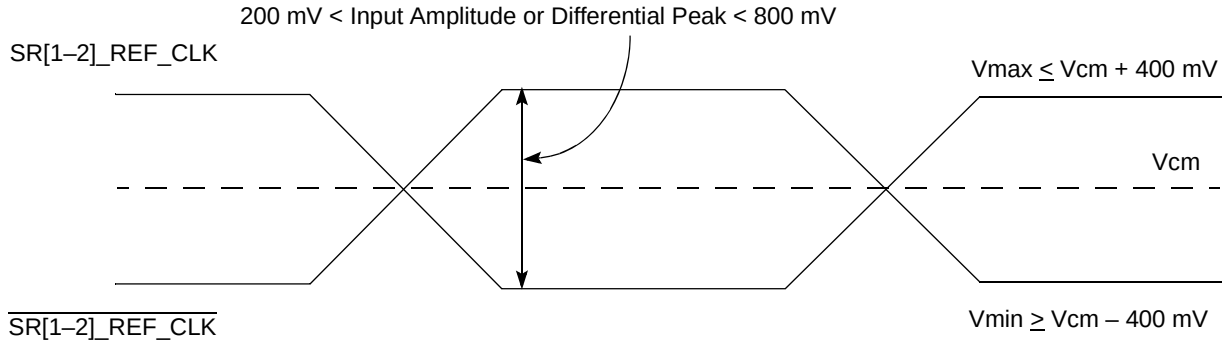


Figure 8. Differential Reference Clock Input DC Requirements (External AC-Coupled)

- Single-Ended Mode
  — The reference clock can also be single-ended. The SR[1–2]_REF_CLK input amplitude (single-ended swing) must be between 400 mV and 800 mV peak-peak (from V_{MIN} to V_{MAX}) with $\overline{\text{SR[1–2]\_REF\_CLK}}$ either left unconnected or tied to ground.
  — The SR[1–2]_REF_CLK input average voltage must be between 200 and 400 mV. Figure 9 shows the SerDes reference clock input requirement for single-ended signalling mode.
  — To meet the input amplitude requirement, the reference clock inputs may need to be DC- or AC-coupled externally. For the best noise performance, the reference of the clock could be DC- or AC-coupled into the unused phase ($\overline{\text{SR[1–2]\_REF\_CLK}}$) through the same source impedance as the clock input (SR[1–2]_REF_CLK) in use.

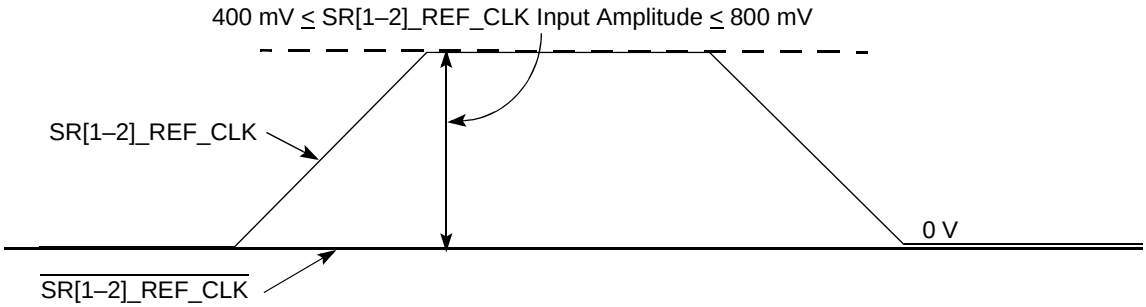


Figure 9. Single-Ended Reference Clock Input DC Requirements

2.5.3.2 DC-Level Requirements for PCI Express Configurations

The DC-level requirements for PCI Express implementations have separate requirements for the Tx and Rx lines. The MSC8156 supports a 2.5 Gbps PCI Express interface defined by the *PCI Express Base Specification, Revision 1.0a*. The transmitter specifications are defined in Table 11 and the receiver specifications are defined in Table 12.

Note: Specifications are valid at the recommended operating conditions listed in Table 3.

Table 11. PCI Express (2.5 Gbps) Differential Transmitter (Tx) Output DC Specifications

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential peak-to-peak output voltage	$V_{TX\text{-}DIFFp\text{-}p}$	800	1000	1200	mV	1
De-emphasized differential output voltage (ratio)	$V_{TX\text{-}DE\text{-}RATIO}$	3.0	3.5	4.0	dB	2
DC differential Tx impedance	$Z_{TX\text{-}DIFF\text{-}DC}$	80	100	120	Ω	3
Transmitter DC impedance	$Z_{TX\text{-}DC}$	40	50	60	Ω	4

Notes:
1. $V_{TX\text{-}DIFFp\text{-}p} = 2 \times |V_{TX\text{-}D+} - V_{TX\text{-}D\text{-}}|$ Measured at the package pins with a test load of 50 Ω to GND on each pin.
2. Ratio of the $V_{TX\text{-}DIFFp\text{-}p}$ of the second and following bits after a transition divided by the $V_{TX\text{-}DIFFp\text{-}p}$ of the first bit after a transition. Measured at the package pins with a test load of 50 Ω to GND on each pin.
3. Tx DC differential mode low impedance
4. Required Tx D+ as well as D– DC Impedance during all states

Table 12. PCI Express (2.5 Gbps) Differential Receiver (Rx) Input DC Specifications

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential input peak-to-peak voltage	$V_{RX\text{-}DIFFp\text{-}p}$	120	1000	1200	mV	1
DC differential Input Impedance	$Z_{RX\text{-}DIFF\text{-}DC}$	80	100	120	Ω	2
DC input impedance	$Z_{RX\text{-}DC}$	40	50	60	Ω	3
Powered down DC input impedance	$Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC}$	50	—	—	KΩ	4
Electrical idle detect threshold	$V_{RX\text{-}IDLE\text{-}DET\text{-}DIFFp\text{-}p}$	65	—	175	mV	5

Notes:
1. $V_{RX\text{-}DIFFp\text{-}p} = 2 \times |V_{RX\text{-}D+} - V_{RX\text{-}D\text{-}}|$ Measured at the package pins with a test load of 50 Ω to GND on each pin.
2. Rx DC differential mode impedance. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM), there is a 5 ms transition time before the receiver termination values must be met on all unconfigured lanes of a port.
3. Required Rx D+ as well as D– DC Impedance (50 ±20% tolerance). Measured at the package pins with a test load of 50 Ω to GND on each pin. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM), there is a 5 ms transition time before the receiver termination values must be met on all unconfigured lanes of a port.
4. Required Rx D+ as well as D– DC Impedance when the receiver terminations do not have power. The Rx DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the Rx ground.
5. $V_{RX\text{-}IDLE\text{-}DET\text{-}DIFFp\text{-}p} = 2 \times |V_{RX\text{-}D+} - V_{RX\text{-}D\text{-}}|$. Measured at the package pins of the receiver

2.5.3.3 DC-Level Requirements for Serial RapidIO Configurations

This sections provided various DC-level requirements for Serial RapidIO Configurations.

Note: Specifications are valid at the recommended operating conditions listed in Table 3.

Table 13. Serial RapidIO Transmitter DC Specifications

Parameter	Symbol	Min	Typical	Max	Units	Notes
Output voltage	V_O	–0.40	—	2.30	V	1
Long run differential output voltage	V_{DIFFPP}	800	—	1600	mVp-p	—
Short run differential output voltage	V_{DIFFPP}	500	—	1000	mVp-p	—

Note: Voltage relative to COMMON of either signal comprising a differential pair.

Table 14. Serial RapidIO Receiver DC Specifications

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential input voltage	V_{IN}	200	—	1600	mVp-p	1

Notes: **1.** Measured at receiver.

2.5.3.4 DC-Level Requirements for SGMII Configurations

Note: Specifications are valid at the recommended operating conditions listed in Table 3

Table 15 describes the SGMII SerDes transmitter AC-coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs (SR[1–2]_TX[n] and $\overline{\text{SR[1–2]\_TX[n]}}$) as shown in Figure 10.

Table 15. SGMII DC Transmitter Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output high voltage	V_{OH}	—	—	$XV_{DD\_SRDS\text{-}Typ}/2 + \lvert V_{OD}\rvert_{\text{-}max}/2$	mV	1
Output low voltage	V_{OL}	$XV_{DD\_SRDS\text{-}Typ}/2 - \lvert V_{OD}\rvert_{\text{-}max}/2$	—	—	mV	1
Output differential voltage ($XV_{DD\text{-}Typ}$ at 1.0 V)	$\lvert V_{OD}\rvert$	323	500	725	mV	2,3,4
		296	459	665		2,3,5
		269	417	604		2,3,6
		243	376	545		2,3,7
		215	333	483		2,3,8
		189	292	424		2,3,9
		162	250	362		2,3,10
Output impedance (single-ended)	R_O	40	50	60	Ω	—

Notes:
1. This does not align to DC-coupled SGMII. $XV_{DD\_SRDS2\text{-}Typ} = 1.1$ V.
2. The $\lvert V_{OD}\rvert$ value shown in the table assumes full multitude by setting srd_smit_lvl as 000 and the following transmit equalization setting in the XMITEQ**AB** (for lanes A and B) or XMITEQ**EF** (for lanes E and F) bit field of Control Register:
• The MSB (bit 0) of the above bit field is set to zero (selecting the full $V_{DD\text{-}DIFF\text{-}p\text{-}p}$ amplitude which is power up default);
• The LSB (bit [1–3]) of the above bit field is set based on the equalization settings listed in notes 4 through 10.
3. The $\lvert V_{OD}\rvert$ value shown in the Typ column is based on the condition of $XV_{DD\_SRDS2\text{-}Typ} = 1.0$ V, no common mode offset variation (V_{OS} =500mV), SerDes transmitter is terminated with 100-Ω differential load between
4. Equalization setting: 1.0x: 0000.
5. Equalization setting: 1.09x: 1000.
6. Equalization setting: 1.2x: 0100.
7. Equalization setting: 1.33x: 1100.
8. Equalization setting: 1.5x: 0010.
9. Equalization setting: 1.71x: 1010.
10. Equalization setting: 2.0x: 0110.
11. $\lvert V_{OD}\rvert = \lvert V_{SR[1–2]\_TXn} - V_{\overline{SR[1–2]\_TXn}}\rvert$. $\lvert V_{OD}\rvert$ is also referred to as output differential peak voltage. $V_{TX\text{-}DIFFp\text{-}p} = 2*\lvert V_{OD}\rvert$.

Table 21. DDR SDRAM Output AC Timing Specifications (continued)

Parameter	Symbol [1]	Min	Max	Unit	Notes

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK(n) clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This will typically be set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these two parameters have been set to the same adjustment value. See the *MSC8156 Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the MSC8156.
6. At recommended operating conditions with V_{DDDDR} (1.5 V or 1,8 V) ± 5%.

Note: For the ADDR/CMD setup and hold specifications in Table 21, it is assumed that the clock control register is set to adjust the memory clocks by ½ applied cycle.

Figure 12 shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

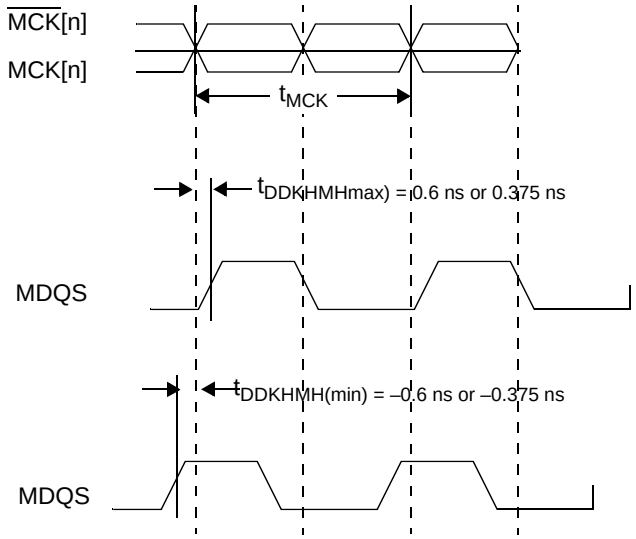


Figure 12. MCK to MDQS Timing

Figure 13 shows the DDR SDRAM output timing diagram.

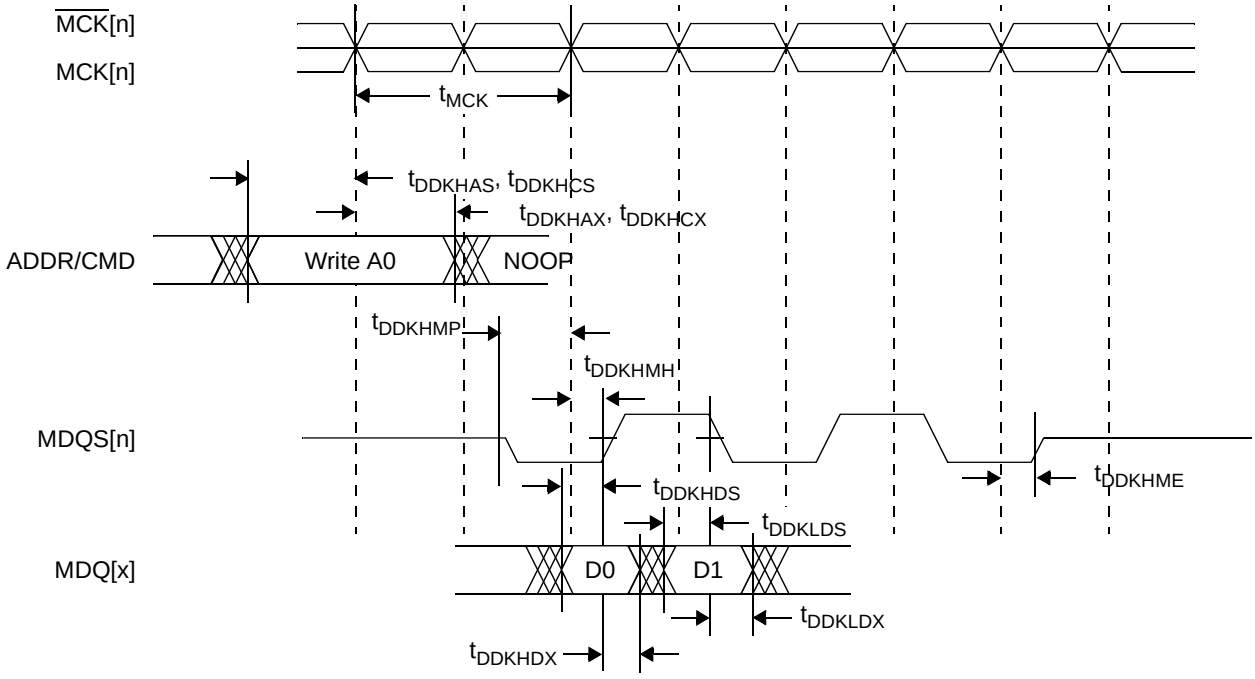


Figure 13. DDR SDRAM Output Timing

Figure 14 provides the AC test load for the DDR2 and DDR3 controller bus.

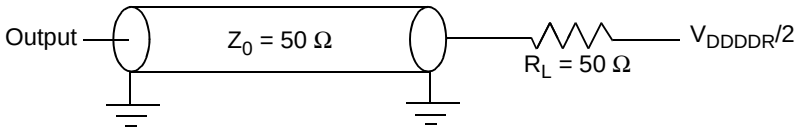


Figure 14. DDR2 and DDR3 Controller Bus AC Test Load

2.6.1.3 DDR2 and DDR3 SDRAM Differential Timing Specifications

This section describes the DC and AC differential timing specifications for the DDR2 and DDR3 SDRAM controller interface. Figure 15 shows the differential timing specification.

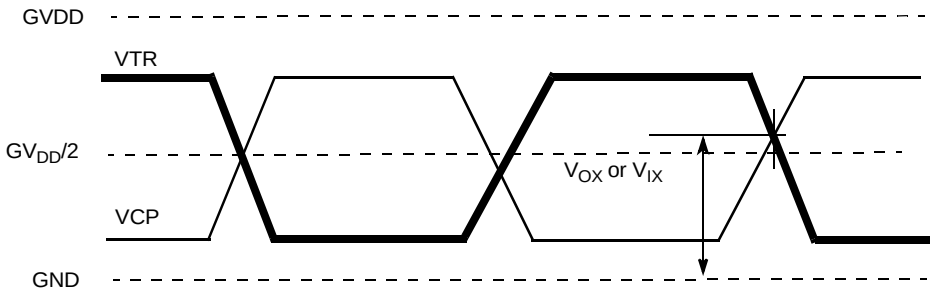


Figure 15. DDR2 and DDR3 SDRAM Differential Timing Specifications

Note: VTR specifies the true input signal (such as MCK or MDQS) and VCP is the complementary input signal (such as $\overline{\text{MCK}}$ or $\overline{\text{MDQS}}$).

Table 22 provides the DDR2 differential specifications for the differential signals MDQS/$\overline{\text{MDQS}}$ and MCK/$\overline{\text{MCK}}$.

Table 22. DDR2 SDRAM Differential Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
Input AC differential cross-point voltage	V_{IXAC}	0.5 × GVDD – 0.175	0.5 × GVDD + 0.175	V
Output AC differential cross-point voltage	V_{OXAC}	0.5 × GVDD – 0.125	0.5 × GVDD + 0.125	V

Table 23 provides the DDR3 differential specifications for the differential signals MDQS/$\overline{\text{MDQS}}$ and MCK/$\overline{\text{MCK}}$.

Table 23. DDR3 SDRAM Differential Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
Input AC differential cross-point voltage	V_{IXAC}	0.5 × GVDD – 0.150	0.5 × GVDD + 0.150	V
Output AC differential cross-point voltage	V_{OXAC}	0.5 × GVDD – 0.115	0.5 × GVDD + 0.115	V

2.6.2 HSSI AC Timing Specifications

The following subsections define the AC timing requirements for the SerDes reference clocks, the PCI Express data lines, the Serial RapidIO data lines, and the SGMII data lines.

2.6.2.1 AC Requirements for SerDes Reference Clock

Table 24 lists AC requirements for the SerDes reference clocks.

Note: Specifications are valid at the recommended operating conditions listed in Table 3.

Table 24. SR[1–2]_REF_CLK and $\overline{\text{SR[1–2]\_REF\_CLK}}$ Input Clock Requirements

Parameter	Symbol	Min	Typical	Max	Units	Notes
SR[1–2]_REF_CLK/$\overline{\text{SR[1–2]\_REF\_CLK}}$ frequency range	t_{CLK_REF}	—	100/125	—	MHz	1
SR[1–2]_REF_CLK/$\overline{\text{SR[1–2]\_REF\_CLK}}$ clock frequency tolerance	t_{CLK_TOL}	–350	—	350	ppm	—
SR[1–2]_REF_CLK/$\overline{\text{SR[1–2]\_REF\_CLK}}$ reference clock duty cycle (measured at 1.6 V)	t_{CLK_DUTY}	40	50	60	%	—
SR[1–2]_REF_CLK/$\overline{\text{SR[1–2]\_REF\_CLK}}$ max deterministic peak-peak jitter at 10^{-6} BER	t_{CLK_DJ}	—	—	42	ps	—
SR[1–2]_REF_CLK/$\overline{\text{SR[1–2]\_REF\_CLK}}$ total reference clock jitter at 10^{-6} BER (peak-to-peak jitter at ref_clk input)	t_{CLK_TJ}	—	—	86	ps	2
SR[1–2]_REF_CLK/$\overline{\text{SR[1–2]\_REF\_CLK}}$ rising/falling edge rate	t_{CLKRR}/t_{CLKFR}	1	—	4	V/ns	3
Differential input high voltage	V_{IH}	200	—	—	mV	4
Differential input low voltage	V_{IL}	—	—	–200	mV	4
Rising edge rate (SR[1–2]_REF_CLK) to falling edge rate (SR[1–2]_REF_CLK) matching	Rise-Fall Matching	—	—	20	%	5, 6

2.6.3 TDM Timing

Table 31 provides the input and output AC timing specifications for the TDM interface.

Table 31. TDM AC Timing Specifications for 62.5 MHz[1]

Parameter	Symbol[2]	Min	Max	Unit
TDMxRCK/TDMxTCK	t_{DM}	16.0	—	ns
TDMxRCK/TDMxTCK high pulse width	t_{DM_HIGH}	7.0	—	ns
TDMxRCK/TDMxTCK low pulse width	t_{DM_LOW}	7.0	—	ns
TDM all input setup time	t_{DMIVKH}	3.6	—	ns
TDMxRD hold time	$t_{DMRDIXKH}$	1.9	—	ns
TDMxTFS/TDMxRFS input hold time	$t_{DMFSIXKH}$	1.9	—	ns
TDMxTCK High to TDMxTD output active	t_{DM_OUTAC}	2.5	—	ns
TDMxTCK High to TDMxTD output valid	$t_{DMTKHOV}$	—	9.8	ns
TDMxTD hold time	$t_{DMTKHOX}$	2.5	—	ns
TDMxTCK High to TDMxTD output high impedance	t_{DM_OUTHI}	—	9.8	ns
TDMxTFS/TDMxRFS output valid	$t_{DMFSKHOV}$	—	9.25	ns
TDMxTFS/TDMxRFS output hold time	$t_{DMFSKHOX}$	2.0	—	ns

Notes:
1. The symbols used for timing specifications follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{HIKHOX} symbolizes the output internal timing (HI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).
2. Output values are based on 30 pF capacitive load.
3. Inputs are referenced to the sampling that the TDM is programmed to use. Outputs are referenced to the programming edge they are programmed to use. Use of the rising edge or falling edge as a reference is programmable. T_{DMxTCK} and T_{DMxRCK} are shown using the rising edge.
4. All values are based on a maximum TDM interface frequency of 62.5 MHz.

Figure 20 shows the TDM receive signal timing.

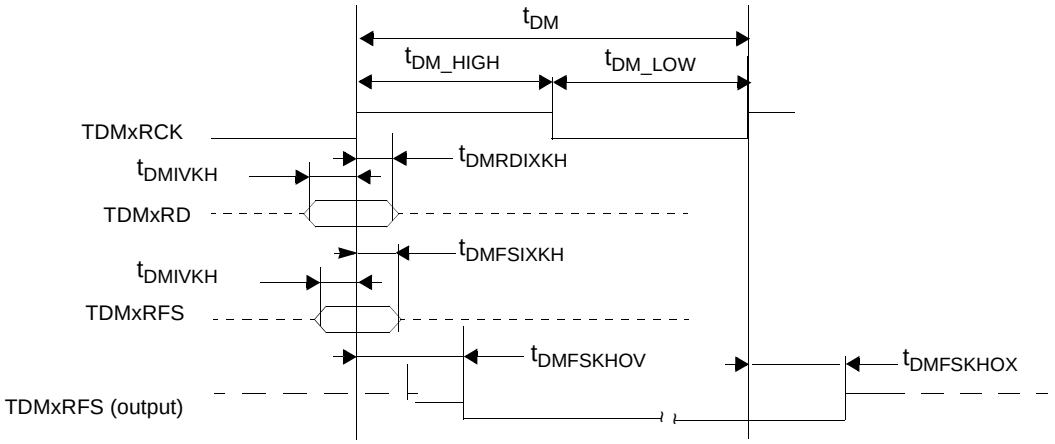


Figure 20. TDM Receive Signals

Figure 21 shows the TDM transmit signal timing.

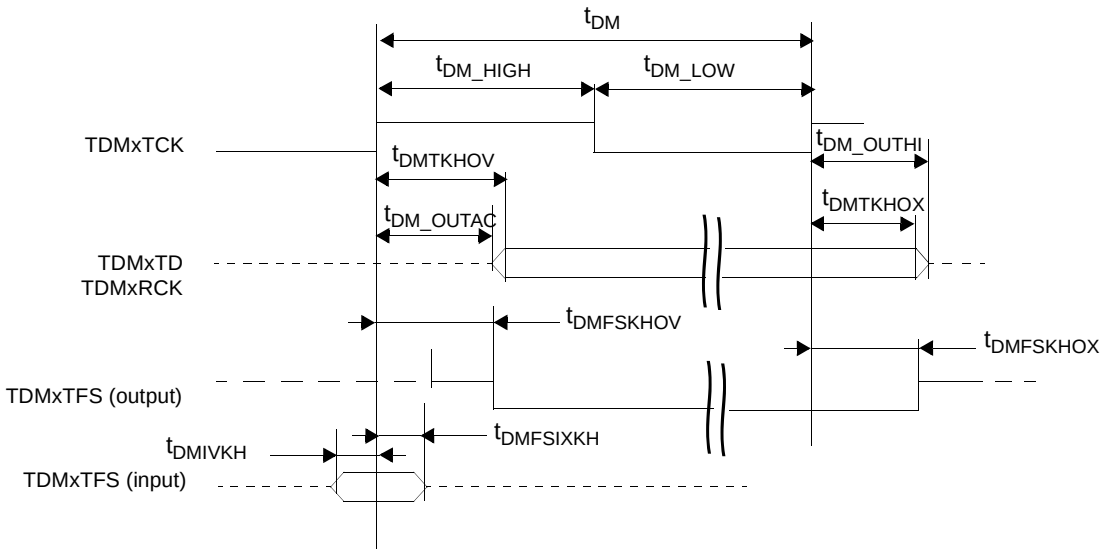


Figure 21. TDM Transmit Signals

Figure 22 provides the AC test load for the TDM/SI.

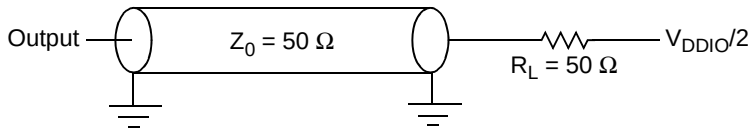


Figure 22. TDM AC Test Load

2.6.4 Timers AC Timing Specifications

Table 32 lists the timer input AC timing specifications.

Table 32. Timers Input AC Timing Specifications

Characteristics	Symbol	Minimum	Unit	Notes
Timers inputs—minimum pulse width	T_{TIWID}	8	ns	1, 2

Notes:
1. The maximum allowed frequency of timer outputs is 125 MHz. Configure the timer modules appropriately.
2. Timer inputs and outputs are asynchronous to any visible clock. Timer outputs should be synchronized before use by any external synchronous logic. Timer inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation.

Note: For recommended operating conditions, see Table 3.

Figure 23 shows the AC test load for the timers.

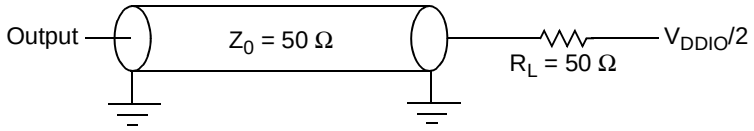


Figure 23. Timer AC Test Load

2.6.5 Ethernet Timing

This section describes the AC electrical characteristics for the Ethernet interface.

There are programmable delay units (PDU) that should be programmed differently for each interface to meet timing. There is a general configuration register 4 (GCR4) used to configure the timing. For additional information, see the *MSC8156 Reference Manual*.

2.6.5.1 Management Interface Timing

Table 33 lists the timer input Ethernet controller management interface timing specifications shown in Figure 24.

Table 33. Ethernet Controller Management Interface Timing

Characteristics	Symbol	Min	Max	Unit
GE_MDC frequency	f_{MDC}	—	2.5	MHz
GE_MDC period	t_{MDC}	400	—	ns
GE_MDC clock pulse width high	t_{MDC_H}	160	—	ns
GE_MDC clock pulse width low	t_{MDC_L}	160	—	ns
GE_MDC to GE_MDIO delay[2]	t_{MDKHDX}	10	70	ns
GE_MDIO to GE_MDC rising edge setup time	t_{MDDVKH}	20	—	ns
GE_MDC rising edge to GE_MDIO hold time	t_{MDDXKH}	0	—	ns

Notes:
1. Program the GE_MDC frequency (f_{MDC}) to a maximum value of 2.5 MHz (400 ns period for t_{MDC}). The value depends on the source clock and configuration of MIIMCFG[MCS] and UPSMR[MDCP]. For example, for a source clock of 400 MHz to achieve f_{MDC} = 2.5 MHz, program MIIMCFG[MCS] = 0x4 and UPSMR[MDCP] = 0. See the *MSC8156 Reference Manual* for configuration details.
2. The value depends on the source clock. For example, for a source clock of 267 MHz, the delay is 70 ns. For a source clock of 333 MHz, the delay is 58 ns.

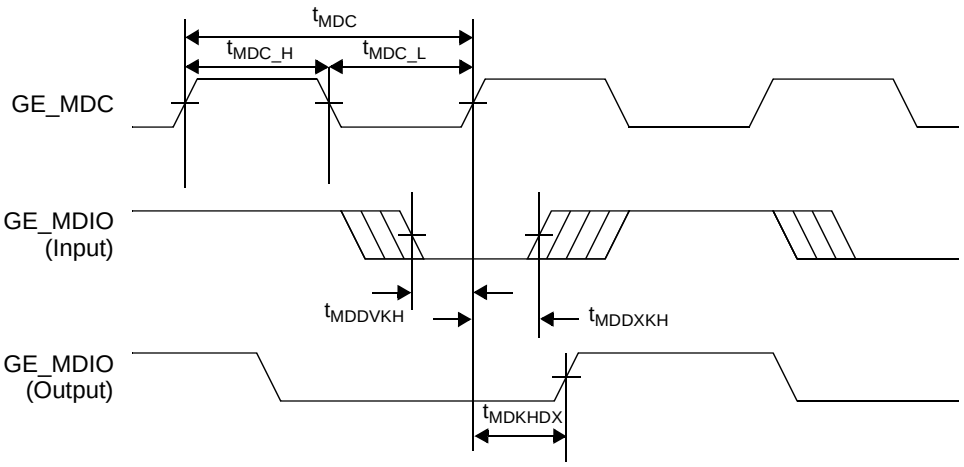


Figure 24. MII Management Interface Timing

2.6.5.2 RGMII AC Timing Specifications

Table 34 presents the RGMII AC timing specifications for applications requiring an on-board delayed clock.

Table 34. RGMII at 1 Gbps[2] with On-Board Delay[3] AC Timing Specifications

Parameter/Condition	Symbol	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)[4]	t_{SKEWT}	–-0.5	—	0.5	ns
Data to clock input skew (at receiver) [4]	t_{SKEWR}	1	—	2.6	ns

Notes:
1. At recommended operating conditions with V_{DDIO} of 2.5 V ± 5%.
2. RGMII at 100 Mbps support is guaranteed by design.
3. Program GCR4 as 0x00000000.
4. This implies that PC board design requires clocks to be routed such that an additional trace delay of greater than 1.5 ns and less than 2.0 ns is added to the associated clock signal.

Table 35 presents the RGMII AC timing specification for applications required non-delayed clock on board.

Table 35. RGMII at 1 Gbps[2] with No On-Board Delay[3] AC Timing Specifications

Parameter/Condition	Symbol	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)[4]	t_{SKEWT}	–2.6	—	–1.0	ns
Data to clock input skew (at receiver)[4]	t_{SKEWR}	–0.5	—	0.5	ns

Notes:
1. At recommended operating conditions with V_{DDIO} of 2.5 V ± 5%.
2. RGMII at 100 Mbps support is guaranteed by design.
3. GCR4 should be programmed as 0x000CC330.
4. This implies that PC board design requires clocks to be routed with no additional trace delay

Figure 25 shows the RGMII AC timing and multiplexing diagrams.

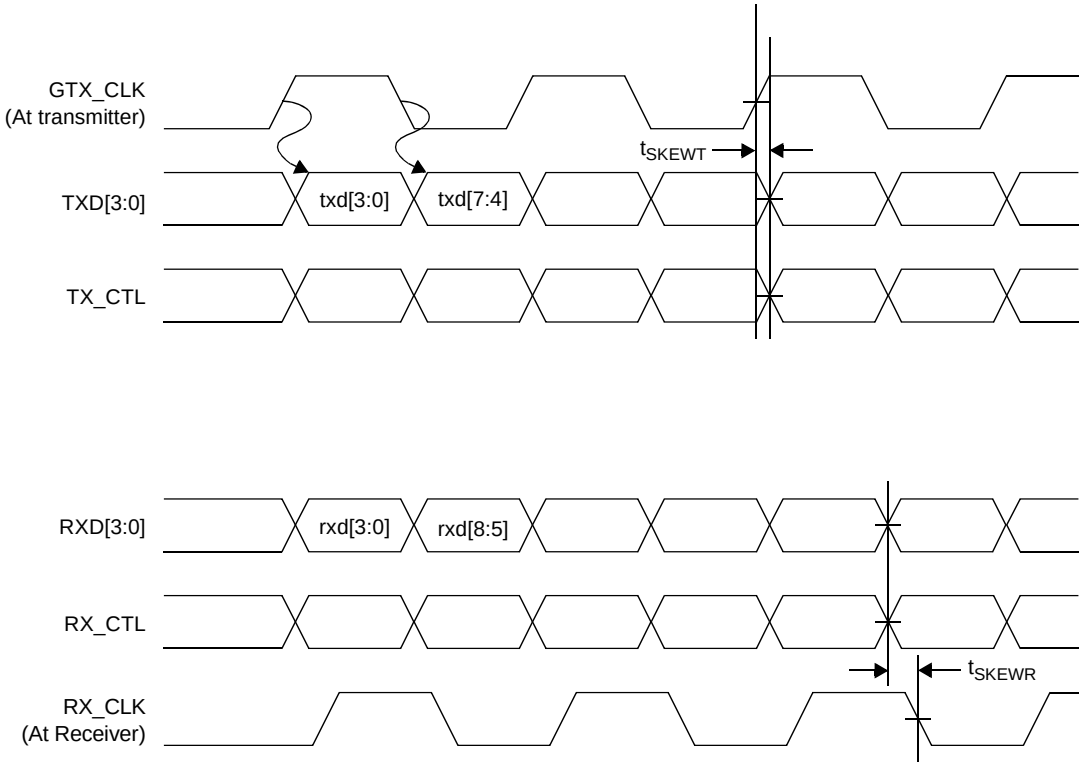


Figure 25. RGMII AC Timing and Multiplexing

2.6.6 SPI Timing

Table 36 lists the SPI input and output AC timing specifications.

Table 36. SPI AC Timing Specifications

Parameter	Symbol [1]	Min	Max	Unit	Note
SPI outputs valid—Master mode (internal clock) delay	t_{NIKHOV}	—	6	ns	2
SPI outputs hold—Master mode (internal clock) delay	t_{NIKHOX}	0.5	—	ns	2
SPI outputs valid—Slave mode (external clock) delay	t_{NEKHOV}	—	12	ns	2
SPI outputs hold—Slave mode (external clock) delay	t_{NEKHOX}	2	—	ns	2
SPI inputs—Master mode (internal clock) input setup time	t_{NIIVKH}	12	—	ns	—
SPI inputs—Master mode (internal clock) input hold time	t_{NIIXKH}	0	—	ns	—
SPI inputs—Slave mode (external clock) input setup time	t_{NEIVKH}	4	—	ns	—
SPI inputs—Slave mode (external clock) input hold time	t_{NEIXKH}	2	—	ns	—

Notes:
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOX} symbolizes the internal timing (NI) for the time SPICLK clock reference (K) goes to the high state (H) until outputs (O) are invalid (X).
2. Output specifications are measured from the 50% level of the rising edge of SPICLK to the 50% level of the signal. Timings are measured at the pin.

Figure 26 provides the AC test load for the SPI.

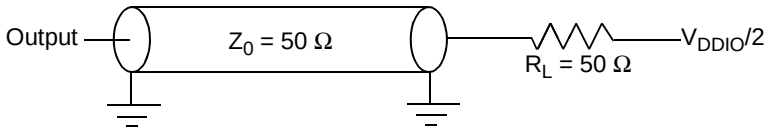
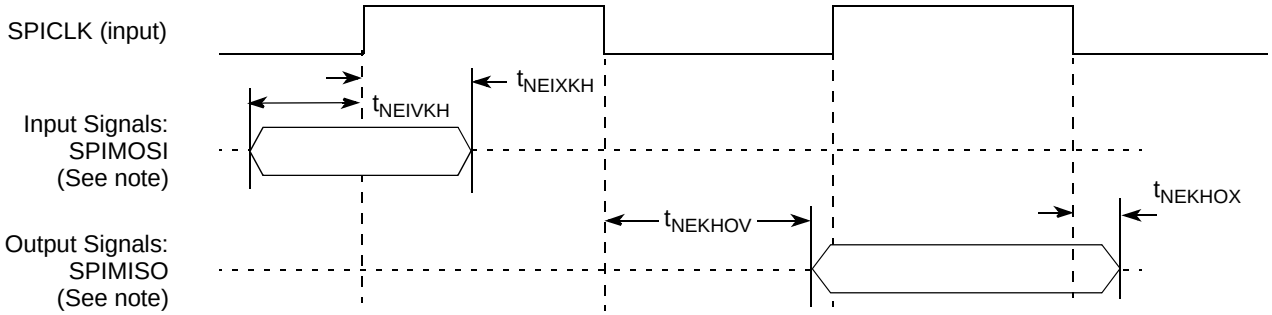


Figure 26. SPI AC Test Load

Figure 27 and Figure 28 represent the AC timings from Table 36. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

Figure 27 shows the SPI timings in slave mode (external clock).



Note: measured with SPMODE[CI] = 0, SPMODE[CP] = 0

Figure 27. SPI AC Timing in Slave Mode (External Clock)

Figure 28 shows the SPI timings in master mode (internal clock).

3.2 PLL Power Supply Design Considerations

Each global PLL power supply must have an external RC filter for the PLLn_AVDD input (see Figure 37) in which the following components are defined as listed:

- R = 5 Ω ± 5%
- C1 = 10 µF ± 10%, 0603, X5R, with ESL ≤ 0.5 nH, low ESL Surface Mount Capacitor.
- C2 = 1.0 µF ± 10%, 0402, X5R, with ESL ≤ 0.5 nH, low ESL Surface Mount Capacitor.

Note: A higher capacitance value for C2 may be used to improve the filter as long as the other C2 parameters do not change.

All three PLLs can connect to a single supply voltage source (such as a voltage regulator) as long as the external RC filter is applied to each PLL separately. For optimal noise filtering, place the circuit as close as possible to its PLLn_AVDD inputs.

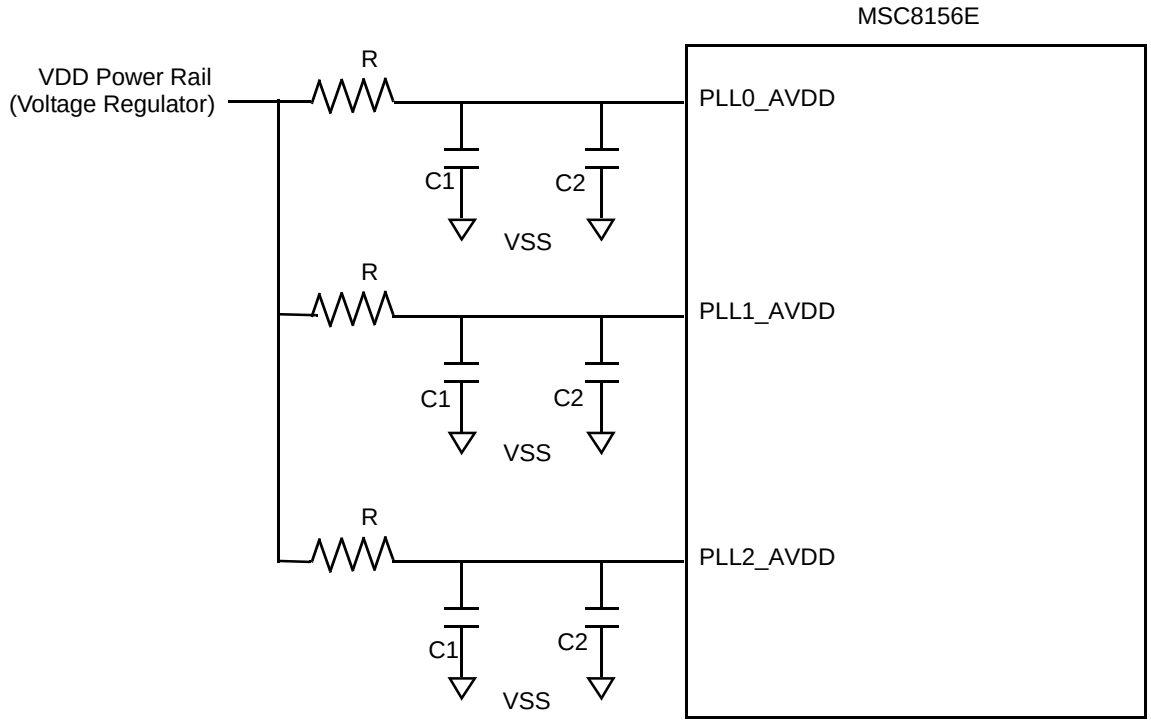


Figure 37. PLL Supplies

Each SerDes PLL power supply must be filtered using a circuit similar to the one shown in Figure 38, to ensure stability of the internal clock. For maximum effectiveness, the filter circuit should be placed as closely as possible to the SRn_PLL_AVDD ball to ensure it filters out as much noise as possible. The ground connection should be near the SRn_PLL_AVDD ball. The 0.003 µF capacitor is closest to the ball, followed by the two 2.2 µF capacitors, and finally the 1 Ω resistor to the board supply plane. The capacitors are connected from SRn_PLL_AVDD to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All trances should be kept short, wide, and direct.

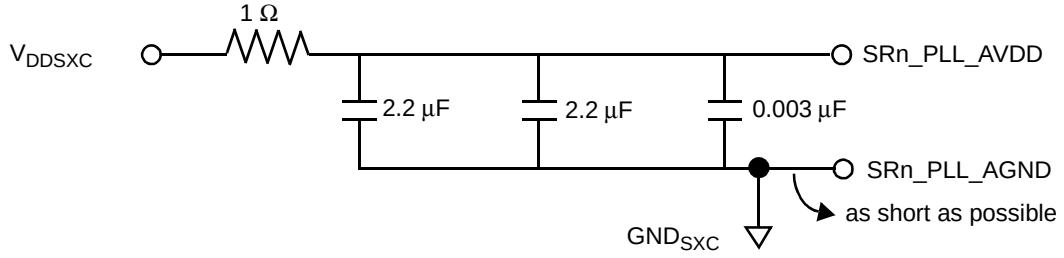


Figure 38. SerDes PLL Supplies

3.5.1.4 DDR2 Unused MAPAR Pin Connections

When the MAPAR signals are not used, refer to Table 43 to determine the correct pin connections.

Table 43. Connectivity of MAPAR Pins for DDR2

Signal Name	Pin connection
MAPAR_OUT	NC
$\overline{\text{MAPAR\_IN}}$	NC

Notes: 1. For the signals listed in this table, the initial M stands for M1 or M2 depending on which DDR controller is used for DDR2.
2. For MSC8156 Revision 1 silicon, these pins were connected to GND. For newer revisions of the MSC8156, connecting these pins to GND increases device power consumption.

3.5.2 HSSI-Related Pins

3.5.2.1 HSSI Port Is Not Used

The signal names in Table 44 and Table 45 are generic names for a RapidIO interface. For actual pin names refer to Table 1.

Table 44. Connectivity of Serial RapidIO Interface Related Pins When the RapidIO Interface Is Not Used

Signal Name	Pin Connection
SR_IMP_CAL_RX	NC
SR_IMP_CAL_TX	NC
$\overline{\text{SR[1–2]\_REF\_CLK}}$	SXCVSS
SR[1–2]_REF_CLK	SXCVSS
SR[1–2]_RXD[3–0]	SXCVSS
$\overline{\text{SR[1–2]\_RXD[3–0]}}$	SXCVSS
$\overline{\text{SR[1–2]\_TXD[3–0]}}$	NC
SR[1–2]_TXD[3–0]	NC
SR[1–2]_PLL_AVDD	In use
SR[1–2]_PLL_AGND	In use
SXPVSS	In use
SXCVSS	In use
SXPVDD	In use
SXCVDD	In use

Note: All lanes in the HSSI SerDes should be powered down. Refer to the *MSC8156 Reference Manual* for details.

3.5.2.2 HSSI Specific Lane Is Not Used

Table 45. Connectivity of HSSI Related Pins When Specific Lane Is Not Used

Signal Name	Pin Connection
SR_IMP_CAL_RX	In use
SR_IMP_CAL_TX	In use
$\overline{\text{SR[1–2]\_REF\_CLK}}$	In use
SR[1–2]_REF_CLK	In use

3.6 Guide to Selecting Connections for Remote Power Supply Sensing

To assure consistency of input power levels, some applications use a practice of connecting the remote sense signal input of an on-board power supply to one of power supply pins of the IC device. The advantage of using this connection is the ability to compensate for the slow components of the IR drop caused by resistive supply current path from on-board power supply to the pins layer on the package. However, because of specific device requirements, not every ball connection can be selected as the remote sense pin. Some of these pins must be connected to the appropriate power supply or ground to ensure correct device functionality. Some connections supply critical power to a specific high usage area of the IC die; using such a connection as a non-supply pin could impact necessary supply current during high current events. The following balls can be used as the board supply remote sense output without degrading the power and ground supply quality:

- *VDD:* W10, T19
- *VSS:* J18, Y10
- *M3VDD:* None

Do not use any other connections for remote sensing. Use of any other connections for this purpose can result in application and device failure.

4 Ordering Information

Consult a Freescale Semiconductor sales office or authorized distributor to determine product availability and place an order.

Part	Package Type	Spheres	Core Voltage	Operating Temperature	Core Frequency (MHz)	Order Number
MSC8156	Flip Chip Plastic Ball Grid Array (FC-PBGA)	Lead-free	1.0 V	0° C to 105°C	1000	MSC8156SVT1000B
				–40° to 105°C	1000	MSC8156TVT1000B