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Understanding [Embedded - DSP \(Digital Signal Processors\)](#)

[Embedded - DSP \(Digital Signal Processors\)](#) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of [Embedded - DSP \(Digital Signal Processors\)](#)

Details

Product Status	Obsolete
Type	SC3850 Six Core
Interface	Ethernet, I ² C, PCI, RGMII, Serial RapidIO, SGMII, SPI, UART/USART
Clock Rate	1GHz
Non-Volatile Memory	ROM (96kB)
On-Chip RAM	576kB
Voltage - I/O	2.50V
Voltage - Core	1.00V
Operating Temperature	0°C ~ 90°C (TJ)
Mounting Type	Surface Mount
Package / Case	-
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=msc8156vt1000b

1 Pin Assignment

This section includes diagrams of the MSC8156 package ball grid array layouts and tables showing how the pinouts are allocated for the package.

1.1 FC-PBGA Ball Layout Diagram

The top view of the FC-PBGA package is shown in Figure 3 with the ball location index numbers.

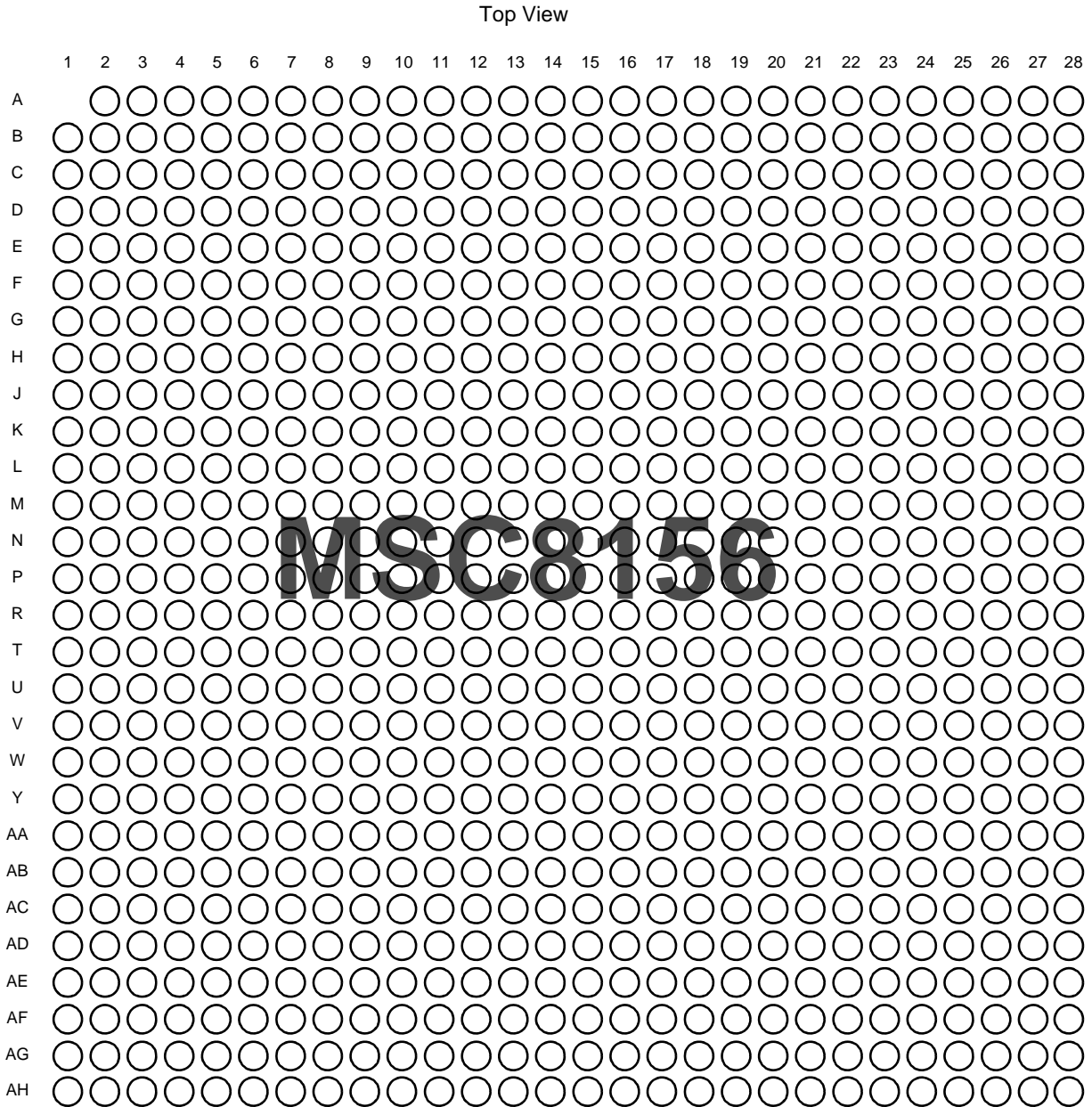


Figure 3. MSC8156 FC-PBGA Package, Top View

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name ^{1,2}	Pin Type ¹⁰	Power Rail Name
B9	M2A13	O	GVDD2
B10	VSS	Ground	N/A
B11	GVDD2	Power	N/A
B12	M2CS1	O	GVDD2
B13	VSS	Ground	N/A
B14	GVDD2	Power	N/A
B15	M2DQ35	I/O	GVDD2
B16	VSS	Ground	N/A
B17	GVDD2	Power	N/A
B18	M2DQ51	I/O	GVDD2
B19	VSS	Ground	N/A
B20	GVDD2	Power	N/A
B21	Reserved	NC	—
B22	Reserved	NC	—
B23	SR1_TXD0	O	SXPVDD1
B24	SR1_TXD0	O	SXPVDD1
B25	SXCVDD1	Power	N/A
B26	SXCVSS1	Ground	N/A
B27	SR1_RXD0	I	SXCVDD1
B28	SR1_RXD0	I	SXCVDD1
C1	M2DQ28	I/O	GVDD2
C2	M2DM3	O	GVDD2
C3	M2DQ26	I/O	GVDD2
C4	M2ECC4	I/O	GVDD2
C5	M2DM8	O	GVDD2
C6	M2ECC2	I/O	GVDD2
C7	M2CKE1	O	GVDD2
C8	M2CK0	O	GVDD2
C9	M2CK0	O	GVDD2
C10	M2BA1	O	GVDD2
C11	M2A1	O	GVDD2
C12	M2WE	O	GVDD2
C13	M2DQ37	I/O	GVDD2
C14	M2DM4	O	GVDD2
C15	M2DQ36	I/O	GVDD2
C16	M2DQ32	I/O	GVDD2
C17	M2DQ55	I/O	GVDD2
C18	M2DM6	O	GVDD2
C19	M2DQ53	I/O	GVDD2
C20	M2DQ52	I/O	GVDD2
C21	Reserved	NC	—
C22	SR1_IMP_CAL_RX	I	SXCVDD1
C23	SXPVSS1	Ground	N/A
C24	SXPVDD1	Power	N/A
C25	SR1_REF_CLK	I	SXCVDD1
C26	SR1_REF_CLK	I	SXCVDD1

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name ^{1,2}	Pin Type ¹⁰	Power Rail Name
G7	M2CKE0	O	GVDD2
G8	M2A11	O	GVDD2
G9	M2A7	O	GVDD2
G10	M2CK2	O	GVDD2
G11	M2APAR_OUT	O	GVDD2
G12	M2ODT1	O	GVDD2
G13	M2APAR_IN	I	GVDD2
G14	M2DQ43	I/O	GVDD2
G15	M2DM5	O	GVDD2
G16	M2DQ44	I/O	GVDD2
G17	M2DQ40	I/O	GVDD2
G18	M2DQ59	I/O	GVDD2
G19	M2DM7	O	GVDD2
G20	M2DQ60	I/O	GVDD2
G21	Reserved	NC	—
G22	Reserved	NC	—
G23	SXPVSS1	Ground	N/A
G24	SXPVDD1	Power	N/A
G25	SR1_IMP_CAL_TX	I	SXCVDD1
G26	SXCVSS1	Ground	N/A
G27	Reserved	NC	—
G28	Reserved	NC	—
H1	GVDD2	Power	N/A
H2	VSS	Ground	N/A
H3	M2DQ18	I/O	GVDD2
H4	GVDD2	Power	N/A
H5	VSS	Ground	N/A
H6	M2DQ20	I/O	GVDD2
H7	GVDD2	Power	N/A
H8	VSS	Ground	N/A
H9	M2A15	O	GVDD2
H10	M2CK2	O	GVDD2
H11	M2MDIC0	I/O	GVDD2
H12	M2VREF	I	GVDD2
H13	M2MDIC1	I/O	GVDD2
H14	M2DQ46	I/O	GVDD2
H15	M2DQ47	I/O	GVDD2
H16	M2DQ45	I/O	GVDD2
H17	M2DQ41	I/O	GVDD2
H18	M2DQ62	I/O	GVDD2
H19	M2DQ63	I/O	GVDD2
H20	M2DQ61	I/O	GVDD2
H21	Reserved	NC	—
H22	Reserved	NC	—
H23	SR1_TXD3/SG2_TX ⁴	O	SXPVDD1
H24	SR1_TXD3/SG2_TX ⁴	O	SXPVDD1

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name ^{1,2}	Pin Type ¹⁰	Power Rail Name
K15	VDD	Power	N/A
K16	VSS	Ground	N/A
K17	VDD	Power	N/A
K18	VSS	Ground	N/A
K19	VDD	Power	N/A
K20	Reserved	NC	—
K21	Reserved	NC	—
K22	Reserved	NC	—
K23	SXPVDD2	Power	N/A
K24	SXPVSS2	Ground	N/A
K25	SXCVDD2	Power	N/A
K26	SXCVSS2	Ground	N/A
K27	SXCVDD2	Power	N/A
K28	SXCVSS2	Ground	N/A
L1	M2DQ9	I/O	GVDD2
L2	M2DQ12	I/O	GVDD2
L3	M2DQ13	I/O	GVDD2
L4	M2DQS0	I/O	GVDD2
L5	M2DQS0	I/O	GVDD2
L6	M2DM0	O	GVDD2
L7	M2DQ3	I/O	GVDD2
L8	M2DQ2	I/O	GVDD2
L9	M2DQ4	I/O	GVDD2
L10	VDD	Power	N/A
L11	VSS	Ground	N/A
L12	M3VDD	Power	N/A
L13	VSS	Ground	N/A
L14	VDD	Power	N/A
L15	VSS	Ground	N/A
L16	VDD	Power	N/A
L17	VSS	Ground	N/A
L18	VDD	Power	N/A
L19	VSS	Ground	N/A
L20	Reserved	NC	—
L21	Reserved	NC	—
L22	Reserved	NC	—
L23	SR2_TXD3/PE_TXD3/SG2_TX ⁴	O	SXPVDD2
L24	SR2_TXD3/PE_TXD3/SG2_TX ⁴	O	SXPVDD2
L25	SXCVSS2	Ground	N/A
L26	SXCVDD2	Power	N/A
L27	SR2_RXD3/PE_RXD3/SG2_RX ⁴	I	SXCVDD2
L28	SR2_RXD3/PE_RXD3/SG2_RX ⁴	I	SXCVDD2
M1	M2DQ8	I/O	GVDD2
M2	VSS	Ground	N/A
M3	GVDD2	Power	N/A
M4	M2DQ15	I/O	GVDD2

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name ^{1,2}	Pin Type ¹⁰	Power Rail Name
N23	SR2_TXD2/PE_TXD2/SG1_TX ⁴	O	SXPVDD2
N24	$\overline{\text{SR2_TXD2/PE_TXD2/SG1_TX}}^4$	O	SXPVDD2
N25	SXCVDD2	Power	N/A
N26	SXCVSS2	Ground	N/A
N27	SR2_RXD2/PE_RXD2/SG1_RX ⁴	I	SXCVDD2
N28	$\overline{\text{SR2_RXD2/PE_RXD2/SG1_RX}}^4$	I	SXCVDD2
P1	CLKIN	I	QVDD
P2	EE0	I	QVDD
P3	QVDD	Power	N/A
P4	VSS	Ground	N/A
P5	STOP_BS	I	QVDD
P6	QVDD	Power	N/A
P7	VSS	Ground	N/A
P8	PLL0_AVDD ⁹	Power	VDD
P9	PLL2_AVDD ⁹	Power	VDD
P10	VSS	Ground	N/A
P11	VDD	Power	N/A
P12	VSS	Ground	N/A
P13	VDD	Power	N/A
P14	VSS	Ground	N/A
P15	MVDD	Power	N/A
P16	VSS	Ground	N/A
P17	MVDD	Power	N/A
P18	VSS	Ground	N/A
P19	VDD	Power	N/A
P20	Reserved	NC	—
P21	Reserved	NC	—
P22	Reserved	NC	—
P23	SXPVDD2	Power	N/A
P24	SXPVSS2	Ground	N/A
P25	SR2_PLL_AGND ⁹	Ground	SXCVSS2
P26	SR2_PLL_AVDD ⁹	Power	SXCVDD2
P27	SXCVSS2	Ground	N/A
P28	SXCVDD2	Power	N/A
R1	VSS	Ground	N/A
R2	NMI	I	QVDD
R3	$\overline{\text{NMI_OUT}}^6$	O	QVDD
R4	$\overline{\text{HRESET}}^{6,7}$	I/O	QVDD
R5	$\overline{\text{INT_OUT}}^6$	O	QVDD
R6	EE1	O	QVDD
R7	VSS	Ground	N/A
R8	PLL1_AVDD ⁹	Power	VDD
R9	VSS	Ground	N/A
R10	VDD	Power	N/A
R11	VSS	Non-user	N/A
R12	VDD	Power	N/A

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name ^{1,2}	Pin Type ¹⁰	Power Rail Name
Y11	GVDD1	Power	N/A
Y12	VSS	Ground	N/A
Y13	GVDD1	Power	N/A
Y14	VSS	Ground	N/A
Y15	GVDD1	Power	N/A
Y16	VSS	Ground	N/A
Y17	GVDD1	Power	N/A
Y18	VSS	Ground	N/A
Y19	GVDD1	Power	N/A
Y20	VSS	Ground	N/A
Y21	NVDD	Power	N/A
Y22	GPIO20/SPI_SL ^{5,8}	I/O	NVDD
Y23	GPIO17/SPI_SCK ^{5,8}	I/O	NVDD
Y24	GPIO14/DRQ0/IRQ14/RC14 ^{5,8}	I/O	NVDD
Y25	GPIO12/IRQ12/RC12 ^{5,8}	I/O	NVDD
Y26	GPIO8/IRQ8/RC8 ^{5,8}	I/O	NVDD
Y27	NVDD	Power	N/A
Y28	VSS	Ground	N/A
AA1	GVDD1	Power	N/A
AA2	VSS	Ground	N/A
AA3	M1DQ18	I/O	GVDD1
AA4	GVDD1	Power	N/A
AA5	VSS	Ground	N/A
AA6	M1DQ20	I/O	GVDD1
AA7	GVDD1	Power	N/A
AA8	VSS	Ground	N/A
AA9	M1A15	O	GVDD1
AA10	M1CK2	O	GVDD1
AA11	M1MDIC0	I/O	GVDD1
AA12	M1VREF	I	GVDD1
AA13	M1MDIC1	I/O	GVDD1
AA14	M1DQ46	I/O	GVDD1
AA15	M1DQ47	I/O	GVDD1
AA16	M1DQ45	I/O	GVDD1
AA17	M1DQ41	I/O	GVDD1
AA18	M1DQ62	I/O	GVDD1
AA19	M1DQ63	I/O	GVDD1
AA20	M1DQ61	I/O	GVDD1
AA21	VSS	Ground	N/A
AA22	GPIO21 ^{5,8}	I/O	NVDD
AA23	GPIO18/SPI_MOSI ^{5,8}	I/O	NVDD
AA24	GPIO16/RC16 ^{5,8}	I/O	NVDD
AA25	GPIO4/DDN1/IRQ4/RC4 ^{5,8}	I/O	NVDD
AA26	GPIO9/IRQ9/RC9 ^{5,8}	I/O	NVDD
AA27	GPIO6/IRQ6/RC6 ^{5,8}	I/O	NVDD
AA28	GPIO1/IRQ1/RC1 ^{5,8}	I/O	NVDD

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name ^{1,2}	Pin Type ¹⁰	Power Rail Name
AH17	M1DQS $\bar{6}$	I/O	GVDD1
AH18	M1DQS6	I/O	GVDD1
AH19	M1DQ48	I/O	GVDD1
AH20	M1DQ49	I/O	GVDD1
AH21	VSS	Ground	N/A
AH22	TDM0RCK/GE2_RD2 ³	I/O	NVDD
AH23	TDM0RDT/GE2_RD3 ³	I/O	NVDD
AH24	TDM0TSN/GE2_RD0 ³	I/O	NVDD
AH25	TDM1RCK/GE2_RD1 ³	I/O	NVDD
AH26	TDM3TDT/GE1_RD3 ³	I/O	NVDD
AH27	TDM3TCK/GE1_RD2 ³	I	NVDD
AH28	VSS	Ground	N/A
Notes:	<ol style="list-style-type: none"> 1. Reserved signals should be disconnected for compatibility with future revisions of the device. Non-user signals are reserved for manufacturing and test purposes only. The assigned signal name is used to indicate whether the signal must be unconnected (Reserved), pulled down (VSS), or pulled up (VDD). 2. Signal function during power-on reset is determined by the RCW source type. 3. Selection of TDM versus RGMII functionality is determined by the RCW bit values. 4. Selection of RapidIO, SGMII, and PCI Express functionality is determined by the RCW bit values. 5. Selection of the GPIO function and other functions is done by GPIO register setup. For configuration details, see the <i>GPIO</i> chapter in the <i>MSC8156 Reference Manual</i>. 6. Open-drain signal. 7. Internal 20 KΩ pull-up resistor. 8. For signals with GPIO functionality, the open-drain and internal 20 KΩ pull-up resistor can be configured by GPIO register programming. See the <i>GPIO</i> chapter of the <i>MSC8156 Reference Manual</i> for configuration details. 9. Connect to power supply via external filter. See Section 3.2, PLL Power Supply Design Considerations for details. 10. Pin types are: Ground = all VSS connections; Power = all VDD connections; I = Input; O = Output; I/O = Input/Output; NC = not connected. 		

2.2 Recommended Operating Conditions

Table 3 lists recommended operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 3. Recommended Operating Conditions

Rating	Symbol	Min	Nominal	Max	Unit
Core supply voltage	V_{DD}	0.97	1.0	1.05	V
M3 memory supply voltage	V_{DDM3}	0.97	1.0	1.05	V
MAPLE-B supply voltage	V_{DDM}	0.97	1.0	1.05	V
DDR memory supply voltage	V_{DDDDR}	1.7	1.8	1.9	V
• DDR2 mode		1.425	1.5	1.575	V
• DDR3 mode		$0.49 \times V_{DDDDR}$	$0.5 \times V_{DDDDR}$	$0.51 \times V_{DDDDR}$	V
DDR reference voltage	MV_{REF}				V
I/O voltage excluding DDR and RapidIO lines	V_{DDIO}	2.375	2.5	2.625	V
Rapid I/O pad voltage	V_{DDSP}	0.97	1.0	1.05	V
Rapid I/O core voltage	V_{DDSC}	0.97	1.0	1.05	V
Operating temperature range:					
• Standard	T_J	0		90	°C
• Higher	T_J	0		105	°C
• Extended	T_A	-40		—	°C
	T_J	—		105	°C

2.5.1.3 DDR2/DDR3 SDRAM Capacitance

Table 8 provides the DDR controller interface capacitance for DDR2 and DDR3 memory.

Note: At recommended operating conditions (see Table 3) with $V_{DDDDR} = 1.8\text{ V}$ for DDR2 memory or $V_{DDDDR} = 1.5\text{ V}$ for DDR3 memory.

Table 8. DDR2/DDR3 SDRAM Capacitance

Parameter	Symbol	Min	Max	Unit
I/O capacitance: DQ, DQS, $\overline{\text{DQS}}$	C_{IO}	6	8	pF
Delta I/O capacitance: DQ, DQS, $\overline{\text{DQS}}$	C_{DIO}	—	0.5	pF
Note: Guaranteed by FAB process and micro-construction.				

2.5.1.4 DDR Reference Current Draw

Table 9 lists the current draw characteristics for MV_{REF} .

Note: Values when used at recommended operating conditions (see Table 3).

Table 9. Current Draw Characteristics for MV_{REF}

Parameter / Condition	Symbol	Min	Max	Unit
Current draw for MV_{REFn}	I_{MVREFn}	—		
• DDR2 SDRAM			300	μA
• DDR3 SDRAM			250	μA

2.5.2 High-Speed Serial Interface (HSSI) DC Electrical Characteristics

The MSC8156 features an HSSI that includes two 4-channel SerDes ports used for high-speed serial interface applications (PCI Express, Serial RapidIO interfaces, and SGMII). This section and its subsections describe the common portion of the SerDes DC, including the DC requirements for the SerDes reference clocks and the SerDes data lane transmitter (Tx) and receiver (Rx) reference circuits. The data lane circuit specifications are specific for each supported interface, and they have individual subsections by protocol. The selection of individual data channel functionality is done via the Reset Configuration Word High Register (RCWHR) SerDes Protocol selection fields (S1P and S2P). Specific AC electrical characteristics are defined in Section 2.6.2, “HSSI AC Timing Specifications.”

2.5.2.1 Signal Term Definitions

The SerDes interface uses differential signalling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals. Figure 4 shows how the signals are defined. For illustration purposes only, one SerDes lane is used in the description. Figure 4 shows the waveform for either a transmitter output (SR[1–2]_TX and

Table 21. DDR SDRAM Output AC Timing Specifications (continued)

Parameter	Symbol ¹	Min	Max	Unit	Notes
<p>Notes:</p> <ol style="list-style-type: none"> The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, MCS, and MDQ/MECC/MDM/MDQS. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK(n) clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This will typically be set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these two parameters have been set to the same adjustment value. See the <i>MSC8156 Reference Manual</i> for a description and understanding of the timing modifications enabled by use of these bits. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the MSC8156. At recommended operating conditions with V_{DDDDR} (1.5 V or 1.8 V) \pm 5%. 					

Note: For the ADDR/CMD setup and hold specifications in Table 21, it is assumed that the clock control register is set to adjust the memory clocks by 1/2 applied cycle.

Figure 12 shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

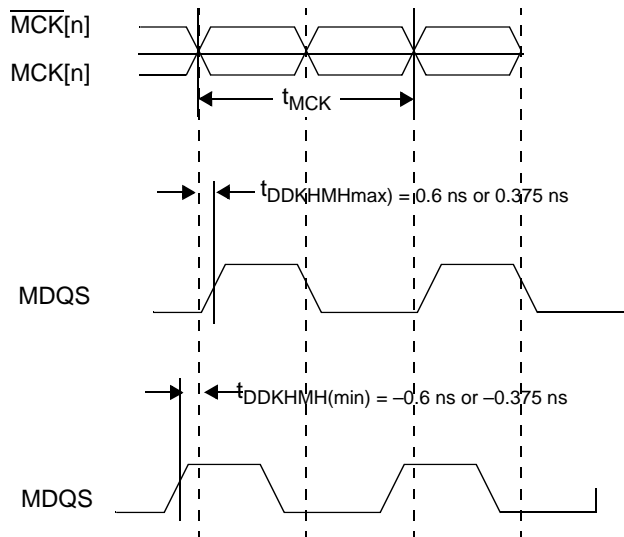


Figure 12. MCK to MDQS Timing

2.6.2.4 SGMII AC Timing Specifications

Note: Specifications are valid at the recommended operating conditions listed in Table 3.

Transmitter and receiver AC characteristics are measured at the transmitter outputs (SR[1-2]_TX[n] and $\overline{\text{SR[1-2]_TX[n]}}$) or at the receiver inputs (SR[1-2]_RX[n] and $\overline{\text{SR[1-2]_RX[n]}}$) as depicted in Figure 19, respectively.

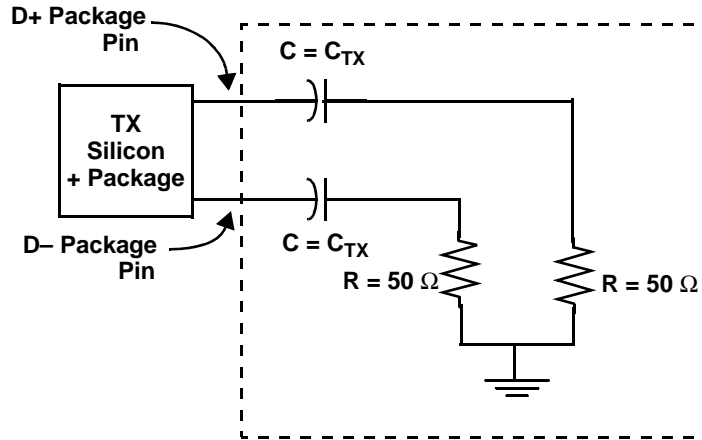


Figure 19. SGMII AC Test/Measurement Load

Table 29 provides the SGMII transmit AC timing specifications. A source synchronous clock is not supported. The AC timing specifications do not include REF_CLK jitter.

Table 29. SGMII Transmit AC Timing Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic Jitter	JD	—	—	0.17	UI p-p	—
Total Jitter	JT	—	—	0.35	UI p-p	2
Unit Interval	UI	799.92	800	800.08	ps	1
Notes:						
1. See Figure 18 for single frequency sinusoidal jitter limits						
2. Each UI is 800 ps ± 100 ppm.						

Table 30 provides the SGMII receiver AC timing specifications. The AC timing specifications do not include REF_CLK jitter.

Table 30. SGMII Receive AC Timing Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic Jitter Tolerance	JD	0.37	—	—	UI p-p	1, 2
Combined Deterministic and Random Jitter Tolerance	JDR	0.55	—	—	UI p-p	1, 2
Total Jitter Tolerance	JT	0.65	—	—	UI p-p	1,2
Bit Error Ratio	BER	—	—	10 ⁻¹²	—	—
Unit Interval	UI	799.92	800.00	800.08	ps	3
Notes:						
1. Measured at receiver.						
2. Refer to RapidIO™ 1x/4x LP Serial Physical Layer Specification for interpretation of jitter specifications. Also see Figure 18.						
3. Each UI is 800 ps ± 100 ppm.						

Electrical Characteristics

Figure 21 shows the TDM transmit signal timing.

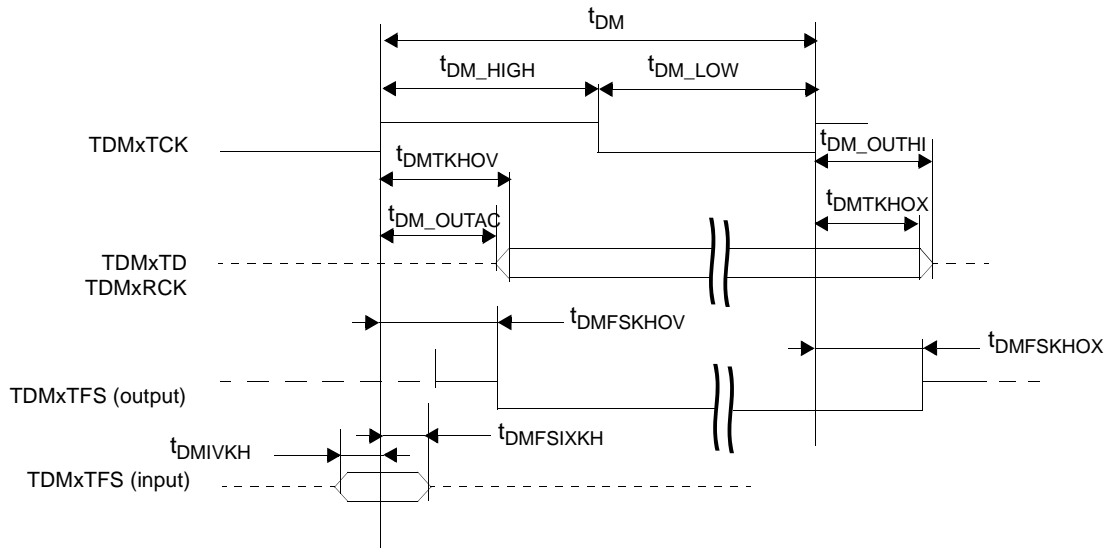


Figure 21. TDM Transmit Signals

Figure 22 provides the AC test load for the TDM/SI.

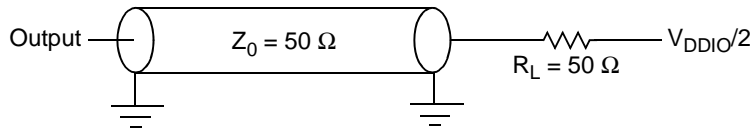


Figure 22. TDM AC Test Load

2.6.4 Timers AC Timing Specifications

Table 32 lists the timer input AC timing specifications.

Table 32. Timers Input AC Timing Specifications

Characteristics	Symbol	Minimum	Unit	Notes
Timers inputs—minimum pulse width	T_{TIWID}	8	ns	1, 2
Notes: <ol style="list-style-type: none"> The maximum allowed frequency of timer outputs is 125 MHz. Configure the timer modules appropriately. Timer inputs and outputs are asynchronous to any visible clock. Timer outputs should be synchronized before use by any external synchronous logic. Timer inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation. 				

Note: For recommended operating conditions, see Table 3.

Figure 23 shows the AC test load for the timers.

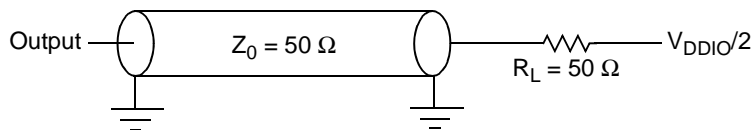


Figure 23. Timer AC Test Load

2.6.5.2 RGMII AC Timing Specifications

Table 34 presents the RGMII AC timing specifications for applications requiring an on-board delayed clock.

Table 34. RGMII at 1 Gbps² with On-Board Delay³ AC Timing Specifications

Parameter/Condition	Symbol	Min	Typ	Max	Unit
Data to clock output skew (at transmitter) ⁴	t_{SKEWT}	-0.5	—	0.5	ns
Data to clock input skew (at receiver) ⁴	t_{SKEWR}	1	—	2.6	ns
Notes: <ol style="list-style-type: none"> 1. At recommended operating conditions with V_{DDIO} of 2.5 V \pm 5%. 2. RGMII at 100 Mbps support is guaranteed by design. 3. Program GCR4 as 0x00000000. 4. This implies that PC board design requires clocks to be routed such that an additional trace delay of greater than 1.5 ns and less than 2.0 ns is added to the associated clock signal. 					

Table 35 presents the RGMII AC timing specification for applications required non-delayed clock on board.

Table 35. RGMII at 1 Gbps² with No On-Board Delay³ AC Timing Specifications

Parameter/Condition	Symbol	Min	Typ	Max	Unit
Data to clock output skew (at transmitter) ⁴	t_{SKEWT}	-2.6	—	-1.0	ns
Data to clock input skew (at receiver) ⁴	t_{SKEWR}	-0.5	—	0.5	ns
Notes: <ol style="list-style-type: none"> 1. At recommended operating conditions with V_{DDIO} of 2.5 V \pm 5%. 2. RGMII at 100 Mbps support is guaranteed by design. 3. GCR4 should be programmed as 0x000CC330. 4. This implies that PC board design requires clocks to be routed with no additional trace delay 					

Figure 25 shows the RGMII AC timing and multiplexing diagrams.

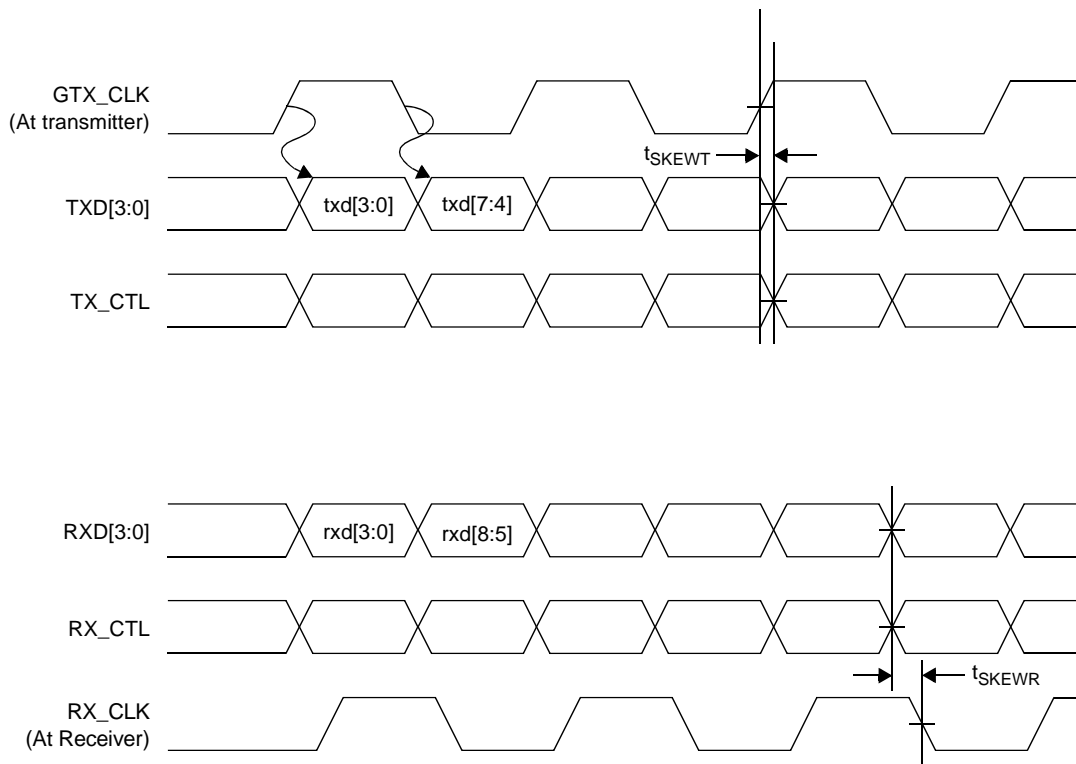
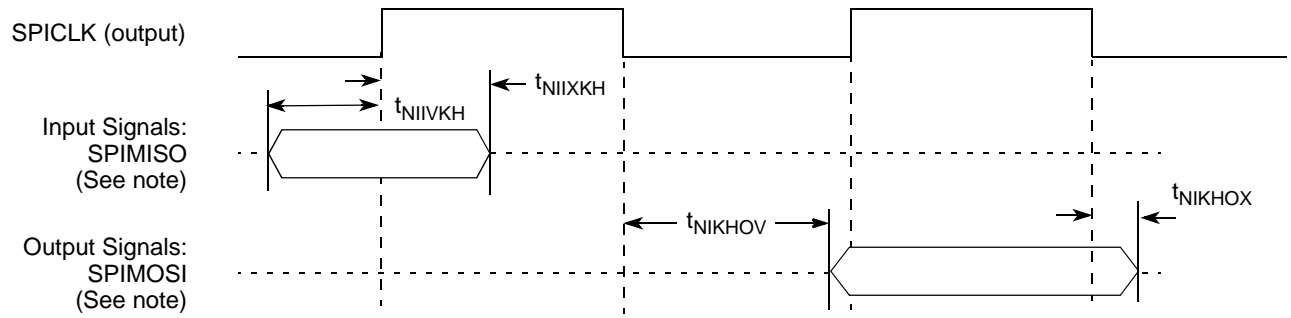


Figure 25. RGMII AC Timing and Multiplexing



Note: measured with SPMODE[CI] = 0, SPMODE[CP] = 0

Figure 28. SPI AC Timing in Master Mode (Internal Clock)

3 Hardware Design Considerations

The following sections discuss areas to consider when the MSC8156 device is designed into a system.

3.1 Power Supply Ramp-Up Sequence

The following subsections describe the required device initialization sequence.

3.1.1 Clock, Reset, and Supply Coordination

Starting the device requires coordination between several inputs including: clock, reset, and power supplies. Follow this guidelines when starting up an MSC8156 device:

- $\overline{\text{PORESET}}$ and $\overline{\text{TRST}}$ must be asserted externally for the duration of the supply ramp-up, using the V_{DDIO} supply. $\overline{\text{TRST}}$ deassertion does not have to be synchronized with $\overline{\text{PORESET}}$ deassertion. However, $\overline{\text{TRST}}$ must be deasserted before normal operation begins to ensure correct functionality of the device.
- CLKIN should toggle at least 32 cycles before $\overline{\text{PORESET}}$ deassertion to guarantee correct device operation. The 32 cycles should only be counted from the time after V_{DDIO} reaches its nominal value (see timing 1 in Figure 33).
- CLKIN should either be stable low during ramp-up of V_{DDIO} supply (and start its swings after ramp-up) or should swing within V_{DDIO} range during V_{DDIO} ramp-up, so its amplitude grows as V_{DDIO} grows during ramp-up.

Figure 33 shows a sequence in which V_{DDIO} ramps-up after V_{DD} and CLKIN begins to toggle with the raise of V_{DDIO} supply.

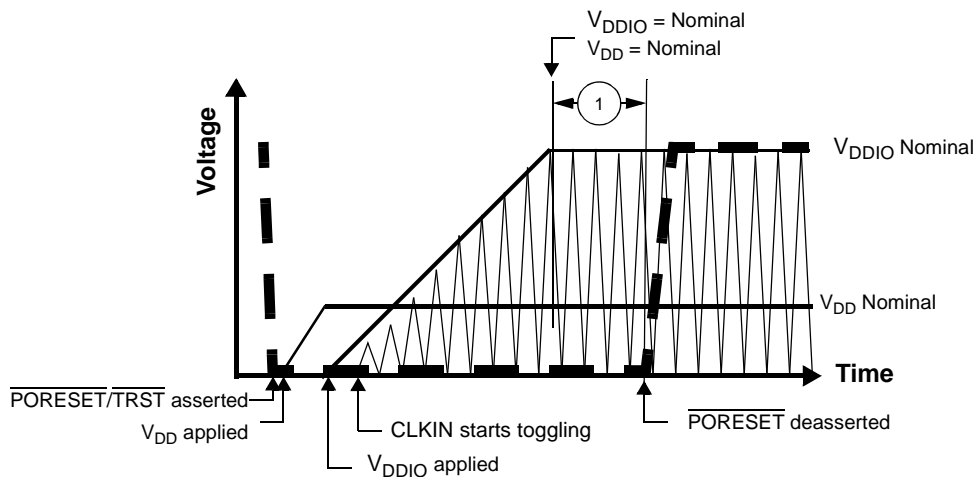


Figure 33. Supply Ramp-Up Sequence with V_{DD} Ramping Before V_{DDIO} and CLKIN Starting With V_{DDIO}

Note: For details on power-on reset flow and duration, see the *Reset* chapter in the *MSC8156 Reference Manual*.

3.1.2 Power-On Ramp Time

This section describes the AC electrical specification for the power-on ramp rate requirements for all voltage supplies (including GVDD/SXPVDD/SXCVDD/QVDD/GVDD/NVDD, all VDD supplies, MVREF, and all AVDD supplies). Controlling the power-on ramp time is required to avoid falsely triggering the ESD circuitry. Table 39 defines the power supply ramp time specification.

Table 39. Power Supply Ramp Rate

Parameter	Min	Max	Unit
Required ramp rate.	—	36000	V/s
Notes: <ol style="list-style-type: none"> 1. Ramp time is specified as a linear ramp from 10% to 90% of nominal voltage of the specific voltage supply. If the ramp is non-linear (for example, exponential), the maximum rate of change from 200 to 500 mV is the most critical because this range might falsely trigger the ESD circuitry. 2. Required over the full recommended operating temperature range (see Table 3). 3. All supplies must be at their stable values within 50 ms. 4. The GVDD pins can be held low on the application board at powerup. If GVDD is not held low, then GVDD will rise to a voltage level that depends on the board-level impedance-to-ground. If the impedance is high (that is, infinite), then theoretically, GVDD can rise up close to the VDD levels. 			

3.1.3 Power Supply Guidelines

Use the following guidelines for power-up sequencing:

- Couple M3VDD with the VDD power rail using an extremely low impedance path.
- Couple inputs PLL1_AVDD, PLL2_AVDD and PLL3_AVDD with the VDD power rail using an RC filter (see Figure 37).
- There is no dependency in power-on/power-off sequence between the GVDD1, GVDD2, NVDD, and QVDD power rails.
- Couple inputs M1VREF and M2VREF with the GVDD1 and GVDD2 power rails, respectively. They should rise at the same time as or after their respective power rail.
- There is no dependency between RapidIO supplies: SXCVDD1, SXCVDD2, SXPVDD1 and SXPVDD2 and other MSC8156 supplies in the power-on/power-off sequence
- Couple inputs SR1_PLL_AVDD and SR2_PLL_AVDD with SXCVDD1 and SXCVDD2 power rails, respectively, using an RC filter (see Figure 38).

External voltage applied to any input line must not exceed the I/O supply voltage related to this line by more than 0.6 V at any time, including during power-up. Some designs require pull-up voltages applied to selected input lines during power-up for configuration purposes. This is an acceptable exception to the rule during start-up. However, each such input can draw up to 80 mA per input pin per MSC8156 device in the system during power-up. An assertion of the inputs to the high voltage level before power-up should be with slew rate less than 4 V/ns.

The device power rails should rise in the following sequence:

1. VDD (and all coupled supplies)

3.3 Clock and Timing Signal Board Layout Considerations

When laying out the system board, use the following guidelines:

- Keep clock and timing signal paths as short as possible and route with 50 Ω impedance.
- Use a serial termination resistor placed close to the clock buffer to minimize signal reflection. Use the following equation to compute the resistor value:

$$R_{\text{term}} = R_{\text{im}} - R_{\text{buf}}$$

where R_{im} = trace characteristic impedance

R_{buf} = clock buffer internal impedance.

3.4 SGMII AC-Coupled Serial Link Connection Example

Figure 39 shows an example of a 4-wire AC-coupled serial link connection. For additional layout suggestions, see *AN3556 MSC815x High Speed Serial Interface Hardware Design Considerations*, available on the Freescale website or from your local sales office or representative.

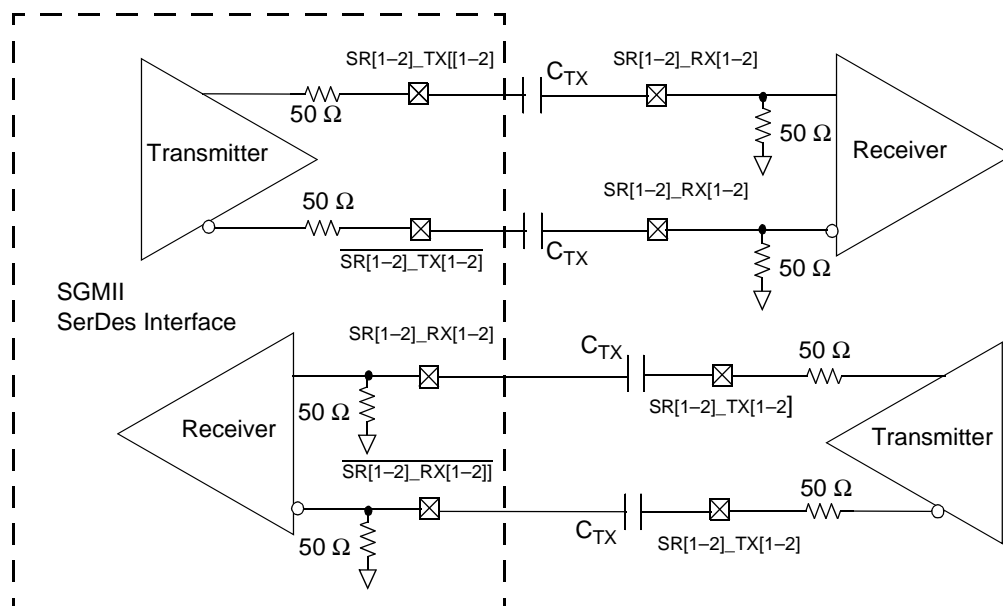


Figure 39. 4-Wire AC-Coupled SGMII Serial Link Connection Example

3.5.1 DDR Memory Related Pins

This section discusses the various scenarios that can be used with either of the MSC8156 DDR ports.

Note: The signal names in Table 40, Table 41 and Table 42 are generic names for a DDR SDRAM interface. For actual pin names refer to Table 1.

3.5.1.1 DDR Interface Is Not Used

Table 40. Connectivity of DDR Related Pins When the DDR Interface Is Not Used

Signal Name	Pin Connection
MDQ[0–63]	NC
MDQS[7–0]	NC
$\overline{\text{MDQS}}[7–0]$	NC
MA[15–0]	NC
MCK[0–2]	NC
$\overline{\text{MCK}}[0–2]$	NC
$\overline{\text{MCS}}[1–0]$	NC
MDM[7–0]	NC
MBA[2–0]	NC
$\overline{\text{MCAS}}$	NC
MCKE[1–0]	NC
MODT[1–0]	NC
MMDIC[1–0]	NC
$\overline{\text{MRAS}}$	NC
$\overline{\text{MWE}}$	NC
MECC[7–0]	NC
MDM8	NC
MDQS8	NC
$\overline{\text{MDQS}}8$	NC
MAPAR_OUT	NC
$\overline{\text{MAPAR}}_{\text{IN}}$	NC
MVREF ³	NC
GVDD1/GVDD2 ³	NC
<p>Notes:</p> <ol style="list-style-type: none"> 1. For the signals listed in this table, the initial M stands for M1 or M2 depending on which DDR controller is not used. 2. If the DDR controller is not used, disable the internal DDR clock by setting the appropriate bit in the System Clock Control Register (SCCR) and put all DDR I/O in sleep mode by setting DR_x_GCR[DDR_x_DOZE] (for DDR controller x). See the <i>Clocks and General Configuration Registers</i> chapters in the MSC8156 Reference Manual for details. 3. For MSC8156 Revision 1 silicon, these pins were connected to GND. For newer revisions of the MSC8156, connecting these pins to GND increases device power consumption. 	

Table 48. Connectivity of TDM Related Pins When TDM Interface Is Not Used

Signal Name	Pin Connection
TDM _n TCLK	GND
TDM _n TxDAT	GND
TDM _n TSYN	GND
V _{DDIO}	2.5 V
Notes: <ol style="list-style-type: none"> 1. $x = \{0, 1, 2, 3\}$ 2. In case of subset of TDM interface usage please make sure to disable unused TDM modules. See <i>TDM</i> chapter in the <i>MSC8156 Reference Manual</i> for details. 	

3.5.5 Miscellaneous Pins

Table 49 lists the board connections for the pins not required by the system design. Table 49 assumes that the alternate function of the specified pin is not used. If the alternate function is used, connect that pin as required to support the selected function.

Table 49. Connectivity of Individual Pins When They Are Not Required

Signal Name	Pin Connection
CLKOUT	NC
EE0	GND
EE1	NC
GPIO[31–0]	NC
SCL	See the GPIO connectivity guidelines in this table.
SDA	See the GPIO connectivity guidelines in this table.
$\overline{\text{INT_OUT}}$	NC
$\overline{\text{IRQ}}[15–0]$	See the GPIO connectivity guidelines in this table.
$\overline{\text{NMI}}$	V _{DDIO}
$\overline{\text{NMI_OUT}}$	NC
RC[21–0]	GND
STOP_BS	GND
TCK	GND
TDI	GND
TDO	NC
TMR[4–0]	See the GPIO connectivity guidelines in this table.
TMS	GND
$\overline{\text{TRST}}$	See Section 3.1 for guidelines.
URXD	See the GPIO connectivity guidelines in this table.
UTXD	See the GPIO connectivity guidelines in this table.
DDN[1–0]	See the GPIO connectivity guidelines in this table.
DRQ[1–0]	See the GPIO connectivity guidelines in this table.
RCW_LSEL_0	GND
RCW_LSEL_1	GND
RCW_LSEL_2	GND
RCW_LSEL_3	GND
V _{DDIO}	2.5 V

Note: For details on configuration, see the *MSC8156 Reference Manual*. For additional information, refer to the *MSC815x* and *MSC825x DSP Family Design Checklist*.

3.6 Guide to Selecting Connections for Remote Power Supply Sensing

To assure consistency of input power levels, some applications use a practice of connecting the remote sense signal input of an on-board power supply to one of power supply pins of the IC device. The advantage of using this connection is the ability to compensate for the slow components of the IR drop caused by resistive supply current path from on-board power supply to the pins layer on the package. However, because of specific device requirements, not every ball connection can be selected as the remote sense pin. Some of these pins must be connected to the appropriate power supply or ground to ensure correct device functionality. Some connections supply critical power to a specific high usage area of the IC die; using such a connection as a non-supply pin could impact necessary supply current during high current events. The following balls can be used as the board supply remote sense output without degrading the power and ground supply quality:

- *VDD*: W10, T19
- *VSS*: J18, Y10
- *M3VDD*: None

Do not use any other connections for remote sensing. Use of any other connections for this purpose can result in application and device failure.

4 Ordering Information

Consult a Freescale Semiconductor sales office or authorized distributor to determine product availability and place an order.

Part	Package Type	Spheres	Core Voltage	Operating Temperature	Core Frequency (MHz)	Order Number
MSC8156	Flip Chip Plastic Ball Grid Array (FC-PBGA)	Lead-free	1.0 V	0° C to 105°C	1000	MSC8156SVT1000B
				-40° to 105°C	1000	MSC8156TVT1000B