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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	60MHz
Connectivity	CANbus, I²C, Microwire, SPI, SSI, SSP, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	46
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2194hbd64-151

Table 2. Pin description *…continued*

Symbol	Pin	Type	Description
P0[14]/DCD1/ EINT1	41	I	**DCD1 —** Data Carrier Detect input for UART1.
		I	**EINT1 —** External interrupt 1 input. **Note:** LOW on this pin while $\overline{\text{RESET}}$ is LOW forces on-chip bootloader to take control of the part after reset.
P0[15]/RI1/EINT2	45	I	**RI1 —** Ring Indicator input for UART1.
		I	**EINT2 —** External interrupt 2 input.
P0[16]/EINT0/ MAT0[2]/CAP0[2]	46	I	**EINT0 —** External interrupt 0 input.
		O	**MAT0[2] —** Match output for Timer 0, channel 2.
		I	**CAP0[2] —** Capture input for Timer 0, channel 2.
P0[17]/CAP1[2]/ SCK1/MAT1[2]	47	I	**CAP1[2] —** Capture input for Timer 1, channel 2.
		I/O	**SCK1 —** Serial Clock for SPI1/SSP[1]. SPI clock output from master or input to slave.
		O	**MAT1[2] —** Match output for Timer 1, channel 2.
P0[18]/CAP1[3]/ MISO1/MAT1[3]	53	I	**CAP1[3] —** Capture input for Timer 1, channel 3.
		I/O	**MISO1 —** Master In Slave Out for SPI1/SSP[1]. Data input to SPI master or data output from SPI slave.
		O	**MAT1[3] —** Match output for Timer 1, channel 3.
P0[19]/MAT1[2]/ MOSI1/CAP1[2]	54	O	**MAT1[2] —** Match output for Timer 1, channel 2.
		I/O	**MOSI1 —** Master Out Slave In for SPI1/SSP[1]. Data output from SPI master or data input to SPI slave.
		I	**CAP1[2] —** Capture input for Timer 1, channel 2.
P0[20]/MAT1[3]/ SSEL1/EINT3	55	O	**MAT1[3] —** Match output for Timer 1, channel 3.
		I	**SSEL1 —** Slave Select for SPI1/SSP[1]. Selects the SPI interface as a slave.
		I	**EINT3 —** External interrupt 3 input.
P0[21]/PWM5/ RD3/CAP1[3]	1	O	**PWM5 —** Pulse Width Modulator output 5.
		I	**RD3 —** CAN3 receiver input.
		I	**CAP1[3] —** Capture input for Timer 1, channel 3.
P0[22]/TD3/ CAP0[0]/MAT0[0]	2	O	**TD3 —** CAN3 transmitter output.
		I	**CAP0[0] —** Capture input for Timer 0, channel 0.
		O	**MAT0[0] —** Match output for Timer 0, channel 0.
P0[23]/RD2	3	I	CAN2 receiver input.
P0[24]/TD2	5	O	CAN2 transmitter output.
P0[25]/RD1	9	O	CAN1 receiver input.
P0[27]/AIN0/ CAP0[1]/MAT0[1]	11	I	**AIN0 —** A/D converter, input 0. This analog input is always connected to its pin.
		I	**CAP0[1] —** Capture input for Timer 0, channel 1.
		O	**MAT0[1] —** Match output for Timer 0, channel 1.
P0[28]/AIN1/ CAP0[2]/MAT0[2]	13	I	**AIN1 —** A/D converter, input 1. This analog input is always connected to its pin.
		I	**CAP0[2] —** Capture input for Timer 0, channel 2.
		O	**MAT0[2] —** Match output for Timer 0, channel 2.
P0[29]/AIN2/ CAP0[3]/MAT0[3]	14	I	**AIN2 —** A/D converter, input 2. This analog input is always connected to its pin.
		I	**CAP0[3] —** Capture input for Timer 0, Channel 3.
		O	**MAT0[3] —** Match output for Timer 0, channel 3.

Table 2. Pin description *…continued*

Symbol	Pin	Type	Description
P0[30]/AIN3/ EINT3/CAP0[0]	15	I	**AIN3 —** A/D converter, input 3. This analog input is always connected to its pin.
		I	**EINT3 —** External interrupt 3 input.
		I	**CAP0[0] —** Capture input for Timer 0, channel 0.
P1[0] to P1[31]		I/O	Port 1 is a 32-bit bidirectional I/O port with individual direction controls for each bit. The operation of port 1 pins depends upon the pin function selected via the Pin Connect Block. Pins 0 through 15 of port 1 are not available.
P1[16]/ TRACEPKT0	16	O	Trace Packet, bit 0. Standard I/O port with internal pull-up.
P1[17]/ TRACEPKT1	12	O	Trace Packet, bit 1. Standard I/O port with internal pull-up.
P1[18]/ TRACEPKT2	8	O	Trace Packet, bit 2. Standard I/O port with internal pull-up.
P1[19]/ TRACEPKT3	4	O	Trace Packet, bit 3. Standard I/O port with internal pull-up.
P1[20]/ TRACESYNC	48	O	Trace Synchronization. Standard I/O port with internal pull-up. **Note:** LOW on this pin while $\overline{\text{RESET}}$ is LOW, enables pins P1[25:16] to operate as Trace port after reset.
P1[21]/ PIPESTAT0	44	O	Pipeline Status, bit 0. Standard I/O port with internal pull-up.
P1[22]/ PIPESTAT1	40	O	Pipeline Status, bit 1. Standard I/O port with internal pull-up.
P1[23]/ PIPESTAT2	36	O	Pipeline Status, bit 2. Standard I/O port with internal pull-up.
P1[24]/ TRACECLK	32	O	Trace Clock. Standard I/O port with internal pull-up.
P1[25]/EXTIN0	28	I	External Trigger Input. Standard I/O with internal pull-up.
P1[26]/RTCK	24	I/O	Returned Test Clock output. Extra signal added to the JTAG port. Assists debugger synchronization when processor frequency varies. Bidirectional pin with internal pull-up. **Note:** LOW on this pin while $\overline{\text{RESET}}$ is LOW, enables pins P1[31:26] to operate as Debug port after reset.
P1[27]/TDO	64	O	Test Data out for JTAG interface.
P1[28]/TDI	60	I	Test Data in for JTAG interface.
P1[29]/TCK	56	I	Test Clock for JTAG interface. This clock must be slower than $\frac{1}{6}$ of the CPU clock (CCLK) for the JTAG interface to operate.
P1[30]/TMS	52	I	Test Mode Select for JTAG interface.
P1[31]/$\overline{\text{TRST}}$	20	I	Test Reset for JTAG interface.
TD1	10	O	CAN1 transmitter output.
$\overline{\text{RESET}}$	57	I	external reset input; a LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. TTL with hysteresis, 5 V tolerant.
XTAL1	62	I	input to the oscillator circuit and internal clock generator circuits.
XTAL2	61	O	output from the oscillator amplifier.
V_{SS}	6, 18, 25, 42, 50	I	ground: 0 V reference.

ISP flash erase command can be executed at any time (no matter whether the CRP is on or off). Removal of CRP is achieved by erasure of full on-chip user flash. With the CRP off, full access to the chip via the JTAG and/or ISP is restored.

6.3 On-chip SRAM

On-chip SRAM may be used for code and/or data storage. The SRAM may be accessed as 8 bit, 16 bit, and 32 bit. The LPC2194 provides 16 kB of SRAM.

6.4 Memory map

The LPC2194 memory maps incorporate several distinct regions, as shown in Figure 3.

In addition, the CPU interrupt vectors may be re-mapped to allow them to reside in either flash memory (the default) or on-chip SRAM. This is described in Section 6.18 “System control”.

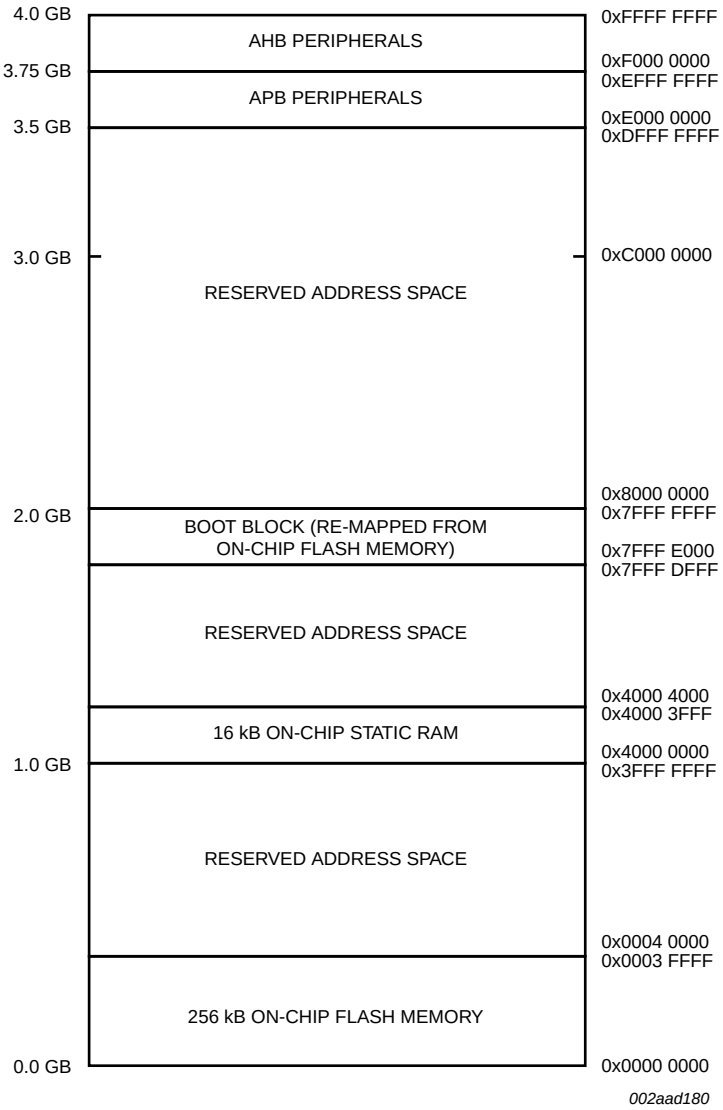


Fig 3. LPC2194 memory map

6.5 Interrupt controller

The Vectored Interrupt Controller (VIC) accepts all of the interrupt request inputs and categorizes them as Fast Interrupt Request (FIQ), vectored Interrupt Request (IRQ), and non-vectored IRQ as defined by programmable settings. The programmable assignment scheme means that priorities of interrupts from the various peripherals can be dynamically assigned and adjusted.

FIQ has the highest priority. If more than one request is assigned to FIQ, the VIC combines the requests to produce the FIQ signal to the ARM processor. The fastest possible FIQ latency is achieved when only one request is classified as FIQ, because then the FIQ service routine can simply start dealing with that device. But if more than one request is assigned to the FIQ class, the FIQ service routine can read a word from the VIC that identifies which FIQ source(s) is (are) requesting an interrupt.

- Ports are accessible via either the legacy group of registers (GPIOs) or the group of registers providing accelerated port access (Fast GPIOs).

6.8 10-bit ADC

The LPC2194 each contain a single 10-bit successive approximation ADC with four multiplexed channels.

6.8.1 Features

- Measurement range of 0 V to 3 V.
- Capable of performing more than 400000 10-bit samples per second.
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition on input pin or Timer Match signal.

6.8.2 ADC features available in LPC2194/01 only

- Every analog input has a dedicated result register to reduce interrupt overhead.
- Every analog input can generate an interrupt once the conversion is completed.
- The ADC pads are 5 V tolerant when configured for digital I/O function(s).

6.9 CAN controllers and acceptance filter

The LPC2194 contains four CAN controllers. The CAN is a serial communications protocol which efficiently supports distributed real-time control with a very high level of security. Its domain of application ranges from high-speed networks to low-cost multiplex wiring.

6.9.1 Features

- Data rates up to 1 Mbit/s on each bus.
- 32-bit register and RAM access.
- Compatible with CAN specification 2.0B, ISO 11898-1.
- Global Acceptance Filter recognizes 11-bit and 29-bit Rx identifiers for all CAN buses.
- Acceptance Filter can provide FullCAN-style automatic reception for selected Standard identifiers.

6.10 UARTs

The LPC2194 each contain two UARTs. In addition to standard transmit and receive data lines, the UART1 also provides a full modem control handshake interface.

6.10.1 Features

- 16 B Receive and Transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.

by 2, 4, 8, or 16 to produce the output clock. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip Reset and may be enabled by software. The program must configure and activate the PLL, wait for the PLL to Lock, then connect to the PLL as a clock source. The PLL settling time is 100 μs.

6.18.3 Reset and wake-up timer

Reset has two sources on the LPC2194: the $\overline{\text{RESET}}$ pin and Watchdog Reset. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin with an additional glitch filter. Assertion of chip Reset by any source starts the Wake-up Timer (see Wake-up Timer description below), causing the internal chip reset to remain asserted until the external Reset is de-asserted, the oscillator is running, a fixed number of clocks have passed, and the on-chip flash controller has completed its initialization.

When the internal Reset is removed, the processor begins executing at address 0, which is the Reset vector. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

The Wake-up Timer ensures that the oscillator and other analog functions required for chip operation are fully functional before the processor is allowed to execute instructions. This is important at power on, all types of Reset, and whenever any of the aforementioned functions are turned off for any reason. Since the oscillator and other functions are turned off during Power-down mode, any wake-up of the processor from Power-down mode makes use of the Wake-up Timer.

The Wake-up Timer monitors the crystal oscillator as the means of checking whether it is safe to begin code execution. When power is applied to the chip, or some event caused the chip to exit Power-down mode, some time is required for the oscillator to produce a signal of sufficient amplitude to drive the clock logic. The amount of time depends on many factors, including the rate of V_{DD} ramp (in the case of power on), the type of crystal and its electrical characteristics (if a quartz crystal is used), as well as any other external circuitry (e.g., capacitors), and the characteristics of the oscillator itself under the existing ambient conditions.

6.18.4 Code security (Code Read Protection - CRP)

This feature of the LPC2194/01 allows the user to enable different levels of security in the system so that access to the on-chip flash and use of the JTAG and ISP can be restricted. When needed, CRP is invoked by programming a specific pattern into a dedicated flash location. IAP commands are not affected by the CRP.

There are three levels of the Code Read Protection.

CRP1 disables access to chip via the JTAG and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors can not be erased.

CRP2 disables access to chip via the JTAG and only allows full flash erase and update using a reduced set of the ISP commands.

Running an application with level CRP3 selected fully disables any access to chip via the JTAG pins and the ISP. This mode effectively disables ISP override using P0[14] pin, too. It is up to the user's application to provide (if needed) flash update mechanism using IAP calls or call reinvoke ISP command to enable flash update via UART0.

when an application does not require any peripherals to run at the full processor rate. Because the APB divider is connected to the PLL output, the PLL remains active (if it was running) during Idle mode.

6.19 Emulation and debugging

The LPC2194 support emulation and debugging via a JTAG serial port. A trace port allows tracing program execution. Debugging and trace functions are multiplexed only with GPIOs on Port 1. This means that all communication, timer and interface peripherals residing on Port 0 are available during the development and debugging phase as they are when the application is run in the embedded system itself.

6.19.1 EmbeddedICE

Standard ARM EmbeddedICE logic provides on-chip debug support. The debugging of the target system requires a host computer running the debugger software and an EmbeddedICE protocol convertor. EmbeddedICE protocol convertor converts the Remote Debug Protocol commands to the JTAG data needed to access the ARM core.

The ARM core has a Debug Communication Channel function built-in. The debug communication channel allows a program running on the target to communicate with the host debugger or another separate host without stopping the program flow or even entering the debug state. The debug communication channel is accessed as a co-processor 14 by the program running on the ARM7TDMI-S core. The debug communication channel allows the JTAG port to be used for sending and receiving data without affecting the normal program flow. The debug communication channel data and control registers are mapped in to addresses in the EmbeddedICE logic.

The JTAG clock (TCK) must be slower than $\frac{1}{6}$ of the CPU clock (CCLK) for the JTAG interface to operate.

6.19.2 Embedded trace macrocell

Since the LPC2194 have significant amounts of on-chip memory, it is not possible to determine how the processor core is operating simply by observing the external pins. The Embedded Trace Macrocell (ETM) provides real-time trace capability for deeply embedded processor cores. It outputs information about processor execution to the trace port.

The ETM is connected directly to the ARM core and not to the main AMBA system bus. It compresses the trace information and exports it through a narrow trace port. An external trace port analyzer must capture the trace information under software debugger control. Instruction trace (or PC trace) shows the flow of execution of the processor and provides a list of all the instructions that were executed. Instruction trace is significantly compressed by only broadcasting branch addresses as well as a set of status signals that indicate the pipeline status on a cycle by cycle basis. Trace information generation can be controlled by selecting the trigger resource. Trigger resources include address comparators, counters and sequencers. Since trace information is compressed the software debugger requires a static image of the code being executed. Self-modifying code can not be traced because of this restriction.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DD(1V8)}$	supply voltage (1.8 V)		[2]	−0.5	+2.5	V
$V_{DD(3V3)}$	supply voltage (3.3 V)		[3]	−0.5	+3.6	V
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)			−0.5	+4.6	V
V_{IA}	analog input voltage			−0.5	+5.1	V
V_I	input voltage	5 V tolerant I/O pins	[4][5]	−0.5	+6.0	V
		other I/O pins	[4][6]	−0.5	$V_{DD(3V3)}$ + 0.5	V
I_{DD}	supply current		[7][8]	-	100	mA
I_{SS}	ground current		[8][9]	-	100	mA
T_j	junction temperature			-	150	°C
T_{stg}	storage temperature		[10]	−65	+150	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption		-	1.5	W
V_{ESD}	electrostatic discharge voltage	human body model	[11]			
		all pins		−2000	+2000	V

[1] The following applies to Table 4:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Internal rail.

[3] External rail.

[4] Including voltage on outputs in 3-state mode.

[5] Only valid when the $V_{DD(3V3)}$ supply voltage is present.

[6] Not to exceed 4.6 V.

[7] Per supply pin.

[8] The peak current is limited to 25 times the corresponding maximum current.

[9] Per ground pin.

[10] Dependent on package type.

[11] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

8. Static characteristics

Table 5. Static characteristics

T_{amb} = −40 °C to +125 °C for industrial applications, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$V_{DD(1V8)}$	supply voltage (1.8 V)		[2]	1.65	1.8	1.95	V
$V_{DD(3V3)}$	supply voltage (3.3 V)		[3]	3.0	3.3	3.6	V
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)			2.5	3.3	3.6	V
Standard port pins, $\overline{\text{RESET}}$, RTCK							
I_{IL}	LOW-level input current	V_I = 0 V; no pull-up		-	-	3	μA
I_{IH}	HIGH-level input current	$V_I = V_{DD(3V3)}$; no pull-down		-	-	3	μA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD(3V3)}$; no pull-up/down		-	-	3	μA
I_{latch}	I/O latch-up current	$-(0.5V_{DD(3V3)}) < V_I < (1.5V_{DD(3V3)})$; T_j < 125 °C		100	-	-	mA
V_I	input voltage		[4][5][6]	0	-	5.5	V
V_O	output voltage	output active		0	-	$V_{DD(3V3)}$	V
V_{IH}	HIGH-level input voltage			2.0	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.8	V
V_{hys}	hysteresis voltage			0.4	-	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = −4 mA	[7]	$V_{DD(3V3)} - 0.4$	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA	[7]	-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(3V3)} - 0.4$ V	[7]	−4	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	[7]	4	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V	[8]	-	-	−45	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DD(3V3)}$	[8]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V	[9]	10	50	150	μA
I_{pu}	pull-up current	V_I = 0 V	[10]	−15	−50	−85	μA
		$V_{DD(3V3)} < V_I$ < 5 V	[9]	0	0	0	μA

Table 5. Static characteristics *…continued*

T_{amb} = −40 °C to +125 °C for industrial applications, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
Oscillator pins						
$V_{i(XTAL1)}$	input voltage on pin XTAL1		0	-	1.8	V
$V_{o(XTAL2)}$	output voltage on pin XTAL2		0	-	1.8	V

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] Internal rail.

[3] External rail.

[4] Including voltage on outputs in 3-state mode.

[5] $V_{DD(3V3)}$ supply voltages must be present.

[6] 3-state outputs go into 3-state mode when $V_{DD(3V3)}$ is grounded.

[7] Accounts for 100 mV voltage drop in all supply lines.

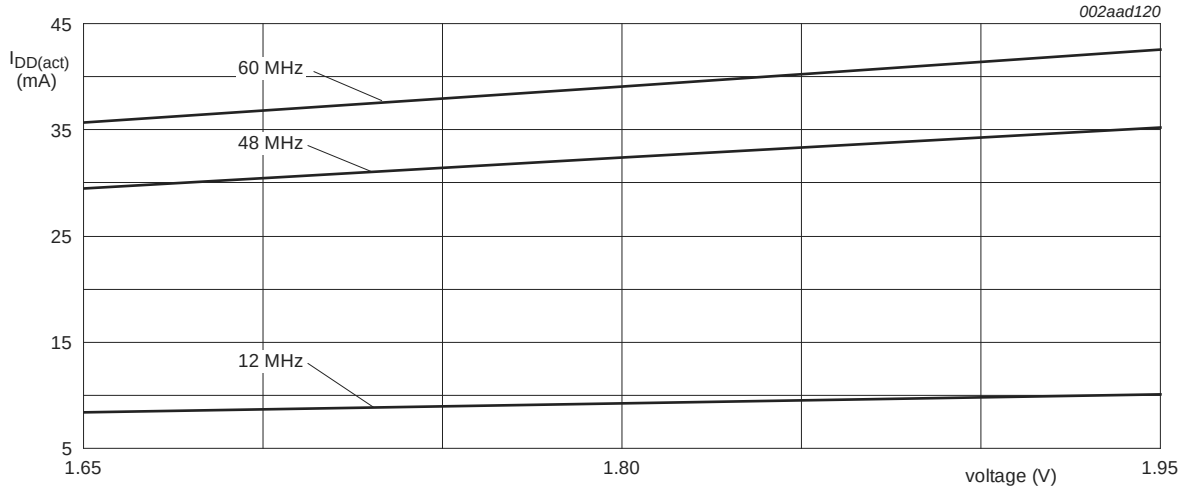
[8] Only allowed for a short time period.

[9] Minimum condition for V_I = 4.5 V, maximum condition for V_I = 5.5 V.

[10] Applies to P1[25:16].

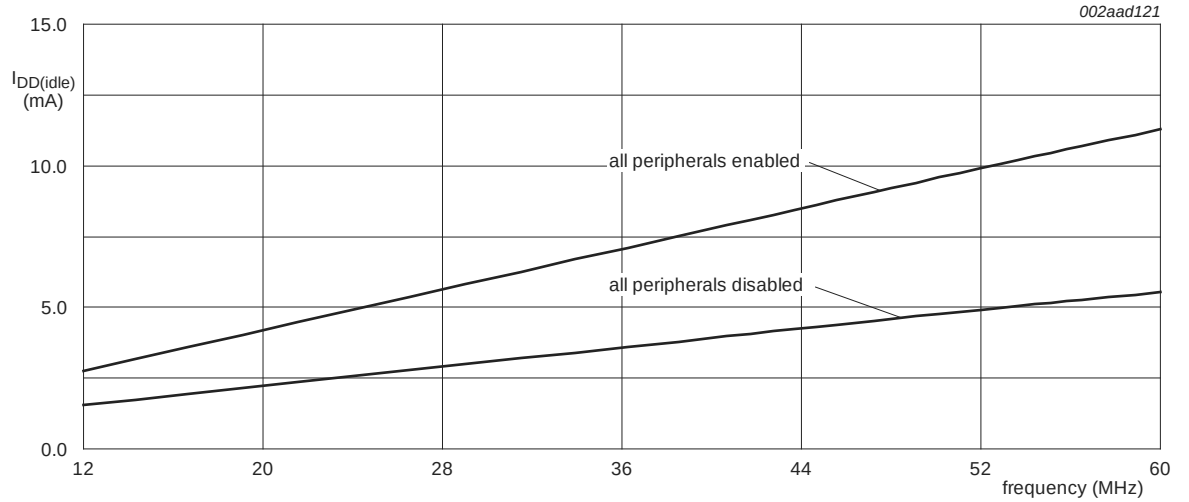
[11] See *LPC2119/2129/2194/2292/2294 User Manual*.

[12] To V_{SS}.



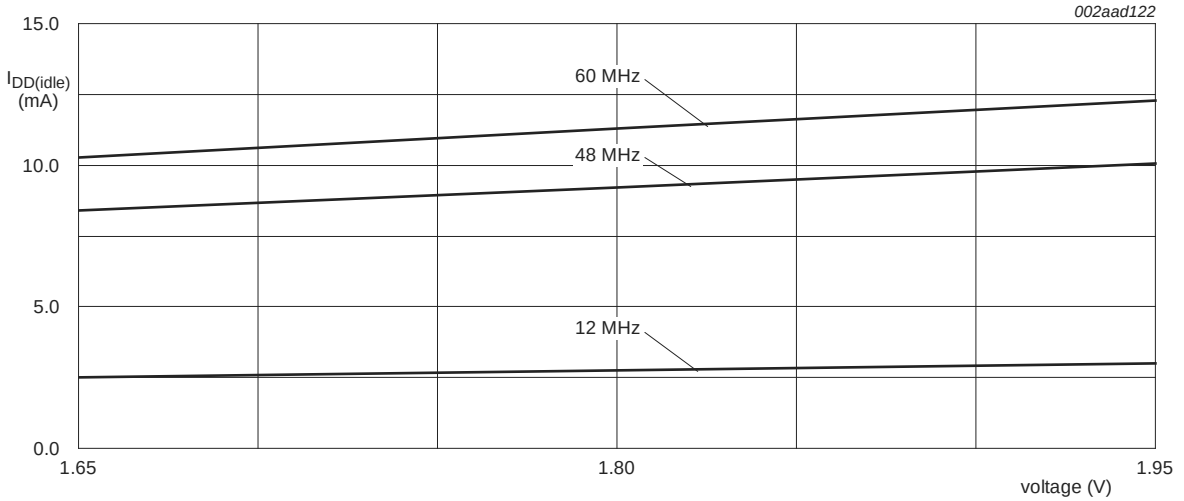
Test conditions: Active mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_{4}$;
Temp = 25 °C; core voltage 1.8 V; all peripherals disabled.

Fig 7. Typical LPC2194/01 $I_{DD(act)}$ measured at different voltages



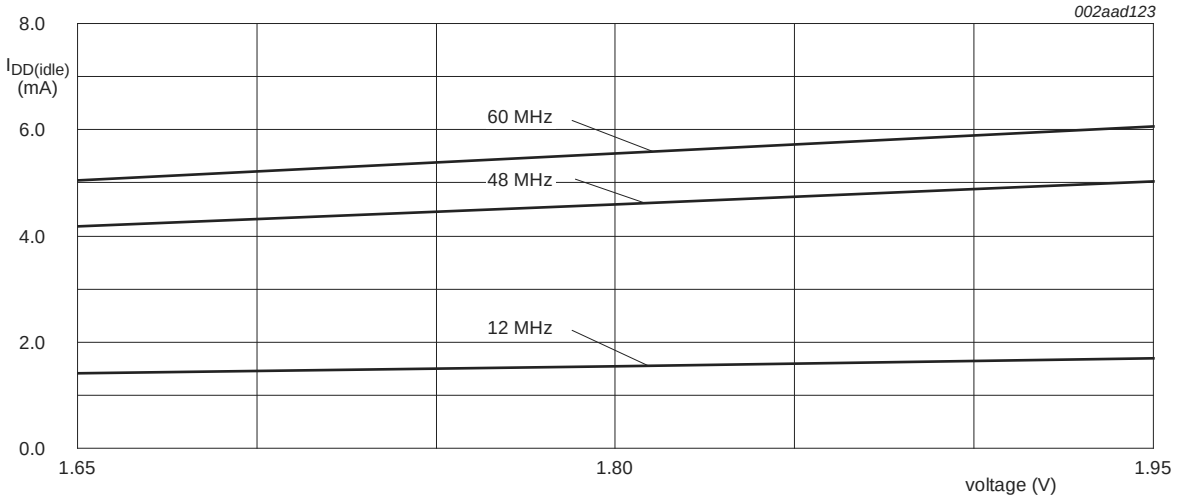
Test conditions: Idle mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_{4}$;
T_{amb} = 25 °C; core voltage 1.8 V.

Fig 8. Typical LPC2194/01 $I_{DD(idle)}$ measured at different frequencies



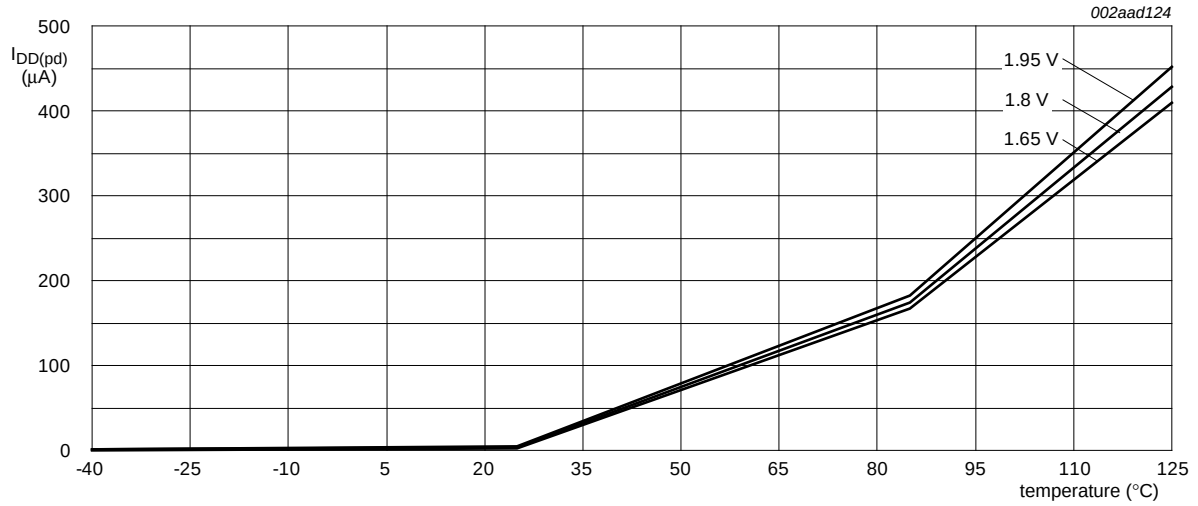
Test conditions: Idle mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_{4}$;
T_{amb} = 25 °C; core voltage 1.8 V; all peripherals enabled.

Fig 9. Typical LPC2194/01 $I_{DD(idle)}$ measured at different voltages



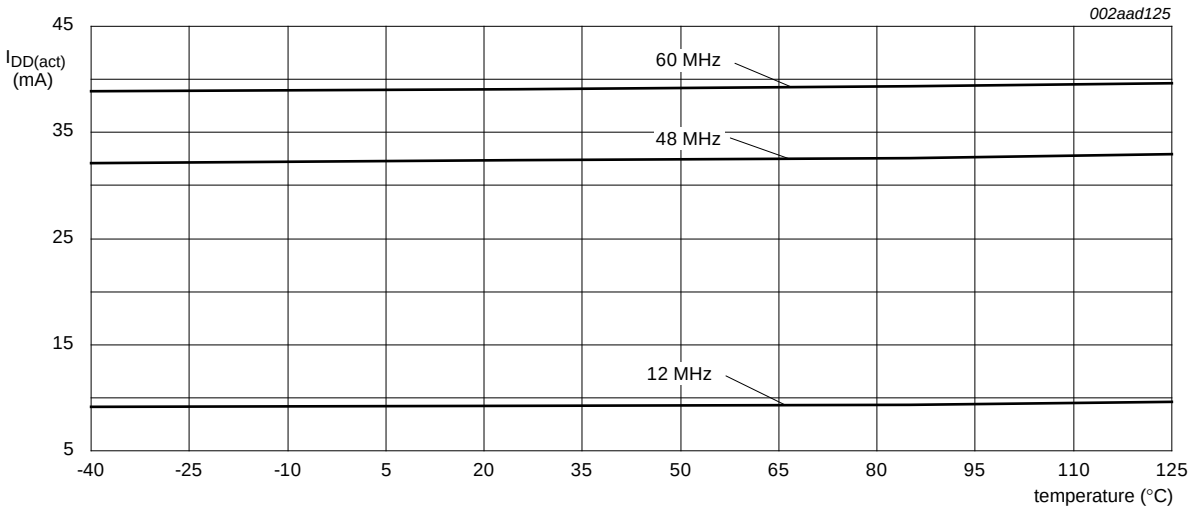
Test conditions: Idle mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_{4}$;
Temp = 25 °C; core voltage 1.8 V; all peripherals disabled.

Fig 10. Typical LPC2194/01 $I_{DD(idle)}$ measured at different voltages



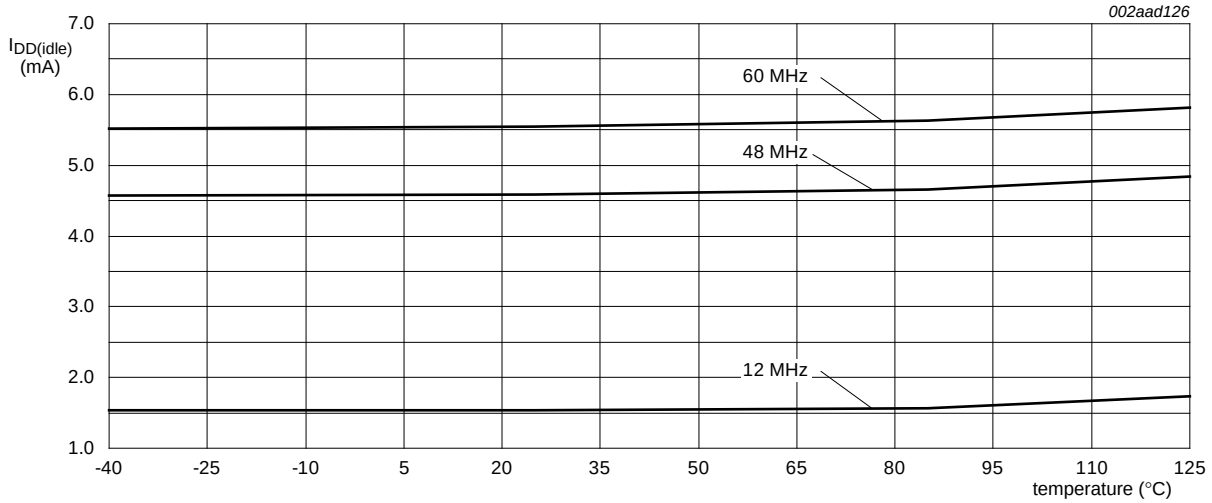
Test conditions: Power-down mode entered executing code from on-chip flash.

Fig 11. Typical LPC2194/01 core power-down current $I_{DD(pd)}$ measured at different temperatures



Test conditions: code executed from on-chip flash; PCLK = $^{CCLK}/_{4}$;
core voltage 1.8 V; all peripherals disabled.

Fig 12. Typical LPC2194/01 $I_{DD(act)}$ measured at different temperatures



Test conditions: Idle mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_{4}$; core voltage 1.8 V; all peripherals disabled.

Fig 13. Typical LPC2194/01 $I_{DD(idle)}$ measured at different temperatures

Table 7. Typical LPC2194/01 peripheral power consumption in active mode
Core voltage 1.8 V; T_{amb} = 25 °C; all measurements in µA; PCLK = $^{CCLK}/_{4}$.

Peripheral	CCLK = 12 MHz	CCLK = 48 MHz	CCLK = 60 MHz
Timer0	43	141	184
Timer1	46	150	180
UART0	98	320	398
UART1	103	351	421
PWM0	103	341	407
I^2C-bus	9	37	53
SPI0/1	6	27	29
RTC	16	55	78
ADC	33	128	167
CAN1/2/3/4	230	769	912

9. Dynamic characteristics

Table 8. Dynamic characteristics

T_{amb} = −40 °C to +125 °C for industrial applications; $V_{DD(1V8)}$, $V_{DD(3V3)}$ over specified ranges.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
External clock						
f_{osc}	oscillator frequency	supplied by an external oscillator (signal generator)	1	-	50	MHz
		external clock frequency supplied by an external crystal oscillator	1	-	30	MHz
		external clock frequency if on-chip PLL is used	10	-	25	MHz
		external clock frequency if on-chip bootloader is used for initial code download	10	-	25	MHz
$T_{cy(clk)}$	clock cycle time		20	-	1000	ns
t_{CHCX}	clock HIGH time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time		-	-	5	ns
t_{CHCL}	clock fall time		-	-	5	ns
Port pins (except P0[2] and P0[3])						
t_r	rise time		-	10	-	ns
t_f	fall time		-	10	-	ns
I^2C-bus pins (P0[2] and P0[3])						
t_f	fall time	V_{IH} to V_{IL}	[2] $20 + 0.1 \times C_b$	-	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Bus capacitance C_b in pF, from 10 pF to 400 pF.

9.1 Timing

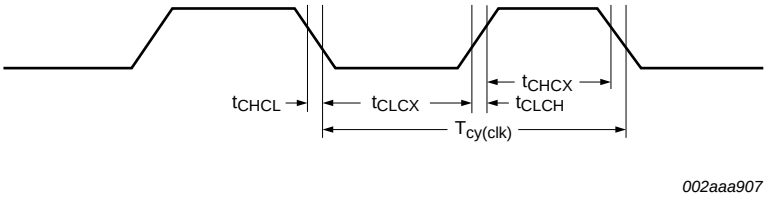
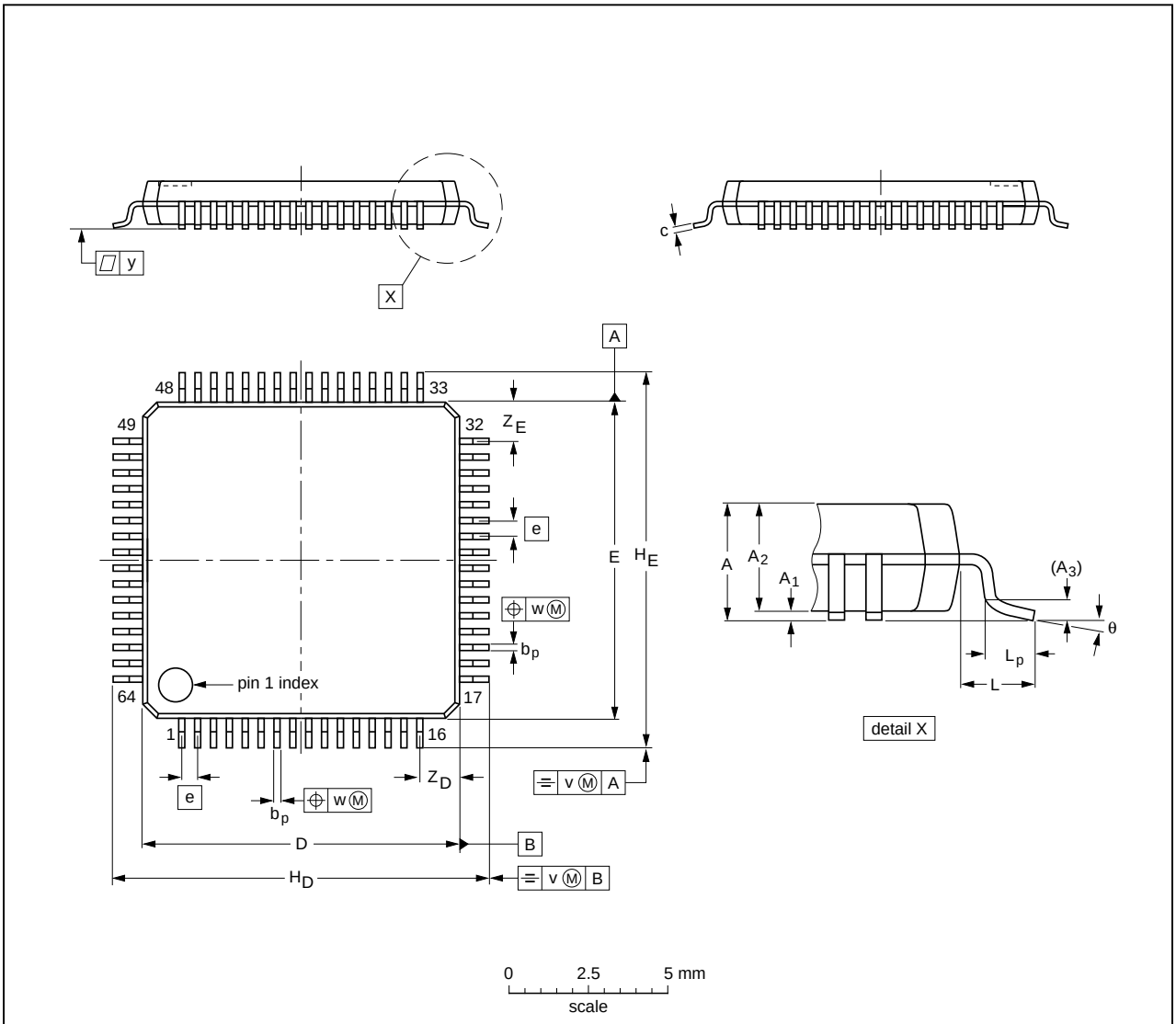


Fig 14. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

10. Package outline

LQFP64: plastic low profile quad flat package; 64 leads; body 10 x 10 x 1.4 mm **SOT314-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	10.1 9.9	10.1 9.9	0.5	12.15 11.85	12.15 11.85	1	0.75 0.45	0.2	0.12	0.1	1.45 1.05	1.45 1.05	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT314-2	136E10	MS-026				~~00-01-19~~ 03-02-25

Fig 15. Package outline SOT314-2 (LQFP64)

11. Abbreviations

Table 9. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
CAN	Controller Area Network
CPU	Central Processing Unit
DCC	Debug Communications Channel
FIFO	First In, First Out
GPIO	General Purpose Input/Output
I/O	Input/Output
JTAG	Joint Test Action Group
PLL	Phase-Locked Loop
PWM	Pulse Width Modulator
RAM	Random Access Memory
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
SSI	Synchronous Serial Interface
SSP	Synchronous Serial Port
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver/Transmitter

12. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC2194 v.6	20110614	Product data sheet	201004021F	LPC2194 v.5
Modifications:	• Table 5 “Static characteristics”; Changed /01 Power-down mode supply current ($I_{DD(pd)}$) from 180 μA to 500 μA for industrial temperature range, and 430 μA to 1000 μA for extended temperature range. • Table 5 “Static characteristics”; Moved V_{hys} voltage from typical to minimum. • Table 5 “Static characteristics”; Changed I^2C pad hysteresis from $0.5V_{DD(3V3)}$ to $0.05V_{DD(3V3)}$.			
LPC2194 v.5	20071210	Product data sheet	-	LPC2194 v.4
Modifications:	• Type number LPC2194HBD64/01 has been added. • Details introduced with /01 devices on new peripherals/features (Fast I/O Ports, SSP, CRP) and enhancements to existing ones (UART0/1, Timers, ADC, and SPI) added. • Power consumption measurements for LPC2194/01 added. • Description of JTAG pin TCK has been updated.			
LPC2194 v.4	20061016	Product data sheet	-	LPC2194 v.3
LPC2194 v.3	20060714	Product data sheet	-	LPC2194 v.2
LPC2194 v.2	20041222	Product data	-	LPC2194 v.1
LPC2194 v.1	20040206	Preliminary data	-	-

13. Legal information

13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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15. Contents

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