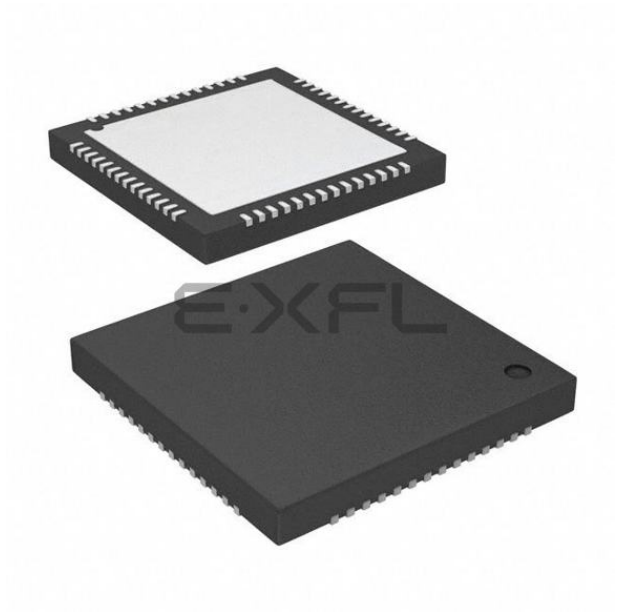
Infineon Technologies - CY8C4248LQI-BL563T Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, IrDA, LINbus, Microwire, SmartCard, SPI, SSP, UART/USART
Peripherals	Bluetooth, Brown-out Detect/Reset, DMA LCD, LVD, POR, PWM, SmartCard, SmartSense, WDT
Number of I/O	36
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x12b SAR; D/A 2xIDAC
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	56-UFQFN Exposed Pad
Supplier Device Package	56-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4248lqi-bl563t

More Information

Cypress provides a wealth of data at http://www.cypress.com to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the introduction page for Bluetooth® Low Energy (BLE) Products. Following is an abbreviated list for PSoC 4 BLE:

- Overview: PSoC Portfolio, PSoC Roadmap
- Product Selectors: PSoC 1, PSoC 3, PSoC 4, PSoC 4 BLE, PSoC 5LP. In addition, PSoC Creator includes a device selection tool.
- Application Notes: Cypress offers a large number of PSoC application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with PSoC 4 BLE are:
  - AN91267: Getting Started with PSoC 4 BLE
  - AN91184: PSoC 4 BLE - Designing BLE Applications
  - AN91162: Creating a BLE Custom Profile
  - AN97060: PSoC 4 BLE and PRoC BLE - Over-The-Air (OTA) Device Firmware Upgrade (DFU) Guide
  - AN91445: Antenna Design and RF Layout Guidelines
  - AN96841: Getting Started With EZ-BLE Module
  - AN85951: PSoC 4 CapSense Design Guide
  - AN95089: PSoC 4/PRoC BLE Crystal Oscillator Selection and Tuning Techniques
  - AN92584: Designing for Low Power and Estimating Battery Life for BLE Applications
- Technical Reference Manual (TRM) is in two documents:
  - Architecture TRM details each PSoC 4 BLE functional block.
  - Registers TRM describes each of the PSoC 4 registers.
- Development Kits:
  - CY8CKIT-042-BLE-A Pioneer Kit, is a flexible, Arduino-compatible, BLE development kit for PSoC 4 BLE.
  - CY8CKIT-142, PSoC 4 BLE Module, features a PSoC 4 BLE device, two crystals for the antenna matching network, a PCB antenna, and other passives, while providing access to all GPIOs of the device.
  - CY8CKIT-143, PSoC 4 BLE 256 KB Module, features a PSoC 4 BLE 256 KB device, two crystals for the antenna matching network, a PCB antenna, and other passives, while providing access to all GPIOs of the device.

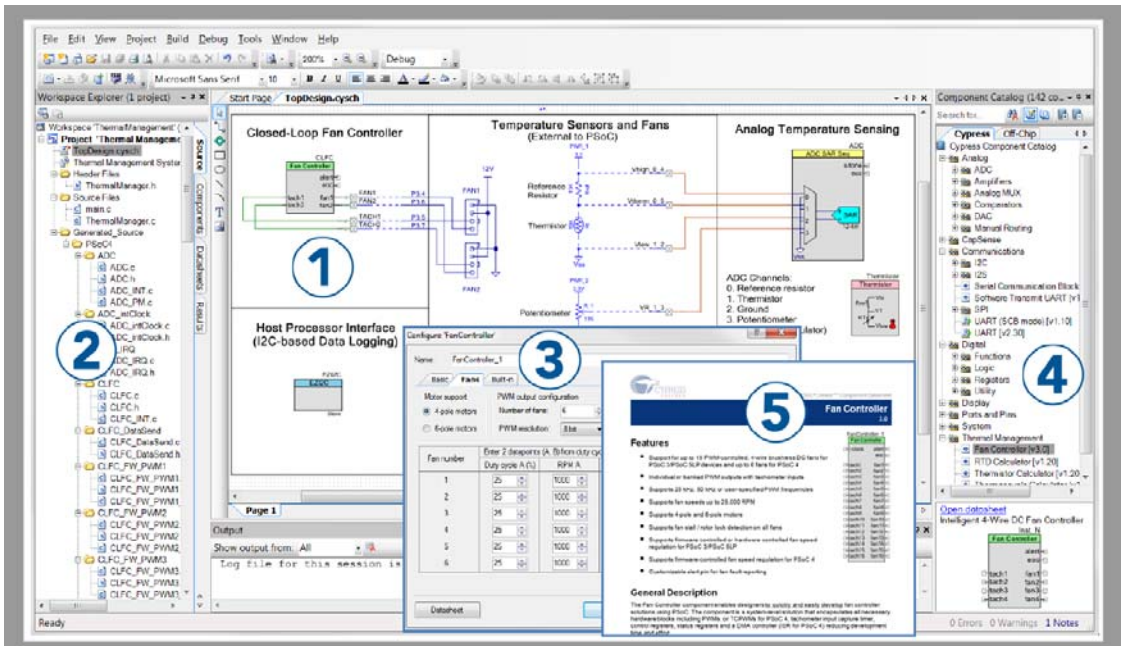
The MiniProg3 device provides an interface for flash programming and debug.

PSoC Creator

PSoC Creator is a free Windows-based Integrated Design Environment (IDE). It enables concurrent hardware and firmware design of PSoC 3, PSoC 4, and PSoC 5LP based systems. Create designs using classic, familiar schematic capture supported by over 100 pre-verified, production-ready PSoC Components; see the list of component datasheets. With PSoC Creator, you can:

1. Drag and drop component icons to build your hardware system design in the main design workspace
2. Codesign your application firmware with the PSoC hardware, using the PSoC Creator IDE C compiler
3. Configure components using the configuration tools
4. Explore the library of 100+ components
5. Review component datasheets

Figure 1. Multiple-Sensor Example Project in PSoC Creator



Contents

Analog Blocks

12-bit SAR ADC

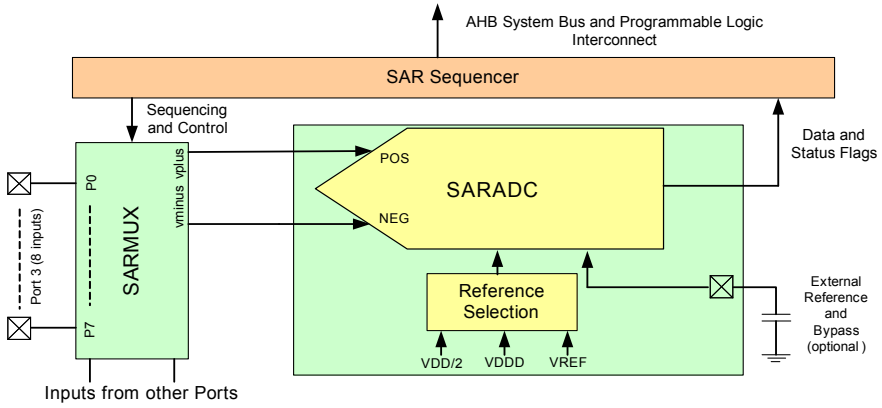
The 12-bit, 806 ksps SAR ADC can operate at a maximum clock rate of 14.508 MHz and requires a minimum of 18 clocks at that frequency to do a 12-bit conversion.

The block functionality is augmented for the user by adding a reference buffer to it (trimmable to ±1%) and by providing the choice of three internal voltage references, V_{DD}, $V_{DD}/2$, and V_{REF} (nominally 1.024 V), as well as an external reference through a REF pin. The sample-and-hold (S/H) aperture is programmable; it allows the gain bandwidth requirements of the amplifier driving the SAR inputs, which determine its settling time, to be relaxed if required. System performance will be 65 dB for true 12-bit precision if appropriate references are used and system noise levels permit it. To improve the performance in noisy conditions, it is possible to provide an external bypass (through a fixed pin location) for the internal reference amplifier.

The SAR is connected to a fixed set of pins through an 8-input sequencer. The sequencer cycles through the selected channels autonomously (sequencer scan) and does so with zero switching overhead (that is, the aggregate sampling bandwidth is equal to 806 ksps whether it is for a single channel or distributed over several channels). The sequencer switching is effected through a state machine or through firmware-driven switching. A feature provided by the sequencer is the buffering of each channel to reduce CPU interrupt-service requirements. To accommodate signals with varying source impedances and frequencies, it is possible to have different sample times programmable for each channel. Also, the signal range specification through a pair of range registers (low- and high-range values) is implemented with a corresponding out-of-range interrupt if the digitized value exceeds the programmed range; this allows fast detection of out-of-range values without having to wait for a sequencer scan to be completed and the CPU to read the values and check for out-of-range values in software.

The SAR is able to digitize the output of the on-chip temperature sensor for calibration and other temperature-dependent functions. The SAR is not available in Deep-Sleep and Hibernate modes as it requires a high-speed clock (up to 18 MHz). The SAR operating range is 1.71 V to 5.5 V.

Figure 4. SAR ADC System Diagram



Opamps (CTBm Block)

PSoC 4100_BLE has two opamps with comparator modes, which allow most common analog functions to be performed on-chip, eliminating external components. PGAs, voltage buffers, filters, transimpedance amplifiers, and other functions can be realized with external passives saving power, cost, and space. The on-chip opamps are designed with enough bandwidth to drive the sample-and-hold circuit of the ADC without requiring external buffering.

Temperature Sensor

PSoC 4100_BLE has an on-chip temperature sensor. This consists of a diode, which is biased by a current source that can be disabled to save power. The temperature sensor is connected to the ADC, which digitizes the reading and produces a temperature value by using a Cypress-supplied software that includes calibration and linearization.

Low-Power Comparators

PSoC 4100_BLE has a pair of low-power comparators, which can also operate in Deep-Sleep and Hibernate modes. This allows the analog system blocks to be disabled while retaining the ability to monitor external voltage levels during low-power modes. The comparator outputs are normally synchronized to avoid metastability unless operating in an asynchronous power mode (Hibernate) where the system wake-up circuit is activated by a comparator-switch event.

Table 2. PSoC 4100_BLE Pin List (WLCSP Package) *(continued)*

Pin	Name	Type	Pin Description
J2	P0.0	GPIO	Port 0 Pin 0, lcd, csd
J3	VDDR	POWER	1.9-V to 5.5-V radio supply
J6	VDDR	POWER	1.9-V to 5.5-V radio supply
J7	No Connect	-	-

High-speed I/O matrix (HSIOM) is a group of high-speed switches that routes GPIOs to the resources inside the device. These resources include CapSense, TCPWMs, I^2C, SPI, UART, and LCD. HSIOM_PORT_SELx are 32-bit-wide registers that control the routing of GPIOs. Each register controls one port; four dedicated bits are assigned to each GPIO in the port. This provides up to 16 different options for GPIO routing as shown in Table 3.

Table 3. HSIOM Port Settings

Value	Description
0	Firmware-controlled GPIO
1	Output is firmware-controlled, but Output Enable (OE) is controlled from DSI.
2	Both output and OE are controlled from DSI.
3	Output is controlled from DSI, but OE is firmware-controlled.
4	Pin is a CSD sense pin
5	Pin is a CSD shield pin
6	Pin is connected to AMUXA
7	Pin is connected to AMUXB
8	Pin-specific Active function #0
9	Pin-specific Active function #1
10	Pin-specific Active function #2
11	Reserved
12	Pin is an LCD common pin
13	Pin is an LCD segment pin
14	Pin-specific Deep-Sleep function #0
15	Pin-specific Deep-Sleep function #1

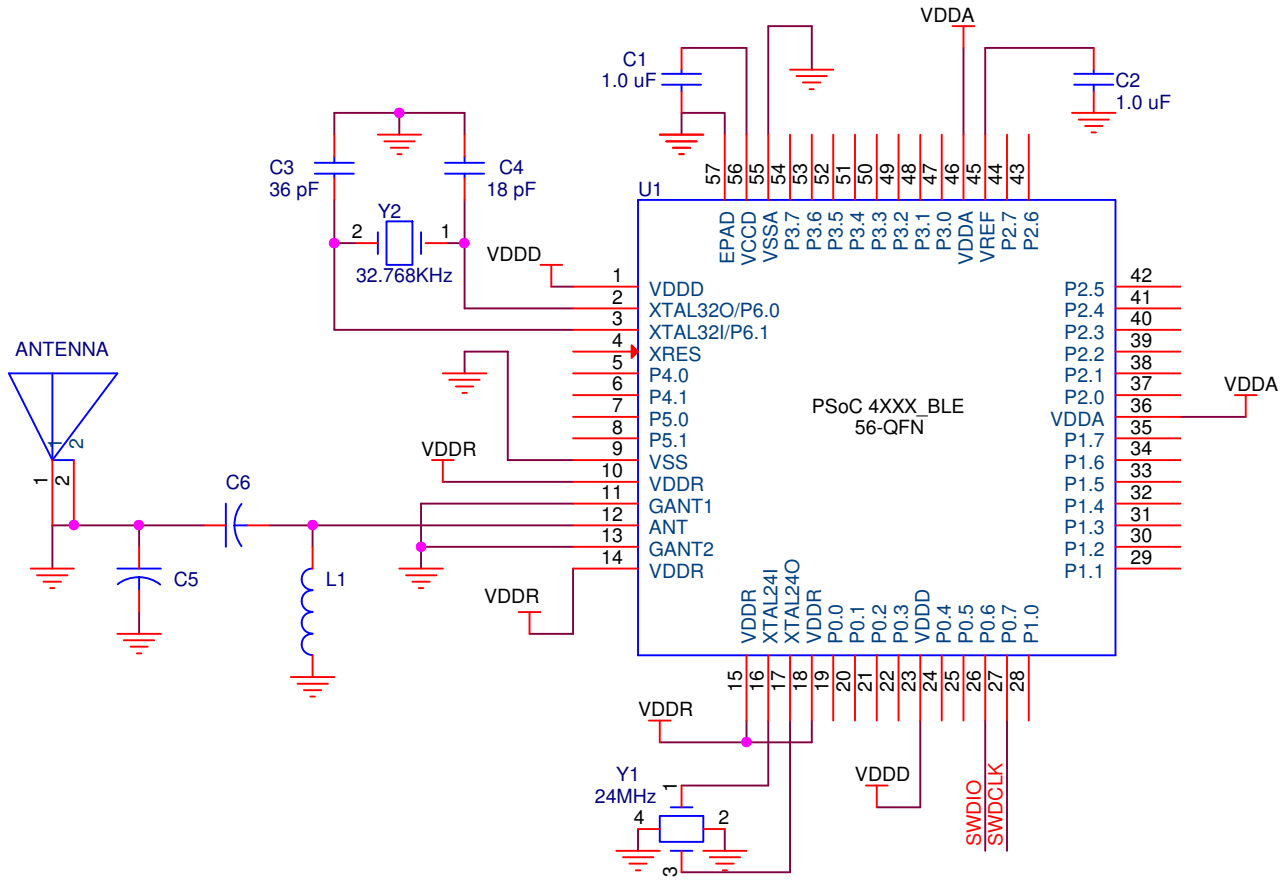
The selection of peripheral function for different GPIO pins is given in Table 4.

Table 4. Port Pin Connections

Name	Analog	Digital (HSIOM_PORT_SELx.SELy) ('x' denotes port number and 'y' denotes pin number)					
		0	8	9	10	14	15
		GPIO	Active #0	Active #1	Active #2	Deep-Sleep #0	Deep-Sleep #1
P0.0	COMP0_INP	GPIO	TCPWM0_P[3]	SCB1_UART_RX[1]		SCB1_I2C_SDA[1]	SCB1_SPI_MOSI[1]
P0.1	COMP0_INN	GPIO	TCPWM0_N[3]	SCB1_UART_TX[1]		SCB1_I2C_SCL[1]	SCB1_SPI_MISO[1]
P0.2		GPIO	TCPWM1_P[3]	SCB1_UART_RTS[1]		COMP0_OUT[0]	SCB1_SPI_SS0[1]
P0.3		GPIO	TCPWM1_N[3]	SCB1_UART_CTS[1]		COMP1_OUT[0]	SCB1_SPI_SCLK[1]
P0.4	COMP1_INP	GPIO	TCPWM1_P[0]	SCB0_UART_RX[1]	EXT_CLK[0]/ ECO_OUT[0]	SCB0_I2C_SDA[1]	SCB0_SPI_MOSI[1]
P0.5	COMP1_INN	GPIO	TCPWM1_N[0]	SCB0_UART_TX[1]		SCB0_I2C_SCL[1]	SCB0_SPI_MISO[1]
P0.6		GPIO	TCPWM2_P[0]	SCB0_UART_RTS[1]		SWDIO[0]	SCB0_SPI_SS0[1]
P0.7		GPIO	TCPWM2_N[0]	SCB0_UART_CTS[1]		SWDCLK[0]	SCB0_SPI_SCLK[1]
P1.0	CTBm1_OA0_INP	GPIO	TCPWM0_P[1]			COMP0_OUT[1]	WCO_OUT[2]
P1.1	CTBm1_OA0_INN	GPIO	TCPWM0_N[1]			COMP1_OUT[1]	SCB1_SPI_SS1
P1.2	CTBm1_OA0_OUT	GPIO	TCPWM1_P[1]				SCB1_SPI_SS2
P1.3	CTBm1_OA1_OUT	GPIO	TCPWM1_N[1]				SCB1_SPI_SS3

The possible pin connections are shown for all analog and digital peripherals (except the radio, LCD, and CSD blocks, which were shown in Table 1). A typical system application connection diagram is shown in Figure 5.

Figure 5. System Application Connection Diagram



Power

The PSoC 4100_BLE device can be supplied from batteries with a voltage range of 1.9 V to 5.5 V by directly connecting to the digital supply (VDDD), analog supply (VDDA), and radio supply (VDDR) pins. Internal LDOs in the device regulate the supply voltage to the required levels for different blocks. The device has one regulator for the digital circuitry and separate regulators for radio circuitry for noise isolation. Analog circuits run directly from the analog supply (VDDA) input. The device uses separate regulators for Deep-Sleep and Hibernate (lowered power supply and retention) modes to minimize the power consumption. The radio stops working below 1.9 V, but the device continues to function down to 1.71 V without RF. Note that VDDR must be supplied whenever VDDD is supplied.

Bypass capacitors must be used from VDDx (x = A, D, or R) to ground. The typical practice for systems in this frequency range is to use a capacitor in the 1-µF range in parallel with a smaller capacitor (for example, 0.1 µF). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

Power Supply	Bypass Capacitors
VDDD	0.1-µF ceramic at each pin plus bulk capacitor 1 µF to 10 µF.
VDDA	0.1-µF ceramic at each pin plus bulk capacitor 1 µF to 10 µF.
VDDR	0.1-µF ceramic at each pin plus bulk capacitor 1 µF to 10 µF.
VCCD	1-µF ceramic capacitor at the VCCD pin.
VREF (optional)	The internal bandgap may be bypassed with a 1-µF to 10-µF capacitor.

Development Support

The PSoC 4100_BLE family has a rich set of documentation, development tools, and online resources to assist you during your development process. Visit www.cypress.com/go/psoc4 to find out more.

Documentation

A suite of documentation supports the PSoC 4100_BLE family to ensure that you can find answers to your questions quickly. This section contains a list of some of the key documents.

Software User Guide: A step-by-step guide for using PSoC Creator. The software user guide shows you how the PSoC Creator build process works in detail, how to use source control with PSoC Creator, and much more.

Component Datasheets: The flexibility of PSoC allows the creation of new peripherals (Components) long after the device has gone into production. Component datasheets provide all of the information needed to select and use a particular Component, including a functional description, API documentation, example code, and AC/DC specifications.

Application Notes: PSoC application notes discuss a particular application of PSoC in depth; examples include creating standard and custom BLE profiles. Application notes often include example projects in addition to the application note document.

Technical Reference Manual: The Technical Reference Manual (TRM) contains all the technical detail you need to use a PSoC device, including a complete description of all PSoC registers. The TRM is available in the Documentation section at www.cypress.com/psoc4.

Online

In addition to print documentation, the Cypress PSoC forums connect you with fellow PSoC users and experts in PSoC from around the world, 24 hours a day, 7 days a week.

Tools

With industry standard cores, programming, and debugging interfaces, the PSoC 4100_BLE family is part of a development tool ecosystem. Visit us at www.cypress.com/go/psoccreator for the latest information on the revolutionary, easy to use PSoC Creator IDE, supported third party compilers, programmers, debuggers, and development kits.

Table 6. DC Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID19	I_{DD9}	Execute from flash; CPU at 24 MHz	–	7.1	–	mA	T = 25 °C, V_{DD} = 3.3 V
SID20	I_{DD10}	Execute from flash; CPU at 24 MHz	–	–	–	mA	T = –40 °C to 105 °C
SID21	I_{DD11}	Execute from flash; CPU at 48 MHz	–	13.4	–	mA	T = 25 °C, V_{DD} = 3.3 V
SID22	I_{DD12}	Execute from flash; CPU at 48 MHz	–	–	–	mA	T = –40 °C to 105 °C
Sleep Mode, V_{DD} = 1.8 V to 5.5 V							
SID23	I_{DD13}	IMO on	–	–	–	mA	T = 25 °C, VDD = 3.3 V, SYSCLK = 3 MHz
Sleep Mode, V_{DD} and V_{DDR} = 1.9 V to 5.5 V							
SID24	I_{DD14}	ECO on	–	–	–	mA	T = 25 °C, VDD = 3.3 V, SYSCLK = 3 MHz
Deep-Sleep Mode, V_{DD} = 1.8 V to 3.6 V							
SID25	I_{DD15}	WDT with WCO on	–	1.3	–	µA	T = 25 °C, V_{DD} = 3.3 V
SID26	I_{DD16}	WDT with WCO on	–	–	–	µA	T = –40 °C to 105 °C
Deep-Sleep Mode, V_{DD} = 3.6 V to 5.5 V							
SID27	I_{DD17}	WDT with WCO on	–	–	–	µA	T = 25 °C, V_{DD} = 5 V
SID28	I_{DD18}	WDT with WCO on	–	–	–	µA	T = –40 °C to 105 °C
Deep-Sleep Mode, V_{DD} = 1.71 V to 1.89 V (Regulator Bypassed)							
SID29	I_{DD19}	WDT with WCO on	–	–	–	µA	T = 25 °C
SID30	I_{DD20}	WDT with WCO on	–	–	–	µA	T = –40 °C to 105 °C
Deep-Sleep Mode, V_{DD} = 2.5 V to 3.6 V							
SID31	I_{DD21}	Opamp on	–	–	–	µA	T = 25 °C, V_{DD} = 3.3 V
SID32	I_{DD22}	Opamp on	–	–	–	µA	T = –40 °C to 105 °C
Deep-Sleep Mode, V_{DD} = 3.6 V to 5.5 V							
SID33	I_{DD23}	Opamp on	–	–	–	µA	T = 25 °C, V_{DD} = 5 V
SID34	I_{DD24}	Opamp on	–	–	–	µA	T = –40 °C to 105 °C
Hibernate Mode, V_{DD} = 1.8 V to 3.6 V							
SID37	I_{DD27}	GPIO and reset active	–	150	–	nA	T = 25 °C, V_{DD} = 3.3 V
SID38	I_{DD28}	GPIO and reset active	–	–	–	nA	T = –40 °C to 105 °C
Hibernate Mode, V_{DD} = 3.6 V to 5.5 V							
SID39	I_{DD29}	GPIO and reset active	–	–	–	nA	T = 25 °C, V_{DD} = 5 V
SID40	I_{DD30}	GPIO and reset active	–	–	–	nA	T = –40 °C to 105 °C
Hibernate Mode, V_{DD} = 1.71 V to 1.89 V (Regulator Bypassed)							
SID41	I_{DD31}	GPIO and reset active	–	–	–	nA	T = 25 °C
SID42	I_{DD32}	GPIO and reset active	–	–	–	nA	T = –40 °C to 105 °C

XRES

Table 12. XRES DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID87	V_{IH}	Input voltage HIGH threshold	0.7 × V_{DDD}	–	–	V	CMOS input
SID88	V_{IL}	Input voltage LOW threshold	–	–	0.3 × V_{DDD}	V	CMOS input
SID89	Rpullup	Pull-up resistor	3.5	5.6	8.5	kΩ	
SID90	C_{IN}	Input capacitance	–	3	–	pF	
SID91	$V_{HYSXRES}$	Input voltage hysteresis	–	100	–	mV	
SID92	I_{DIODE}	Current through protection diode to V_{DDD}/V_{SS}	–	–	100	µA	

Table 13. XRES AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID93	$T_{RESETWIDTH}$	Reset pulse width	1	–	–	µs	

Analog Peripherals

Opamp

Table 14. Opamp Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
I_{DD} (Opamp Block Current. V_{DD} = 1.8 V. No Load)							
SID94	I_{DD_HI}	Power = high	–	1000	1300	µA	
SID95	I_{DD_MED}	Power = medium	–	500	–	µA	
SID96	I_{DD_LOW}	Power = low	–	250	350	µA	
GBW (Load = 20 pF, 0.1 mA. V_{DDA} = 2.7 V)							
SID97	GBW_HI	Power = high	6	–	–	MHz	
SID98	GBW_MED	Power = medium	4	–	–	MHz	
SID99	GBW_LO	Power = low	–	1	–	MHz	
I_{OUT_MAX} (V_{DDA} ≥ 2.7 V, 500 mV from Rail)							
SID100	$I_{OUT\_MAX\_HI}$	Power = high	10	–	–	mA	
SID101	$I_{OUT\_MAX\_MID}$	Power = medium	10	–	–	mA	
SID102	$I_{OUT\_MAX\_LO}$	Power = low	–	5	–	mA	
I_{OUT} (V_{DDA} = 1.71 V, 500 mV from Rail)							
SID103	$I_{OUT\_MAX\_HI}$	Power = high	4	–	–	mA	
SID104	$I_{OUT\_MAX\_MID}$	Power = medium	4	–	–	mA	
SID105	$I_{OUT\_MAX\_LO}$	Power = low	–	2	–	mA	
SID106	V_{IN}	Charge pump on, V_{DDA} ≥ 2.7 V	–0.05	–	V_{DDA} – 0.2	V	
SID107	V_{CM}	Charge pump on, V_{DDA} ≥ 2.7 V	–0.05	–	V_{DDA} – 0.2	V	
V_{OUT} (V_{DDA} ≥ 2.7 V)							
SID108	V_{OUT_1}	Power = high, I_{LOAD}=10 mA	0.5	–	V_{DDA} – 0.5	V	
SID109	V_{OUT_2}	Power = high, I_{LOAD}=1 mA	0.2	–	V_{DDA} – 0.2	V	
SID110	V_{OUT_3}	Power = medium, I_{LOAD}=1 mA	0.2	–	V_{DDA} – 0.2	V	
SID111	V_{OUT_4}	Power = low, I_{LOAD}=0.1 mA	0.2	–	V_{DDA} – 0.2	V	
SID112	V_{OS_TR}	Offset voltage, trimmed	1	±0.5	1	mV	High mode

Table 15. Comparator DC Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID143	V_{ICM1}	Input common mode voltage in normal mode	0	–	V_{DDD} –0.1	V	Modes 1 and 2
SID144	V_{ICM2}	Input common mode voltage in low-power mode	0	–	V_{DDD}	V	
SID145	V_{ICM3}	Input common mode voltage in ultra low-power mode	0	–	V_{DDD} –1.15	V	V_{DDD} ≥ 2.6 V for Temp < 0 °C V_{DDD} ≥ 1.8 V for Temp ≥ 0 °C
SID146	CMRR	Common mode rejection ratio	50	–	–	dB	V_{DDD} ≥ 2.7 V
SID147	CMRR	Common mode rejection ratio	42	–	–	dB	V_{DDD} ≤ 2.7 V
SID148	I_{CMP1}	Block current, normal mode	–	–	400	µA	
SID149	I_{CMP2}	Block current, low-power mode	–	–	100	µA	
SID150	I_{CMP3}	Block current in ultra-low-power mode	–	6	–	µA	V_{DDD} ≥ 2.6 V for Temp < 0 °C V_{DDD} ≥ 1.8 V for Temp ≥ 0 °C
SID151	Z_{CMP}	DC input impedance of comparator	35	–	–	MΩ	

Table 16. Comparator AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID152	T_{RESP1}	Response time, normal mode, 50-mV overdrive	–	38	–	ns	50-mV overdrive
SID153	T_{RESP2}	Response time, low-power mode, 50-mV overdrive	–	70	–	ns	50-mV overdrive
SID154	T_{RESP3}	Response time, ultra-low-power mode, 50-mV overdrive	–	2.3	–	µs	200-mV overdrive V_{DDD} ≥ 2.6 V for Temp < 0 °C V_{DDD} ≥ 1.8 V for Temp ≥ 0 °C

Temperature Sensor

Table 17. Temperature Sensor Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID155	$T_{SENSACC}$	Temperature-sensor accuracy	–5	±1	5	°C	–40 to +85 °C

Counter

Table 23. Counter DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID200	I_{CTR1}	Block current consumption at 3 MHz	–	–	42	µA	16-bit timer, 85 °C
SID200A			–	–	46	µA	16-bit timer, 105 °C
SID201	I_{CTR2}	Block current consumption at 12 MHz	–	–	130	µA	16-bit timer, 85 °C
SID201A			–	–	137	µA	16-bit timer, 105 °C
SID202	I_{CTR3}	Block current consumption at 48 MHz	–	–	535	µA	16-bit timer, 85 °C
SID202A			–	–	560	µA	16-bit timer, 105 °C

Table 24. Counter AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID203	$T_{CTRFREQ}$	Operating frequency	F_{CLK}	–	48	MHz	
SID204	$T_{CTRPWINT}$	Capture pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	
SID205	$T_{CTRPWEXT}$	Capture pulse width (external)	$2 \times T_{CLK}$	–	–	ns	
SID206	T_{CTRES}	Counter Resolution	T_{CLK}	–	–	ns	
SID207	$T_{CENWIDINT}$	Enable pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	
SID208	$T_{CENWIDEXT}$	Enable pulse width (external)	$2 \times T_{CLK}$	–	–	ns	
SID209	$T_{CTRRESWINT}$	Reset pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	
SID210	$T_{CTRRESWEXT}$	Reset pulse width (external)	$2 \times T_{CLK}$	–	–	ns	

Pulse Width Modulation (PWM)

Table 25. PWM DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID211	I_{PWM1}	Block current consumption at 3 MHz	–	–	42	µA	16-bit timer, 85 °C
SID211A			–	–	46	µA	16-bit timer, 105 °C
SID212	I_{PWM2}	Block current consumption at 12 MHz	–	–	130	µA	16-bit timer, 85 °C
SID212A			–	–	137	µA	16-bit timer, 105 °C
SID213	I_{PWM3}	Block current consumption at 48 MHz	–	–	535	µA	16-bit timer, 85 °C
SID213A			–	–	560	µA	16-bit timer, 105 °C

Table 26. PWM AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID214	$T_{PWMFREQ}$	Operating frequency	F_{CLK}	–	48	MHz	
SID215	$T_{PWMPWINT}$	Pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	
SID216	T_{PWMEXT}	Pulse width (external)	$2 \times T_{CLK}$	–	–	ns	
SID217	$T_{PWMKILLINT}$	Kill pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	
SID218	$T_{PWMKILLEXT}$	Kill pulse width (external)	$2 \times T_{CLK}$	–	–	ns	
SID219	$T_{PWMEINT}$	Enable pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	
SID220	$T_{PWMENEXT}$	Enable pulse width (external)	$2 \times T_{CLK}$	–	–	ns	
SID221	$T_{PWMRESWINT}$	Reset pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	
SID222	$T_{PWMRESWEXT}$	Reset pulse width (external)	$2 \times T_{CLK}$	–	–	ns	

SPI Specifications

Table 33. Fixed SPI DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID237	I_{SPI1}	Block current consumption at 1 Mbps	–	–	360	µA	
SID238	I_{SPI2}	Block current consumption at 4 Mbps	–	–	560	µA	
SID239	I_{SPI3}	Block current consumption at 8 Mbps	–	–	600	µA	

Table 34. Fixed SPI AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID240	F_{SPI}	SPI operating frequency (master; 6x oversampling)	–	–	8	MHz	

Table 35. Fixed SPI Master Mode AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID241	T_{DMO}	MOSI valid after Sclock driving edge	–	–	18	ns	
SID242	T_{DSI}	MISO valid before Sclock capturing edge. Full clock, late MISO sampling used	20	–	–	ns	Full clock, late MISO sampling
SID243	T_{HMO}	Previous MOSI data hold time	0	–	–	ns	Referred to Slave capturing edge

Table 36. Fixed SPI Slave Mode AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID244	T_{DMI}	MOSI valid before Sclock capturing edge	40	–	–	ns	
SID245	T_{DSO}	MISO valid after Sclock driving edge	–	–	42 + 3 × T_{SCB}	ns	
SID246	T_{DSO_ext}	MISO valid after Sclock driving edge in external clock mode	–	–	50	ns	V_{DD} < 3.0 V
SID247	T_{HSO}	Previous MISO data hold time	0	–	–	ns	
SID248	$T_{SSELSCK}$	SSEL valid to first SCK valid edge	100	–	–	ns	

Table 41. Brown-Out Detect

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID261	$V_{FALLPPOR}$	BOD trip voltage in Active and Sleep modes	1.64	–	–	V	
SID262	$V_{FALLDPSLP}$	BOD trip voltage in Deep-Sleep mode	1.4	–	–	V	

Table 42. Hibernate Reset

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID263	$V_{HBRTRIP}$	BOD trip voltage in Hibernate mode	1.1	–	–	V	

Voltage Monitors

Table 43. Voltage Monitor DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID265	V_{LVI1}	LVI_A/D_SEL[3:0] = 0000b	1.71	1.75	1.79	V	
SID266	V_{LVI2}	LVI_A/D_SEL[3:0] = 0001b	1.76	1.80	1.85	V	
SID267	V_{LVI3}	LVI_A/D_SEL[3:0] = 0010b	1.85	1.90	1.95	V	
SID268	V_{LVI4}	LVI_A/D_SEL[3:0] = 0011b	1.95	2.00	2.05	V	
SID269	V_{LVI5}	LVI_A/D_SEL[3:0] = 0100b	2.05	2.10	2.15	V	
SID270	V_{LVI6}	LVI_A/D_SEL[3:0] = 0101b	2.15	2.20	2.26	V	
SID271	V_{LVI7}	LVI_A/D_SEL[3:0] = 0110b	2.24	2.30	2.36	V	
SID272	V_{LVI8}	LVI_A/D_SEL[3:0] = 0111b	2.34	2.40	2.46	V	
SID273	V_{LVI9}	LVI_A/D_SEL[3:0] = 1000b	2.44	2.50	2.56	V	
SID274	V_{LVI10}	LVI_A/D_SEL[3:0] = 1001b	2.54	2.60	2.67	V	
SID275	V_{LVI11}	LVI_A/D_SEL[3:0] = 1010b	2.63	2.70	2.77	V	
SID276	V_{LVI12}	LVI_A/D_SEL[3:0] = 1011b	2.73	2.80	2.87	V	
SID277	V_{LVI13}	LVI_A/D_SEL[3:0] = 1100b	2.83	2.90	2.97	V	
SID278	V_{LVI14}	LVI_A/D_SEL[3:0] = 1101b	2.93	3.00	3.08	V	
SID279	V_{LVI15}	LVI_A/D_SEL[3:0] = 1110b	3.12	3.20	3.28	V	
SID280	V_{LVI16}	LVI_A/D_SEL[3:0] = 1111b	4.39	4.50	4.61	V	
SID281	LVI_IDD	Block current	–	–	100	µA	

Table 44. Voltage Monitor AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID282	$T_{MONTRIP}$	Voltage monitor trip time	–	–	1	µs	

Table 52. BLE Subsystem *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID365	FTX, ACC	Frequency accuracy	–150	–	150	kHz	RF-PHY Specification (TRM-LE/CA/06/C)
SID366	FTX, MAXDR	Maximum frequency drift	–50	–	50	kHz	RF-PHY Specification (TRM-LE/CA/06/C)
SID367	FTX, INITDR	Initial frequency drift	–20	–	20	kHz	RF-PHY Specification (TRM-LE/CA/06/C)
SID368	FTX, DR	Maximum drift rate	–20	–	20	kHz/ 50 µs	RF-PHY Specification (TRM-LE/CA/06/C)
SID369	IBSE1	In-band spurious emission at 2-MHz offset	–	–	–20	dBm	RF-PHY Specification (TRM-LE/CA/03/C)
SID370	IBSE2	In-band spurious emission at ≥3-MHz offset	–	–	-30	dBm	RF-PHY Specification (TRM-LE/CA/03/C)
SID371	TXSE1	Transmitter spurious emissions (average), <1.0 GHz	–	–	-55.5	dBm	FCC-15.247
SID372	TXSE2	Transmitter spurious emissions (average), >1.0 GHz	–	–	-41.5	dBm	FCC-15.247
RF Current Specifications							
SID373	IRX	Receive current in normal mode	–	18.7	–	mA	
SID373A	IRX_RF	Radio receive current in normal mode	–	16.4	–	mA	Measured at V_{DDR}
SID374	IRX, HIGHGAIN	Receive current in high-gain mode	–	21.5	–	mA	
SID375	ITX, 3dBm	TX current at 3-dBm setting (PA10)	–	20	–	mA	
SID376	ITX, 0dBm	TX current at 0-dBm setting (PA7)	–	16.5	–	mA	
SID376A	ITX_RF, 0dBm	Radio TX current at 0 dBm setting (PA7)	–	15.6	–	mA	Measured at V_{DDR}
SID376B	ITX_RF, 0dBm	Radio TX current at 0 dBm excluding Balun loss	–	14.2	–	mA	Guaranteed by design simulation
SID377	ITX,-3dBm	TX current at –3-dBm setting (PA4)	–	15.5	–	mA	
SID378	ITX,-6dBm	TX current at –6-dBm setting (PA3)	–	14.5	–	mA	
SID379	ITX,-12dBm	TX current at –12-dBm setting (PA2)	–	13.2	–	mA	
SID380	ITX,-18dBm	TX current at –18-dBm setting (PA1)	–	12.5	–	mA	
SID380A	Iavg_1sec, 0dBm	Average current at 1-second BLE connection interval	–	17.1	–	µA	TXP: 0 dBm; ±20-ppm master and slave clock accuracy.
SID380B	Iavg_4sec, 0dBm	Average current at 4-second BLE connection interval	–	6.1	–	µA	TXP: 0 dBm; ±20-ppm master and slave clock accuracy.
General RF Specifications							
SID381	FREQ	RF operating frequency	2400	–	2482	MHz	
SID382	CHBW	Channel spacing	–	2	–	MHz	
SID383	DR	On-air data rate	–	1000	–	kbps	
SID384	IDLE2TX	BLE.IDLE to BLE. TX transition time	–	120	140	µs	
SID385	IDLE2RX	BLE.IDLE to BLE. RX transition time	–	75	120	µs	

Ordering Information

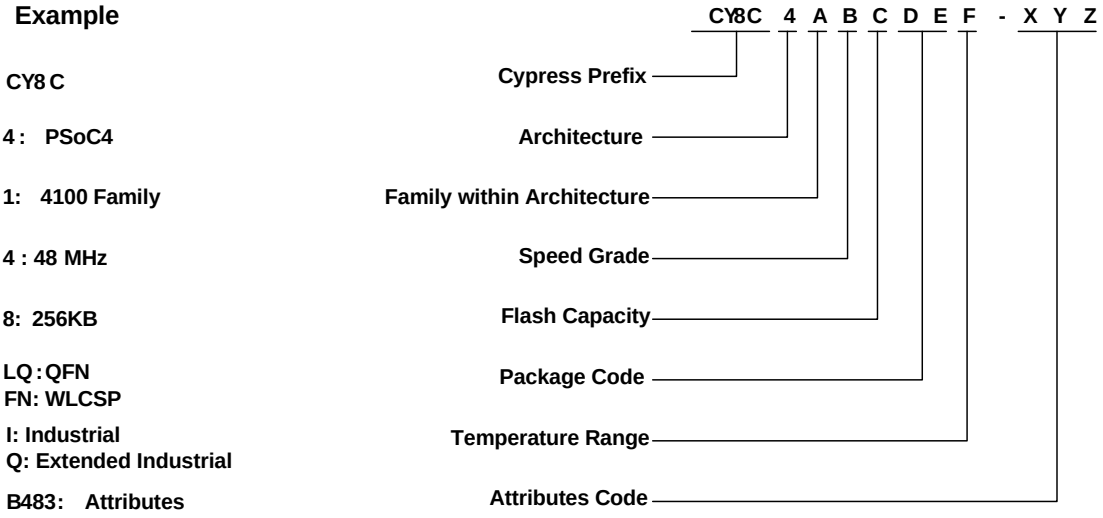
The PSoC 4100_BLE part numbers and features are listed in the following table.

Product Family	MPN	Max CPU Speed (MHz)	BLE subsystem	Flash (KB)	SRAM (KB)	UDB	Opamp	CapSense	TMG (Gestures)	Direct LCD Drive	12-bit SAR ADC	DMA	LP Comparators	TCPWM Blocks	SCB Blocks	GPIO	Package	Temperature Range
PSoC 4100_BL	CY8C4127LQI-BL473	24	4.1	128	16	–	2	–	–	–	806 ksps	–	2	4	2	36	QFN	85 °C
	CY8C4127LQI-BL453	24	4.1	128	16	–	2	1	–	–	806 ksps	–	2	4	2	36	QFN	85 °C
	CY8C4127LQI-BL483	24	4.1	128	16	–	2	1	–	1	806 ksps	–	2	4	2	36	QFN	85 °C
	CY8C4127FNI-BL483	24	4.1	128	16	–	2	1	–	1	806 ksps	–	2	4	2	36	68-CSP	85 °C
	CY8C4127LQI-BL493	24	4.1	128	16	–	2	1	1	1	806 ksps	–	2	4	2	36	QFN	85 °C
	CY8C4127FNI-BL493	24	4.1	128	16	–	2	1	1	1	806 ksps	–	2	4	2	36	68-CSP	85 °C
	CY8C4128LQI-BL473	24	4.1	256	32	–	2	–	–	–	806 ksps	–	2	4	2	36	QFN	85 °C
	CY8C4128LQI-BL483	24	4.1	256	32	–	2	1	–	1	806 ksps	–	2	4	2	36	QFN	85 °C
	CY8C4128LQI-BL543	24	4.2	256	32	–	2	–	–	–	806 ksps	1	–	4	2	36	QFN	85 °C
	CY8C4128FNI-BL543	24	4.2	256	32	–	2	–	–	–	806 ksps	1	–	4	2	36	76-CSP	85 °C
	CY8C4128LQI-BL573	24	4.2	256	32	–	2	–	–	–	806 ksps	1	2	4	2	36	QFN	85 °C
	CY8C4128FNI-BL573	24	4.2	256	32	–	2	–	–	–	806 ksps	1	2	4	2	36	76-CSP	85 °C
	CY8C4128LQI-BL553	24	4.2	256	32	–	2	1	–	–	806 ksps	1	2	4	2	36	QFN	85 °C
	CY8C4128FNI-BL553	24	4.2	256	32	–	2	1	–	–	806 ksps	1	2	4	2	36	76-CSP	85 °C
	CY8C4128LQI-BL563	24	4.2	256	32	–	2	–	–	1	806 ksps	1	2	4	2	36	QFN	85 °C
	CY8C4128FNI-BL563	24	4.2	256	32	–	2	–	–	1	806 ksps	1	2	4	2	36	76-CSP	85 °C
	CY8C4128LQI-BL583	24	4.2	256	32	–	2	1	–	1	806 ksps	1	2	4	2	36	QFN	85 °C
	CY8C4128FNI-BL583	24	4.2	256	32	–	2	1	–	1	806 ksps	1	2	4	2	36	76-CSP	85 °C
	CY8C4128LQI-BL593	24	4.2	256	32	–	2	1	1	1	806 ksps	1	2	4	2	36	QFN	85 °C
	CY8C4128FNI-BL593	24	4.2	256	32	–	2	1	1	1	806 ksps	1	2	4	2	36	76-CSP	85 °C

Part Numbering Conventions

PSoC 4 devices follow the part numbering convention described in the following table. All fields are single-character alphanumeric (0, 1, 2, …, 9, A,B, …, Z) unless stated otherwise.

The part numbers are of the form CY8C4ABCDEF-XYZ where the fields are defined as follows.



The Field Values are listed in the following table.

Field	Description	Values	Meaning
CY8C	Cypress Prefix		
4	Architecture	4	PSoC 4
A	Family within architecture	1	4100-BLE Family
B	CPU Speed	2	24 MHz
C	Flash Capacity	8	256KB
DE	Package Code	FN	WLCSP
		LQ	QFN
F	Temperature Range	I	Industrial 85 °C
		Q	Extended Industrial 105 °C
XYZ	Attributes Code	BL400-BL499	Bluetooth 4.1 compliant
		BL500-BL599	Bluetooth 4.2 compliant

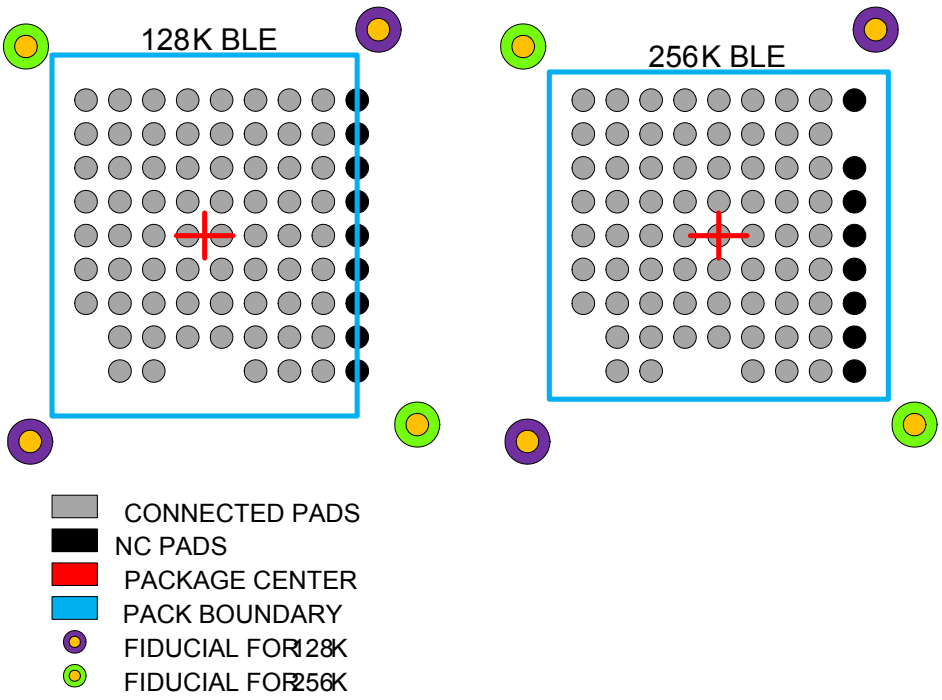
WLCSP Compatibility

The PSoC 4XXX_BLE family has products with 128 KB (16KB SRAM) and 256 KB (32KB SRAM) Flash. Package pin-outs and sizes are identical for the 56-pin QFN package but are different in one dimension for the 68-ball WLCSP.

The 256KB Flash product has an extra column of balls which are required for mechanical integrity purposes in the Chip-Scale package. With consideration for this difference, the land pattern on the PCB may be designed such that either product may be used with no change to the PCB design.

Figure 7 shows the 128KB and 256 KB Flash CSP packages.

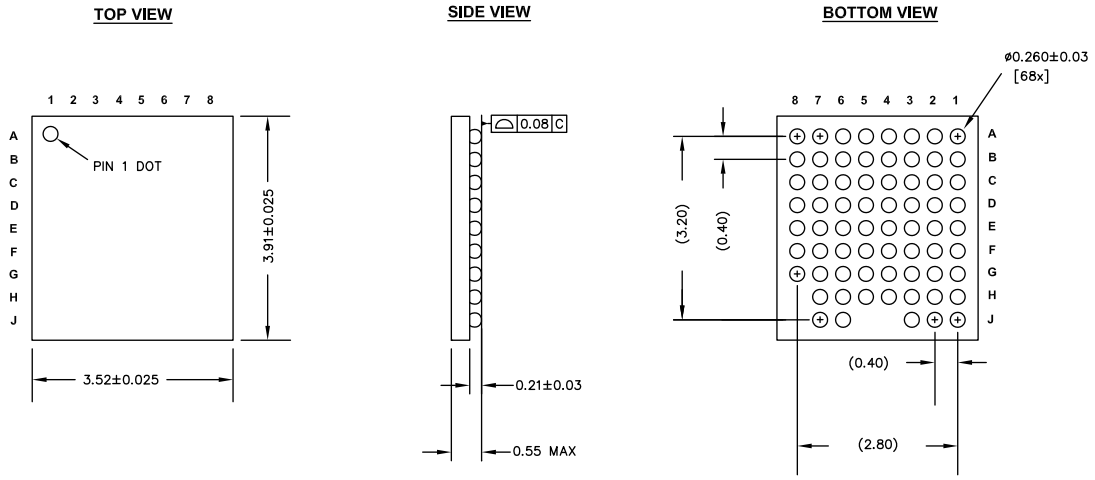
Figure 7. 128KB and 256 KB Flash CSP Packages



The rightmost column of (all NC, No Connect) balls in the 256K BLE WLCSP is for mechanical integrity purposes. The package is thus wider (3.2 mm versus 2.8 mm). All other dimensions are identical. Cypress will provide layout symbols for PCB layout.

The scheme in Figure 7 is implemented to design the PCB for the 256K BLE package with the appropriate space requirements thus allowing use of either package at a later time without redesigning the Printed Circuit Board.

Figure 8. 68-Ball WLCSP Package Outline

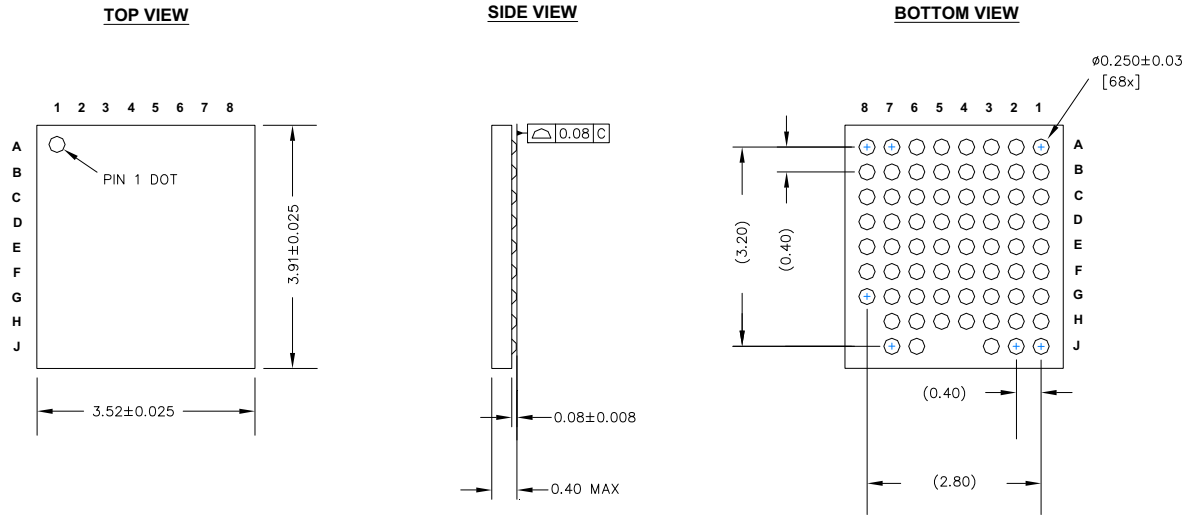


NOTES:

1. REFERENCE JEDEC PUBLICATION 95, DESIGN GUIDE 4.18
2. ALL DIMENSIONS ARE IN MILLIMETERS

001-92343 *A

Figure 9. 68-Ball Thin WLCSP

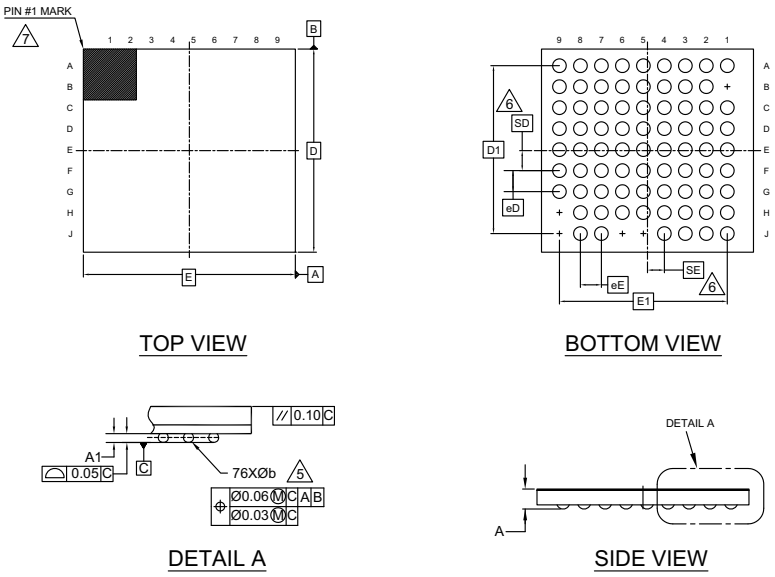


NOTES:

1. REFERENCE JEDEC PUBLICATION 95, DESIGN GUIDE 4.18
2. ALL DIMENSIONS ARE IN MILLIMETERS

001-99408 **

Figure 10. 76-Ball WLCSP Package Outline



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	0.55
A1	0.18	0.21	0.24
D	3.87 BSC		
E	4.04 BSC		
D1	3.20 BSC		
E1	3.20 BSC		
MD	9		
ME	9		
N	76		
Ø b	0.23	0.26	0.29
eD	0.40 BSC		
eE	0.40 BSC		
SD	0.381 BSC		
SE	0.321 BSC		

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
3. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
4. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
6. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
7. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.
9. JEDEC SPECIFICATION NO. REF : N/A

001-96603 *B

Table 59. Acronyms Used in this Document *(continued)*

Acronym	Description
Opamp	operational amplifier
PAL	programmable array logic, see also PLD
PC	program counter
PCB	printed circuit board
PGA	programmable gain amplifier
PHUB	peripheral hub
PHY	physical layer
PICU	port interrupt control unit
PLA	programmable logic array
PLD	programmable logic device, see also PAL
PLL	phase-locked loop
PMDD	package material declaration data sheet
POR	power-on reset
PRES	precise power-on reset
PRS	pseudo random sequence
PS	port read data register
PSoC®	Programmable System-on-Chip™
PSRR	power supply rejection ratio
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RTL	register transfer language
RTR	remote transmission request
RX	receive
SAR	successive approximation register
SC/CT	switched capacitor/continuous time
SCL	I^2C serial clock
SDA	I^2C serial data
S/H	sample and hold
SINAD	signal to noise and distortion ratio
SIO	special input/output, GPIO with advanced features. See GPIO.
SOC	start of conversion
SOF	start of frame
SPI	Serial Peripheral Interface, a communications protocol
SR	slew rate
SRAM	static random access memory

Table 59. Acronyms Used in this Document *(continued)*

Acronym	Description
SRES	software reset
STN	super twisted nematic
SWD	serial wire debug, a test protocol
SWV	single-wire viewer
TD	transaction descriptor, see also DMA
THD	total harmonic distortion
TIA	transimpedance amplifier
TN	twisted nematic
TRM	technical reference manual
TTL	transistor-transistor logic
TX	transmit
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UDB	universal digital block
USB	Universal Serial Bus
USBIO	USB input/output, PSoC pins used to connect to a USB port
VDAC	voltage DAC, see also DAC, IDAC
WDT	watchdog timer
WOL	write once latch, see also NVL
WRES	watchdog timer reset
XRES	external reset I/O pin
XTAL	crystal

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