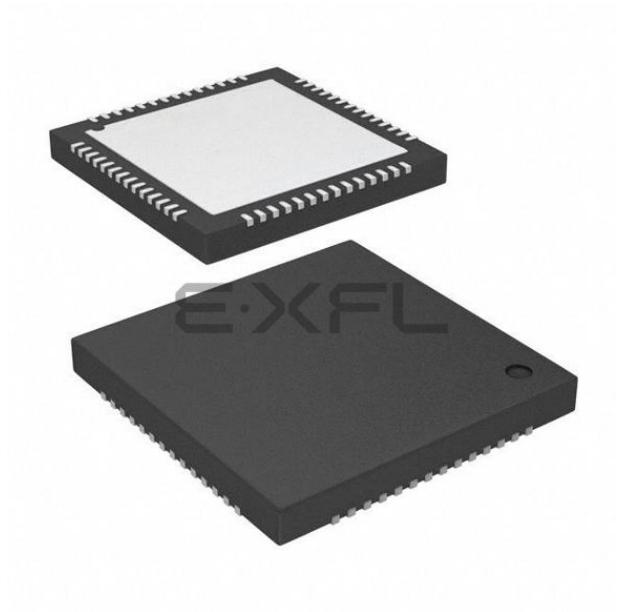
Infineon Technologies - CY8C4248LQQ-BL583 Datasheet



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What is "Embedded - Microcontrollers"?

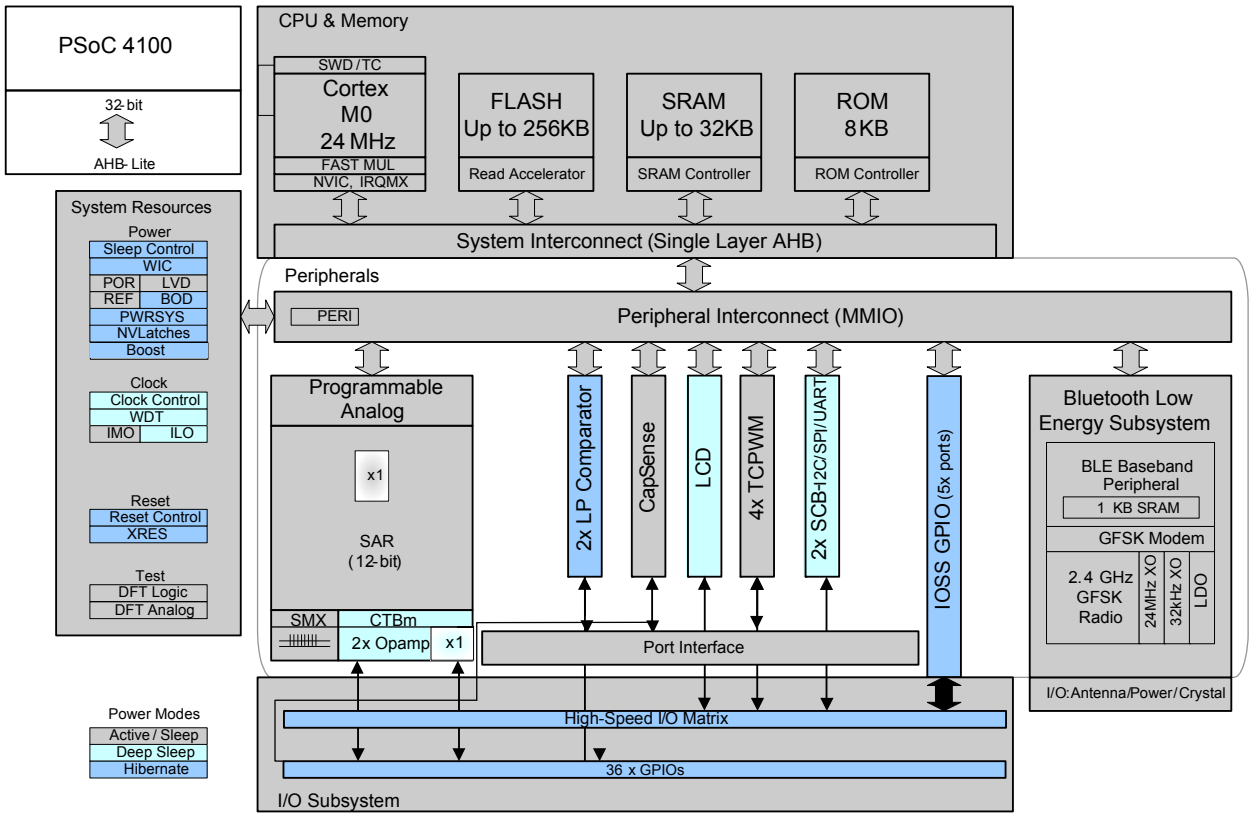
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, IrDA, LINbus, Microwire, SmartCard, SPI, SSP, UART/USART
Peripherals	Bluetooth, Brown-out Detect/Reset, Cap Sense, DMA LCD, LVD, POR, PWM, SmartCard, SmartSense, WDT
Number of I/O	36
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x12b SAR; D/A 2xIDAC
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	56-UFQFN Exposed Pad
Supplier Device Package	56-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4248lqq-bl583

Contents

Figure 2. Block Diagram



The PSoC 4100_BLE devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware.

The Arm SWD interface supports all programming and debug features of the device.

Complete debug-on-chip functionality enables full-device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debugging.

The PSoC Creator IDE provides fully integrated programming and debugging support for the PSoC 4100_BLE devices. The SWD interface is fully compatible with industry-standard third-party tools. With the ability to disable debug features, very robust flash protection, and allowing customer-proprietary functionality to be implemented in on-chip programmable blocks, the PSoC 4100_BLE family provides a level of security not possible with multi-chip application solutions or with microcontrollers.

Debug circuits are enabled by default and can only be disabled in firmware. If not enabled, the only way to re-enable them is to erase the entire device, clear flash protection, and reprogram the device with the new firmware that enables debugging.

Additionally, all device interfaces can be permanently disabled (device security) for applications concerned about phishing attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. Because all programming, debug, and test interfaces are disabled when maximum device security is enabled, PSoC 4100_BLE with device security enabled may not be returned for failure analysis. This is a trade-off the PSoC 4100_BLE allows the customer to make.

Fixed-Function Digital

Timer/Counter/PWM Block

The timer/counter/PWM block consists of four 16-bit counters with user-programmable period length. There is a capture register to record the count value at the time of an event (which may be an I/O event), a period register which is used to either stop or auto-reload the counter when its count is equal to the period register, and compare registers to generate compare value signals which are used as PWM duty cycle outputs. The block also provides true and complementary outputs with programmable offset between them to allow the use as deadband programmable complementary PWM outputs. It also has a kill input to force outputs to a predetermined state; for example, this is used in motor-drive systems when an overcurrent state is indicated and the PWMs driving the FETs need to be shut off immediately with no time for software intervention.

Serial Communication Blocks (SCB)

PSoC 4100_BLE has two SCBs, each of which can implement an I^2C, UART, or SPI interface.

I^2C Mode: The hardware I^2C block implements a full multi-master and slave interface (it is capable of multimaster arbitration). This block is capable of operating at speeds of up to 1 Mbps (Fast-Mode Plus) and has flexible buffering options to reduce the interrupt overhead and latency for the CPU. It also supports EzI^2C that creates a mailbox address range in the memory of PSoC 4100_BLE and effectively reduces the I^2C communication to reading from and writing to an array in the memory. In addition, the block supports an 8-deep FIFO for receive and transmit, which, by increasing the time given for the CPU to read the data, greatly reduces the need for clock stretching caused by the CPU not having read the data on time. The FIFO mode is available in all channels and is very useful in the absence of DMA.

The I^2C peripheral is compatible with I^2C Standard-mode, Fast-mode, and Fast-Mode Plus devices as defined in the NXP I^2C-bus specification and user manual (UM10204). The I^2C bus I/O is implemented with GPIOs in open-drain modes.

SCB1 is fully compliant with Standard-mode (100 kHz), Fast-mode (400 kHz), and Fast-Mode Plus (1 MHz) I^2C signaling specifications when routed to GPIO pins P5.0 and P5.1, except for hot swap capability during I2C active communication. The remaining GPIOs do not meet the hot-swap specification (V_{DD} off; draw < 10-µA current) for Fast mode and Fast-Mode Plus, I_{OL} spec (20 mA) for Fast-Mode Plus, hysteresis spec (0.05 × V_{DD}) for Fast mode and Fast-Mode Plus, and minimum fall-time spec for Fast mode and Fast-Mode Plus.

- GPIO cells, including P5.0 and P5.1, cannot be hot-swapped or powered up independent of the rest of the I^2C system.
- The GPIO pins P5.0 and P5.1 are overvoltage-tolerant but cannot be hot-swapped or powered up independent of the rest of the I^2C system.
- Fast-Mode Plus has an I_{OL} specification of 20 mA at a V_{OL} of 0.4 V. The GPIO cells can sink a maximum of 8 mA I_{OL} with a V_{OL} maximum of 0.6 V.
- Fast mode and Fast-Mode Plus specify minimum Fall times, which are not met with the GPIO cell; the Slow-Strong mode can help meet this spec depending on the bus load.

UART Mode: This is a full-feature UART operating at up to 1 Mbps. It supports automotive single-wire interface (LIN), infrared interface (IrDA), and SmartCard (ISO7816) protocols, all of which are minor variants of the basic UART protocol. In addition, it supports the 9-bit multiprocessor mode that allows the addressing of peripherals connected over common RX and TX lines. Common UART functions such as parity error, break detect, and frame error are supported. An 8-deep FIFO allows much greater CPU service latencies to be tolerated.

SPI Mode: The SPI mode supports full Motorola SPI, TI Secure Simple Pairing (SSP) (essentially adds a start pulse that is used to synchronize SPI Codecs), and National Microwire (half-duplex form of SPI). The SPI block can use the FIFO for transmit and receive.

GPIO

PSoC 4100_BLE has 36 GPIOs. The GPIO block implements the following:

- Eight drive-strength modes:
  - Analog input mode (input and output buffers disabled)
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL)
- Pins 0 and 1 of Port 5 are overvoltage-tolerant Pins
- Individual control of input and output buffer enabling/disabling in addition to drive-strength modes
- Hold mode for latching the previous state (used for retaining the I/O state in Deep-Sleep and Hibernate modes)
- Selectable slew rates for dV/dt-related noise control to improve EMI

The pins are organized in logical entities called ports, which are 8-bit in width. During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix (HSIOM) is used to multiplex between various signals that may connect to an I/O pin. Pin locations for fixed-function peripherals are also fixed to reduce internal multiplexing complexity (these signals do not go through the DSI network). DSI signals are not affected by this and any pin may be routed to any UDB through the DSI network.

Data output and pin-state registers store, respectively, the values to be driven on the pins and the states of the pins themselves.Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it (5 for PSoC 4100_BLE since it has 4.5 ports).

Table 1. PSoC 4100_BLE Pin List (QFN Package) *(continued)*

Pin	Name	Type	Description
40	P2.3	GPIO	Port 2 Pin 3, lcd, csd
41	P2.4	GPIO	Port 2 Pin 4, lcd, csd
42	P2.5	GPIO	Port 2 Pin 5, lcd, csd
43	P2.6	GPIO	Port 2 Pin 6, lcd, csd
44	P2.7	GPIO	Port 2 Pin 7, lcd, csd
45	VREF	REF	1.024-V reference
46	VDDA	POWER	1.71-V to 5.5-V analog supply
47	P3.0	GPIO	Port 3 Pin 0, lcd, csd
48	P3.1	GPIO	Port 3 Pin 1, lcd, csd
49	P3.2	GPIO	Port 3 Pin 2, lcd, csd
50	P3.3	GPIO	Port 3 Pin 3, lcd, csd
51	P3.4	GPIO	Port 3 Pin 4, lcd, csd
52	P3.5	GPIO	Port 3 Pin 5, lcd, csd
53	P3.6	GPIO	Port 3 Pin 6, lcd, csd
54	P3.7	GPIO	Port 3 Pin 7, lcd, csd
55	VSSA	GROUND	Analog ground
56	VCCD	POWER	Regulated 1.8-V supply, connect to 1-µF capacitor
57	EPAD	GROUND	Ground paddle for the QFN package

Table 2. PSoC 4100_BLE Pin List (WLCSP Package)

Pin	Name	Type	Pin Description
A1	VREF	REF	1.024-V reference
A2	VSSA	GROUND	Analog ground
A3	P3.3	GPIO	Port 3 Pin 3, lcd, csd
A4	P3.7	GPIO	Port 3 Pin 7, lcd, csd
A5	VSSD	GROUND	Digital ground
A6	VSSA	GROUND	Analog ground
A7	VCCD	POWER	Regulated 1.8-V supply, connect to 1-µF capacitor
A8	VDDD	POWER	1.71-V to 5.5-V radio supply
B1	P2.3	GPI	Port 2 Pin 3, lcd, csd
B2	VSSA	GROUND	Analog ground
B3	P2.7	GPIO	Port 2 Pin 7, lcd, csd
B4	P3.4	GPIO	Port 3 Pin 4, lcd, csd
B5	P3.5	GPIO	Port 3 Pin 5, lcd, csd
B6	P3.6	GPIO	Port 3 Pin 6, lcd, csd
B7	XTAL32I/P6.1	CLOCK	32.768-kHz crystal or external clock input
B8	XTAL32O/P6.0	CLOCK	32.768-kHz crystal
C1	VSSA	GROUND	Analog ground
C2	P2.2	GPIO	Port 2 Pin 2, lcd, csd
C3	P2.6	GPIO	Port 2 Pin 6, lcd, csd
C4	P3.0	GPIO	Port 3 Pin 0, lcd, csd
C5	P3.1	GPIO	Port 3 Pin 1, lcd, csd

Table 2. PSoC 4100_BLE Pin List (WLCSP Package) *(continued)*

Pin	Name	Type	Pin Description
C6	P3.2	GPIO	Port 3 Pin 2, lcd, csd
C7	XRES	RESET	Reset, active LOW
C8	P4.0	GPIO	Port 4 Pin 0, lcd, csd
D1	P1.7	GPIO	Port 1 Pin 7, lcd, csd
D2	VDDA	POWER	1.71-V to 5.5-V analog supply
D3	P2.0	GPIO	Port 2 Pin 0, lcd, csd
D4	P2.1	GPIO	Port 2 Pin 1, lcd, csd
D5	P2.5	GPIO	Port 2 Pin 5, lcd, csd
D6	VSSD	GROUND	Digital ground
D7	P4.1	GPIO	Port 4 Pin 1, lcd, csd
D8	P5.0	GPIO	Port 5 Pin 0, lcd, csd
E1	P1.2	GPIO	Port 1 Pin 2, lcd, csd
E2	P1.3	GPIO	Port 1 Pin 3, lcd, csd
E3	P1.4	GPIO	Port 1 Pin 4, lcd, csd
E4	P1.5	GPIO	Port 1 Pin 5, lcd, csd
E5	P1.6	GPIO	Port 1 Pin 6, lcd, csd
E6	P2.4	GPIO	Port 2 Pin 4, lcd, csd
E7	P5.1	GPIO	Port 5 Pin 1, lcd, csd
E8	VSSD	GROUND	Digital ground
F1	VSSD	GROUND	Digital ground
F2	P0.7	GPIO	Port 0 Pin 7, lcd, csd
F3	P0.3	GPIO	Port 0 Pin 3, lcd, csd
F4	P1.0	GPIO	Port 1 Pin 0, lcd, csd
F5	P1.1	GPIO	Port 1 Pin 1, lcd, csd
F6	VSSR	GROUND	Radio ground
F7	VSSR	GROUND	Radio ground
F8	VDDR	POWER	1.9-V to 5.5-V radio supply
G1	P0.6	GPIO	Port 0 Pin 6, lcd, csd
G2	VDDD	POWER	1.71-V to 5.5-V digital supply
G3	P0.2	GPIO	Port 0 Pin 2, lcd, csd
G4	VSSD	GROUND	Digital ground
G5	VSSR	GROUND	Radio ground
G6	VSSR	GROUND	Radio ground
G7	GANT	GROUND	Antenna shielding ground
G8	VSSR	GROUND	Radio ground
H1	P0.5	GPIO	Port 0 Pin 5, lcd, csd
H2	P0.1	GPIO	Port 0 Pin 1, lcd, csd
H3	XTAL24O	CLOCK	24-MHz crystal
H4	XTAL24I	CLOCK	24-MHz crystal or external clock input
H5	VSSR	GROUND	Radio ground
H6	VSSR	GROUND	Radio ground
H7	ANT	ANTENNA	Antenna pin
J1	P0.4	GPIO	Port 0 Pin 4, lcd, csd

Table 2. PSoC 4100_BLE Pin List (WLCSP Package) *(continued)*

Pin	Name	Type	Pin Description
J2	P0.0	GPIO	Port 0 Pin 0, lcd, csd
J3	VDDR	POWER	1.9-V to 5.5-V radio supply
J6	VDDR	POWER	1.9-V to 5.5-V radio supply
J7	No Connect	-	-

High-speed I/O matrix (HSIOM) is a group of high-speed switches that routes GPIOs to the resources inside the device. These resources include CapSense, TCPWMs, I^2C, SPI, UART, and LCD. HSIOM_PORT_SELx are 32-bit-wide registers that control the routing of GPIOs. Each register controls one port; four dedicated bits are assigned to each GPIO in the port. This provides up to 16 different options for GPIO routing as shown in Table 3.

Table 3. HSIOM Port Settings

Value	Description
0	Firmware-controlled GPIO
1	Output is firmware-controlled, but Output Enable (OE) is controlled from DSI.
2	Both output and OE are controlled from DSI.
3	Output is controlled from DSI, but OE is firmware-controlled.
4	Pin is a CSD sense pin
5	Pin is a CSD shield pin
6	Pin is connected to AMUXA
7	Pin is connected to AMUXB
8	Pin-specific Active function #0
9	Pin-specific Active function #1
10	Pin-specific Active function #2
11	Reserved
12	Pin is an LCD common pin
13	Pin is an LCD segment pin
14	Pin-specific Deep-Sleep function #0
15	Pin-specific Deep-Sleep function #1

The selection of peripheral function for different GPIO pins is given in Table 4.

Table 4. Port Pin Connections

Name	Analog	Digital (HSIOM_PORT_SELx.SELy) ('x' denotes port number and 'y' denotes pin number)					
		0	8	9	10	14	15
		GPIO	Active #0	Active #1	Active #2	Deep-Sleep #0	Deep-Sleep #1
P0.0	COMP0_INP	GPIO	TCPWM0_P[3]	SCB1_UART_RX[1]		SCB1_I2C_SDA[1]	SCB1_SPI_MOSI[1]
P0.1	COMP0_INN	GPIO	TCPWM0_N[3]	SCB1_UART_TX[1]		SCB1_I2C_SCL[1]	SCB1_SPI_MISO[1]
P0.2		GPIO	TCPWM1_P[3]	SCB1_UART_RTS[1]		COMP0_OUT[0]	SCB1_SPI_SS0[1]
P0.3		GPIO	TCPWM1_N[3]	SCB1_UART_CTS[1]		COMP1_OUT[0]	SCB1_SPI_SCLK[1]
P0.4	COMP1_INP	GPIO	TCPWM1_P[0]	SCB0_UART_RX[1]	EXT_CLK[0]/ ECO_OUT[0]	SCB0_I2C_SDA[1]	SCB0_SPI_MOSI[1]
P0.5	COMP1_INN	GPIO	TCPWM1_N[0]	SCB0_UART_TX[1]		SCB0_I2C_SCL[1]	SCB0_SPI_MISO[1]
P0.6		GPIO	TCPWM2_P[0]	SCB0_UART_RTS[1]		SWDIO[0]	SCB0_SPI_SS0[1]
P0.7		GPIO	TCPWM2_N[0]	SCB0_UART_CTS[1]		SWDCLK[0]	SCB0_SPI_SCLK[1]
P1.0	CTBm1_OA0_INP	GPIO	TCPWM0_P[1]			COMP0_OUT[1]	WCO_OUT[2]
P1.1	CTBm1_OA0_INN	GPIO	TCPWM0_N[1]			COMP1_OUT[1]	SCB1_SPI_SS1
P1.2	CTBm1_OA0_OUT	GPIO	TCPWM1_P[1]				SCB1_SPI_SS2
P1.3	CTBm1_OA1_OUT	GPIO	TCPWM1_N[1]				SCB1_SPI_SS3

Electrical Specifications

Absolute Maximum Ratings

Table 5. Absolute Maximum Ratings[1]

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID1	V_{DDD_ABS}	Analog, digital, or radio supply relative to V_{SS} (V_{SSD} = V_{SSA})	–0.5	–	6	V	Absolute max
SID2	V_{CCD_ABS}	Direct digital core voltage input relative to V_{SSD}	–0.5	–	1.95	V	Absolute max
SID3	V_{GPIO_ABS}	GPIO voltage	–0.5	–	V_{DD} +0.5	V	Absolute max
SID4	I_{GPIO_ABS}	Maximum current per GPIO	–25	–	25	mA	Absolute max
SID5	$I_{GPIO\_injection}$	GPIO injection current, Max for V_{IH} > V_{DDD}, and Min for V_{IL} < V_{SS}	–0.5	–	0.5	mA	Absolute max, current injected per pin
BID57	ESD_HBM	Electrostatic discharge human body model	2200[2]	–	–	V	
BID58	ESD_CDM	Electrostatic discharge charged device model	500	–	–	V	
BID61	LU	Pin current for latch-up	–200	–	200	mA	

Device Level Specifications

All specifications are valid for –40 °C ≤ TA ≤ 105 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

Table 6. DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID6	V_{DD}	Power supply input voltage (V_{DDA} = V_{DDD} = V_{DD})	1.8	–	5.5	V	With regulator enabled
SID7	V_{DD}	Power supply input voltage unregulated (V_{DDA} = V_{DDD} = V_{DD})	1.71	1.8	1.89	V	Internally unregulated Supply
SID8	V_{DDR}	Radio supply voltage (Radio ON)	1.9	–	5.5	V	
SID8A	V_{DDR}	Radio supply voltage (Radio OFF)	1.71	–	5.5	V	
SID9	V_{CCD}	Digital regulator output voltage (for core logic)	–	1.8	–	V	
SID10	C_{VCCD}	Digital regulator output bypass capacitor	1	1.3	1.6	µF	X5R ceramic or better
Active Mode, V_{DD} = 1.71 V to 5.5 V							
SID13	I_{DD3}	Execute from flash; CPU at 3 MHz	–	1.7	–	mA	T = 25 °C, V_{DD} = 3.3 V
SID14	I_{DD4}	Execute from flash; CPU at 3 MHz	–	–	–	mA	T = –40 C to 105 °C
SID15	I_{DD5}	Execute from flash; CPU at 6 MHz	–	2.5	–	mA	T = 25 °C, V_{DD} = 3.3 V
SID16	I_{DD6}	Execute from flash; CPU at 6 MHz	–	–	–	mA	T = –40 °C to 105 °C
SID17	I_{DD7}	Execute from flash; CPU at 12 MHz	–	4	–	mA	T = 25 °C, V_{DD} = 3.3 V
SID18	I_{DD8}	Execute from flash; CPU at 12 MHz	–	–	–	mA	T = –40 °C to 105 °C

Notes
1. Usage above the absolute maximum conditions listed in Table 5 may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.
2. This does not apply to the RF pins (ANT, XTALI, and XTALO). RF pins (ANT, XTALI, and XTALO) are tested for 500-V HBM.

Table 6. DC Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID19	I_{DD9}	Execute from flash; CPU at 24 MHz	–	7.1	–	mA	T = 25 °C, V_{DD} = 3.3 V
SID20	I_{DD10}	Execute from flash; CPU at 24 MHz	–	–	–	mA	T = –40 °C to 105 °C
SID21	I_{DD11}	Execute from flash; CPU at 48 MHz	–	13.4	–	mA	T = 25 °C, V_{DD} = 3.3 V
SID22	I_{DD12}	Execute from flash; CPU at 48 MHz	–	–	–	mA	T = –40 °C to 105 °C
Sleep Mode, V_{DD} = 1.8 V to 5.5 V							
SID23	I_{DD13}	IMO on	–	–	–	mA	T = 25 °C, VDD = 3.3 V, SYSCLK = 3 MHz
Sleep Mode, V_{DD} and V_{DDR} = 1.9 V to 5.5 V							
SID24	I_{DD14}	ECO on	–	–	–	mA	T = 25 °C, VDD = 3.3 V, SYSCLK = 3 MHz
Deep-Sleep Mode, V_{DD} = 1.8 V to 3.6 V							
SID25	I_{DD15}	WDT with WCO on	–	1.3	–	µA	T = 25 °C, V_{DD} = 3.3 V
SID26	I_{DD16}	WDT with WCO on	–	–	–	µA	T = –40 °C to 105 °C
Deep-Sleep Mode, V_{DD} = 3.6 V to 5.5 V							
SID27	I_{DD17}	WDT with WCO on	–	–	–	µA	T = 25 °C, V_{DD} = 5 V
SID28	I_{DD18}	WDT with WCO on	–	–	–	µA	T = –40 °C to 105 °C
Deep-Sleep Mode, V_{DD} = 1.71 V to 1.89 V (Regulator Bypassed)							
SID29	I_{DD19}	WDT with WCO on	–	–	–	µA	T = 25 °C
SID30	I_{DD20}	WDT with WCO on	–	–	–	µA	T = –40 °C to 105 °C
Deep-Sleep Mode, V_{DD} = 2.5 V to 3.6 V							
SID31	I_{DD21}	Opamp on	–	–	–	µA	T = 25 °C, V_{DD} = 3.3 V
SID32	I_{DD22}	Opamp on	–	–	–	µA	T = –40 °C to 105 °C
Deep-Sleep Mode, V_{DD} = 3.6 V to 5.5 V							
SID33	I_{DD23}	Opamp on	–	–	–	µA	T = 25 °C, V_{DD} = 5 V
SID34	I_{DD24}	Opamp on	–	–	–	µA	T = –40 °C to 105 °C
Hibernate Mode, V_{DD} = 1.8 V to 3.6 V							
SID37	I_{DD27}	GPIO and reset active	–	150	–	nA	T = 25 °C, V_{DD} = 3.3 V
SID38	I_{DD28}	GPIO and reset active	–	–	–	nA	T = –40 °C to 105 °C
Hibernate Mode, V_{DD} = 3.6 V to 5.5 V							
SID39	I_{DD29}	GPIO and reset active	–	–	–	nA	T = 25 °C, V_{DD} = 5 V
SID40	I_{DD30}	GPIO and reset active	–	–	–	nA	T = –40 °C to 105 °C
Hibernate Mode, V_{DD} = 1.71 V to 1.89 V (Regulator Bypassed)							
SID41	I_{DD31}	GPIO and reset active	–	–	–	nA	T = 25 °C
SID42	I_{DD32}	GPIO and reset active	–	–	–	nA	T = –40 °C to 105 °C

GPIO

Table 8. GPIO DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID58	V_{IH}	Input voltage HIGH threshold	0.7 × V_{DD}	–	–	V	CMOS input
SID59	V_{IL}	Input voltage LOW threshold	–	–	0.3 × V_{DD}	V	CMOS input
SID60	V_{IH}	LVTTL input, V_{DD} < 2.7 V	0.7 × V_{DD}	–	-	V	
SID61	V_{IL}	LVTTL input, V_{DD} < 2.7 V	–	–	0.3× V_{DD}	V	
SID62	V_{IH}	LVTTL input, V_{DD} ≥ 2.7 V	2.0	–	-	V	
SID63	V_{IL}	LVTTL input, V_{DD} ≥ 2.7 V	–	–	0.8	V	
SID64	V_{OH}	Output voltage HIGH level	V_{DD} –0.6	–	–	V	I_{OH} = 4 mA at 3.3-V V_{DD}
SID65	V_{OH}	Output voltage HIGH level	V_{DD} –0.5	–	–	V	I_{OH} = 1 mA at 1.8-V V_{DD}
SID66	V_{OL}	Output voltage LOW level	–	–	0.6	V	I_{OL} = 8 mA at 3.3-V V_{DD}
SID67	V_{OL}	Output voltage LOW level	–	–	0.6	V	I_{OL}= 4 mA at 1.8-V V_{DD}
SID68	V_{OL}	Output voltage LOW level	–	–	0.4	V	I_{OL} = 3 mA at 3.3-V V_{DD}
SID69	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	
SID70	$R_{PULLDOWN}$	Pull-down resistor	3.5	5.6	8.5	kΩ	
SID71	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	25 °C, V_{DD} = 3.3 V
SID72	I_{IL_CTBM}	Input leakage on CTBm input pins	–	–	4	nA	
SID73	C_{IN}	Input capacitance	–	–	7	pF	
SID74	V_{HYSTTL}	Input hysteresis LVTTL	25	40		mV	V_{DD} > 2.7 V
SID75	$V_{HYSCMOS}$	Input hysteresis CMOS	0.05 × V_{DD}	–	–	mV	
SID76	I_{DIODE}	Current through protection diode to V_{DD}/V_{SS}	–	–	100	µA	Except for overvoltage-toler ant pins (P5.0 and P5.1)
SID77	I_{TOT_GPIO}	Maximum total source or sink chip current	–	–	200	mA	

Table 9. GPIO AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID78	T_{RISEF}	Rise time in Fast-Strong mode	2	–	12	ns	3.3-V V_{DDD}, C_{LOAD} = 25 pF
SID79	T_{FALLF}	Fall time in Fast-Strong mode	2	–	12	ns	3.3-V V_{DDD}, C_{LOAD} = 25 pF
SID80	T_{RISES}	Rise time in Slow-Strong mode	10	–	60	ns	3.3-V V_{DDD}, C_{LOAD} = 25 pF
SID81	T_{FALLS}	Fall time in Slow-Strong mode	10	–	60	ns	3.3-V V_{DDD}, C_{LOAD} = 25 pF

Note
3. V_{IH} must not exceed V_{DDD} + 0.2 V.

Table 9. GPIO AC Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID82	$F_{GPIOUT1}$	GPIO Fout; 3.3 V ≤ V_{DD} ≤ 5.5 V. Fast-Strong mode	–	–	33	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID83	$F_{GPIOUT2}$	GPIO Fout; 1.7 V≤ V_{DD} ≤ 3.3 V. Fast-Strong mode	–	–	16.7	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID84	$F_{GPIOUT3}$	GPIO Fout; 3.3 V ≤ V_{DD} ≤ 5.5 V. Slow-Strong mode	–	–	7	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID85	$F_{GPIOUT4}$	GPIO Fout; 1.7 V ≤ V_{DD} ≤ 3.3 V. Slow-Strong mode	–	–	3.5	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID86	F_{GPIOIN}	GPIO input operating frequency; 1.71 V ≤ V_{DD} ≤ 5.5 V	–	–	48	MHz	90/10% V_{IO}

Table 10. OVT GPIO DC Specifications (P5_0 and P5_1 Only)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID71A	I_{IL}	Input leakage current (absolute value), V_{IH} > V_{DD}	–	–	10	µA	25 °C, V_{DD} = 0 V, V_{IH}= 3.0 V
SID66A	V_{OL}	Output voltage LOW level	–	–	0.4	V	I_{OL} = 20 mA, V_{DD} > 2.9 V

Table 11. OVT GPIO AC Specifications (P5_0 and P5_1 Only)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID78A	T_{RISE_OVFS}	Output rise time in Fast-Strong mode	1.5	–	12	ns	25-pF load, 10%–90%, V_{DD}=3.3 V
SID79A	T_{FALL_OVFS}	Output fall time in Fast-Strong mode	1.5	–	12	ns	25-pF load, 10%–90%, V_{DD}=3.3 V
SID80A	T_{RISSS}	Output rise time in Slow-Strong mode	10	–	60	ns	25-pF load, 10%–90%, V_{DD}=3.3 V
SID81A	T_{FALLSS}	Output fall time in Slow-Strong mode	10	–	60	ns	25-pF load, 10%–90%, V_{DD}=3.3 V
SID82A	$F_{GPIOUT1}$	GPIO F_{OUT}; 3.3 V ≤ V_{DD} ≤ 5.5 V Fast-Strong mode	–	–	24	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID83A	$F_{GPIOUT2}$	GPIO F_{OUT}; 1.71 V ≤ V_{DD} ≤ 3.3 V Fast-Strong mode	–	–	16	MHz	90/10%, 25-pF load, 60/40 duty cycle

CSD

Table 20. CSD Block Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID179	V_{CSD}	Voltage range of operation	1.71	–	5.5	V	
SID180	IDAC1	DNL for 8-bit resolution	–1	–	1	LSB	
SID181	IDAC1	INL for 8-bit resolution	–3	–	3	LSB	
SID182	IDAC2	DNL for 7-bit resolution	–1	–	1	LSB	
SID183	IDAC2	INL for 7-bit resolution	–3	–	3	LSB	
SID184	SNR	Ratio of counts of finger to noise	5	–	–	Ratio	Capacitance range of 9 pF to 35 pF, 0.1-pF sensitivity. Radio is not operating during the scan
SID185	I_{DAC1_CRT1}	Output current of IDAC1 (8 bits) in High range	–	612	–	µA	
SID186	I_{DAC1_CRT2}	Output current of IDAC1 (8 bits) in Low range	–	306	–	µA	
SID187	I_{DAC2_CRT1}	Output current of IDAC2 (7 bits) in High range	–	305	–	µA	
SID188	I_{DAC2_CRT2}	Output current of IDAC2 (7 bits) in Low range	–	153	–	µA	

Digital Peripherals

Timer

Table 21. Timer DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID189	I_{TIM1}	Block current consumption at 3 MHz	–	–	42	µA	16-bit timer, 85 °C
SID189A			–	–	46	µA	16-bit timer, 105 °C
SID190	I_{TIM2}	Block current consumption at 12 MHz	–	–	130	µA	16-bit timer, 85 °C
SID190A			–	–	137	µA	16-bit timer, 105 °C
SID191	I_{TIM3}	Block current consumption at 48 MHz	–	–	535	µA	16-bit timer, 85 °C
SID191A			–	–	560	µA	16-bit timer, 105 °C

Table 22. Timer AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID192	$T_{TIMFREQ}$	Operating frequency	F_{CLK}	–	48	MHz	
SID193	$T_{CAPWINT}$	Capture pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	
SID194	$T_{CAPWEXT}$	Capture pulse width (external)	$2 \times T_{CLK}$	–	–	ns	
SID195	T_{TIMRES}	Timer resolution	T_{CLK}	–	–	ns	
SID196	$T_{TENWIDINT}$	Enable pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	
SID197	$T_{TENWIDEXT}$	Enable pulse width (external)	$2 \times T_{CLK}$	–	–	ns	
SID198	$T_{TIMRESWINT}$	Reset pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	
SID199	$T_{TIMRESEXT}$	Reset pulse width (external)	$2 \times T_{CLK}$	–	–	ns	

Table 50. External Clock Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID301	ExtClkFreq	External clock input frequency	0	–	48	MHz	CMOS input level only
SID302	ExtClkDuty	Duty cycle; Measured at $V_{DD}/2$	45	–	55	%	CMOS input level only

Table 51. UDB AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
Data Path performance							
SID303	$F_{MAX-TIMER}$	Max frequency of 16-bit timer in a UDB pair	–	–	48	MHz	
SID304	$F_{MAX-ADDER}$	Max frequency of 16-bit adder in a UDB pair	–	–	48	MHz	
SID305	F_{MAX_CRC}	Max frequency of 16-bit CRC/PRS in a UDB pair	–	–	48	MHz	
PLD Performance in UDB							
SID306	F_{MAX_PLD}	Max frequency of 2-pass PLD function in a UDB pair	–	–	48	MHz	
Clock to Output Performance							
SID307	$T_{CLK\_OUT\_UDB1}$	Prop. delay for clock in to data out at 25 °C, Typical	–	15	–	ns	
SID308	$T_{CLK\_OUT\_UDB2}$	Prop. delay for clock in to data out, Worst case	–	25	–	ns	

Table 52. BLE Subsystem

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
RF Receiver Specification							
SID340	RXS, IDLE	RX sensitivity with idle transmitter	–	–89	–	dBm	
SID340A		RX sensitivity with idle transmitter excluding Balun loss	–	–91	–	dBm	Guaranteed by design simulation
SID341	RXS, DIRTY	RX sensitivity with dirty transmitter	–	–87	–70	dBm	RF-PHY Specification (RCV-LE/CA/01/C)
SID342	RXS, HIGHGAIN	RX sensitivity in high-gain mode with idle transmitter	–	–91	–	dBm	
SID343	PRXMAX	Maximum input power	–10	–1	–	dBm	RF-PHY Specification (RCV-LE/CA/06/C)
SID344	CI1	Cochannel interference, Wanted signal at –67 dBm and Interferer at FRX	–	9	21	dB	RF-PHY Specification (RCV-LE/CA/03/C)
SID345	CI2	Adjacent channel interference Wanted signal at –67 dBm and Interferer at FRX ±1 MHz	–	3	15	dB	RF-PHY Specification (RCV-LE/CA/03/C)
SID346	CI3	Adjacent channel interference Wanted signal at –67 dBm and Interferer at FRX ±2 MHz	–	–29	–	dB	RF-PHY Specification (RCV-LE/CA/03/C)

Table 52. BLE Subsystem *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
RSSI Specifications							
SID386	RSSI, ACC	RSSI accuracy	–	±5	–	dB	
SID387	RSSI, RES	RSSI resolution	–	1	–	dB	
SID388	RSSI, PER	RSSI sample period	–	6	–	µs	

Table 53. ECO Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID389	F_{ECO}	Crystal frequency	–	24	–	MHz	
SID390	F_{TOL}	Frequency tolerance	–50	–	50	ppm	
SID391	ESR	Equivalent series resistance	–	–	60	Ω	
SID392	PD	Drive level	–	–	100	µW	
SID393	T_{START1}	Startup time (Fast Charge on)	–	–	850	µs	
SID394	T_{START2}	Startup time (Fast Charge off)	–	–	3	ms	
SID395	C_L	Load capacitance	–	8	–	pF	
SID396	C0	Shunt capacitance	–	1.1	–	pF	
SID397	I_{ECO}	Operating current	–	1400	–	µA	Includes LDO+BG current

Table 54. WCO Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID398	F_{WCO}	Crystal frequency	–	32.768	–	kHz	
SID399	FTOL	Frequency tolerance	–	50	–	ppm	
SID400	ESR	Equivalent series resistance	–	50	–	kΩ	
SID401	PD	Drive level	–	–	1	µW	
SID402	T_{START}	Startup time	–	–	500	ms	
SID403	C_L	Crystal load capacitance	6	–	12.5	pF	
SID404	C0	Crystal shunt capacitance	–	1.35	–	pF	
SID405	I_{WCO1}	Operating current (High-Power mode)	–	–	8	µA	
SID406	I_{WCO2}	Operating current (low-power mode)	–	–	1	µA	85 °C
SID406A			–	–	2.6	µA	105 °C

Packaging

Table 55. Package Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
T_A	Operating ambient temperature	–	–40	25.00	105	°C
T_J	Operating junction temperature	–	–40	–	125	°C
T_{JA}	Package θ_{JA} (56-pin QFN)	–	–	16.9	–	°C/watt
T_{JC}	Package θ_{JC} (56-pin QFN)	–	–	9.7	–	°C/watt
T_{JA}	Package θ_{JA} (76-ball WLCSP)	–	–	20.1	–	°C/watt
T_{JC}	Package θ_{JC} (76-ball WLCSP)	–	–	0.19	–	°C/watt
T_{JA}	Package θ_{JA} (76-ball Thin WLCSP)	–	–	20.9	–	°C/watt
T_{JC}	Package θ_{JC} (76-ball Thin WLCSP)	–	–	0.17	–	°C/watt
T_{JA}	Package θ_{JA} (68-ball WLCSP)		–	16.6	–	°C/watt
T_{JC}	Package θ_{JC} (68-ball WLCSP)		–	0.19	–	°C/watt
T_{JA}	Package θ_{JA} (68-ball Thin WLCSP)		–	16.6	–	°C/watt
T_{JC}	Package θ_{JC} (68-ball Thin WLCSP)		–	0.19	–	°C/watt

Table 56. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time at Peak Temperature
All packages	260 °C	30 seconds

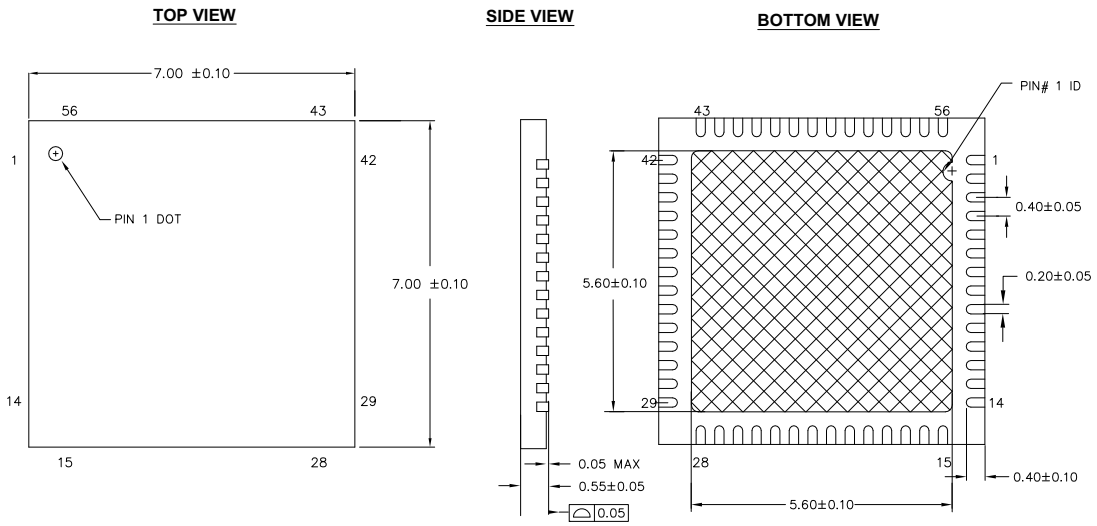
Table 57. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Package	MSL
56-pin QFN	MSL 3
All WLCSP packages	MSL 1

Table 58. Package Details

Spec ID	Package	Description
001-58740 Rev. *C	56-pin QFN	7.0 mm × 7.0 mm × 0.6 mm
001-96603 Rev. *A	76-ball WLCSP	4.04 mm × 3.87 mm × 0.55 mm
002-10658, Rev. **	76-ball thin WLCSP	4.04 mm × 3.87 mm × 0.4 mm
001-92343 Rev. *A	68-ball WLCSP	3.52 mm × 3.91 mm × 0.55 mm
001-99408 Rev **	68-ball Thin WLCSP	52 mm × 3.91 mm × 0.4 mm

Figure 6. 56-Pin QFN 7 mm × 7 mm × 0.6 mm



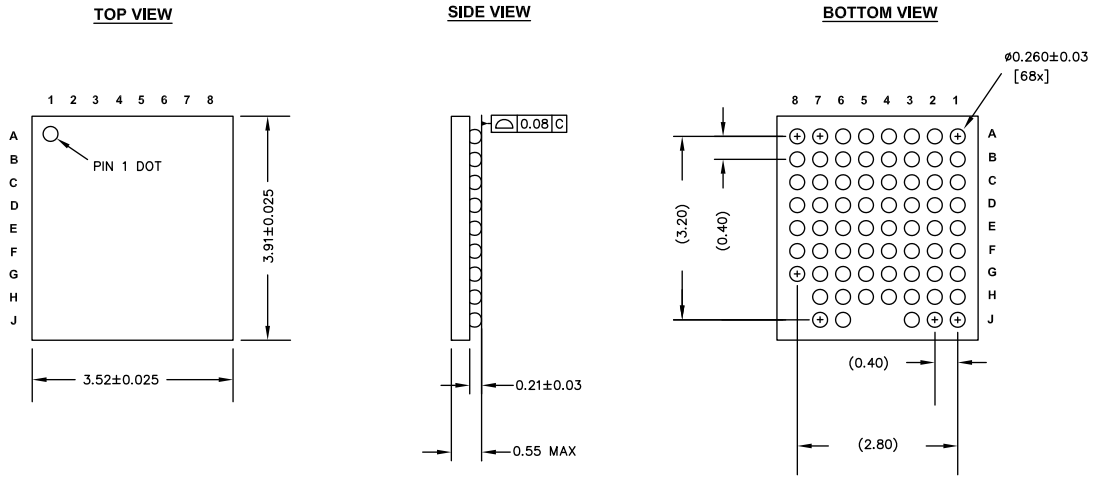
NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. BASED ON REF JEDEC # MO-248
3. ALL DIMENSIONS ARE IN MILLIMETERS

001-58740 *C

The center pad on the QFN package must be connected to ground (V_{SS}) for the proper operation of the device.

Figure 8. 68-Ball WLCSP Package Outline

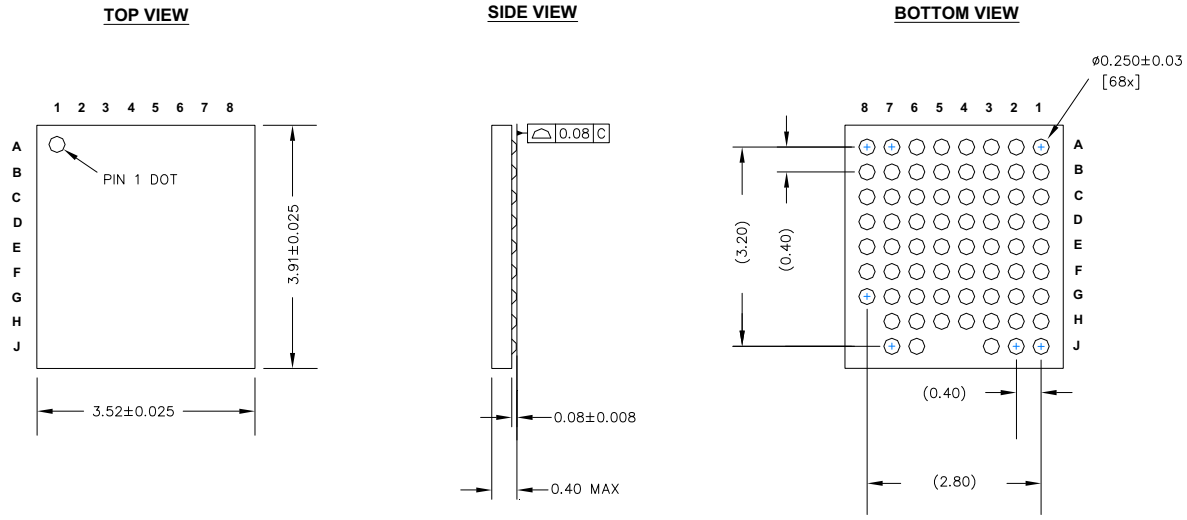


NOTES:

1. REFERENCE JEDEC PUBLICATION 95, DESIGN GUIDE 4.18
2. ALL DIMENSIONS ARE IN MILLIMETERS

001-92343 *A

Figure 9. 68-Ball Thin WLCSP

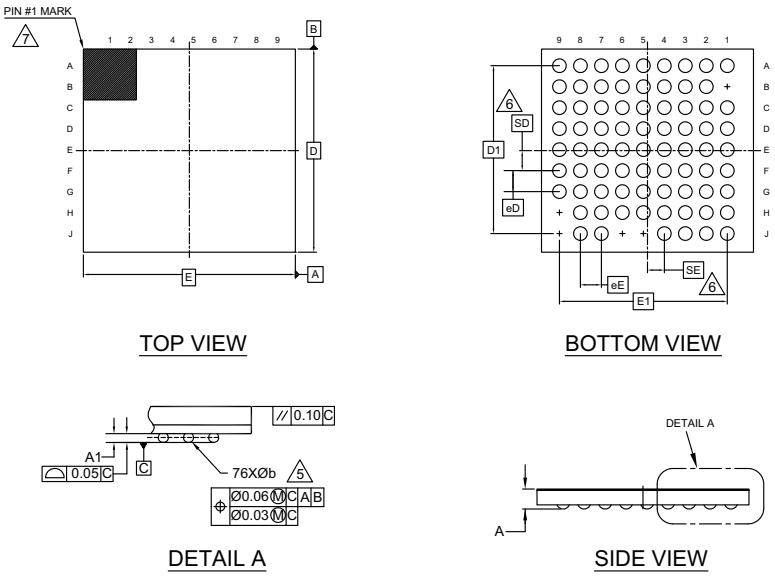


NOTES:

1. REFERENCE JEDEC PUBLICATION 95, DESIGN GUIDE 4.18
2. ALL DIMENSIONS ARE IN MILLIMETERS

001-99408 **

Figure 10. 76-Ball WLCSP Package Outline



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	0.55
A1	0.18	0.21	0.24
D	3.87 BSC		
E	4.04 BSC		
D1	3.20 BSC		
E1	3.20 BSC		
MD	9		
ME	9		
N	76		
Ø b	0.23	0.26	0.29
eD	0.40 BSC		
eE	0.40 BSC		
SD	0.381 BSC		
SE	0.321 BSC		

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
3. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
4. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
6. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
7. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.
9. JEDEC SPECIFICATION NO. REF : N/A

001-96603 *B

Acronyms

Table 59. Acronyms Used in this Document

Acronym	Description
ABUS	analog local bus
ADC	analog-to-digital converter
AG	analog global
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an Arm data transfer bus
ALU	arithmetic logic unit
AMUXBUS	analog multiplexer bus
API	application programming interface
APSR	application program status register
Arm®	advanced RISC machine, a CPU architecture
ATM	automatic thump mode
BW	bandwidth
CAN	Controller Area Network, a communications protocol
CMRR	common-mode rejection ratio
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
DAC	digital-to-analog converter, see also IDAC, VDAC
DFB	digital filter block
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DMIPS	Dhrystone million instructions per second
DMA	direct memory access, see also TD
DNL	differential nonlinearity, see also INL
DNU	do not use
DR	port write data registers
DSI	digital system interconnect
DWT	data watchpoint and trace
ECC	error correcting code
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
EMIF	external memory interface
EOC	end of conversion
EOF	end of frame
EPSR	execution program status register
ESD	electrostatic discharge

Table 59. Acronyms Used in this Document *(continued)*

Acronym	Description
ETM	embedded trace macrocell
FET	field-effect transistor
FIR	finite impulse response, see also IIR
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output, applies to a PSoC pin
HCI	host controller interface
HVI	high-voltage interrupt, see also LVI, LVD
IC	integrated circuit
IDAC	current DAC, see also DAC, VDAC
IDE	integrated development environment
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
IIR	infinite impulse response, see also FIR
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
INL	integral nonlinearity, see also DNL
I/O	input/output, see also GPIO, DIO, SIO, USBIO
IPOR	initial power-on reset
IPSR	interrupt program status register
IRQ	interrupt request
ITM	instrumentation trace macrocell
LCD	liquid crystal display
LIN	Local Interconnect Network, a communications protocol.
LR	link register
LUT	lookup table
LVD	low-voltage detect, see also LVI
LVI	low-voltage interrupt, see also HVI
LVTTL	low-voltage transistor-transistor logic
MAC	multiply-accumulate
MCU	microcontroller unit
MISO	master-in slave-out
NC	no connect
NMI	nonmaskable interrupt
NRZ	non-return-to-zero
NVIC	nested vectored interrupt controller
NVL	nonvolatile latch, see also WOL

Table 59. Acronyms Used in this Document *(continued)*

Acronym	Description
Opamp	operational amplifier
PAL	programmable array logic, see also PLD
PC	program counter
PCB	printed circuit board
PGA	programmable gain amplifier
PHUB	peripheral hub
PHY	physical layer
PICU	port interrupt control unit
PLA	programmable logic array
PLD	programmable logic device, see also PAL
PLL	phase-locked loop
PMDD	package material declaration data sheet
POR	power-on reset
PRES	precise power-on reset
PRS	pseudo random sequence
PS	port read data register
PSoC®	Programmable System-on-Chip™
PSRR	power supply rejection ratio
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RTL	register transfer language
RTR	remote transmission request
RX	receive
SAR	successive approximation register
SC/CT	switched capacitor/continuous time
SCL	I^2C serial clock
SDA	I^2C serial data
S/H	sample and hold
SINAD	signal to noise and distortion ratio
SIO	special input/output, GPIO with advanced features. See GPIO.
SOC	start of conversion
SOF	start of frame
SPI	Serial Peripheral Interface, a communications protocol
SR	slew rate
SRAM	static random access memory

Table 59. Acronyms Used in this Document *(continued)*

Acronym	Description
SRES	software reset
STN	super twisted nematic
SWD	serial wire debug, a test protocol
SWV	single-wire viewer
TD	transaction descriptor, see also DMA
THD	total harmonic distortion
TIA	transimpedance amplifier
TN	twisted nematic
TRM	technical reference manual
TTL	transistor-transistor logic
TX	transmit
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UDB	universal digital block
USB	Universal Serial Bus
USBIO	USB input/output, PSoC pins used to connect to a USB port
VDAC	voltage DAC, see also DAC, IDAC
WDT	watchdog timer
WOL	write once latch, see also NVL
WRES	watchdog timer reset
XRES	external reset I/O pin
XTAL	crystal

Revision History

Description Title: PSoC® 4: PSoC 4100_BLE Family Datasheet Programmable System-on-Chip (PSoC®) Document Number: 002-23052				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	6078076	PMAD/ WKA	02/22/2018	New datasheet