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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, IrDA, LINbus, Microwire, SmartCard, SPI, SSP, UART/USART
Peripherals	Bluetooth, Brown-out Detect/Reset, Cap Sense, DMA LCD, LVD, POR, PWM, SmartCard, SmartSense, WDT
Number of I/O	36
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x12b SAR; D/A 2xIDAC
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	56-UFQFN Exposed Pad
Supplier Device Package	56-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4248lqq-bl583t

Fixed-Function Digital

Timer/Counter/PWM Block

The timer/counter/PWM block consists of four 16-bit counters with user-programmable period length. There is a capture register to record the count value at the time of an event (which may be an I/O event), a period register which is used to either stop or auto-reload the counter when its count is equal to the period register, and compare registers to generate compare value signals which are used as PWM duty cycle outputs. The block also provides true and complementary outputs with programmable offset between them to allow the use as deadband programmable complementary PWM outputs. It also has a kill input to force outputs to a predetermined state; for example, this is used in motor-drive systems when an overcurrent state is indicated and the PWMs driving the FETs need to be shut off immediately with no time for software intervention.

Serial Communication Blocks (SCB)

PSoC 4100_BLE has two SCBs, each of which can implement an I^2C, UART, or SPI interface.

I^2C Mode: The hardware I^2C block implements a full multi-master and slave interface (it is capable of multimaster arbitration). This block is capable of operating at speeds of up to 1 Mbps (Fast-Mode Plus) and has flexible buffering options to reduce the interrupt overhead and latency for the CPU. It also supports EzI^2C that creates a mailbox address range in the memory of PSoC 4100_BLE and effectively reduces the I^2C communication to reading from and writing to an array in the memory. In addition, the block supports an 8-deep FIFO for receive and transmit, which, by increasing the time given for the CPU to read the data, greatly reduces the need for clock stretching caused by the CPU not having read the data on time. The FIFO mode is available in all channels and is very useful in the absence of DMA.

The I^2C peripheral is compatible with I^2C Standard-mode, Fast-mode, and Fast-Mode Plus devices as defined in the NXP I^2C-bus specification and user manual (UM10204). The I^2C bus I/O is implemented with GPIOs in open-drain modes.

SCB1 is fully compliant with Standard-mode (100 kHz), Fast-mode (400 kHz), and Fast-Mode Plus (1 MHz) I^2C signaling specifications when routed to GPIO pins P5.0 and P5.1, except for hot swap capability during I2C active communication. The remaining GPIOs do not meet the hot-swap specification (V_{DD} off; draw < 10-µA current) for Fast mode and Fast-Mode Plus, I_{OL} spec (20 mA) for Fast-Mode Plus, hysteresis spec (0.05 × V_{DD}) for Fast mode and Fast-Mode Plus, and minimum fall-time spec for Fast mode and Fast-Mode Plus.

- GPIO cells, including P5.0 and P5.1, cannot be hot-swapped or powered up independent of the rest of the I^2C system.
- The GPIO pins P5.0 and P5.1 are overvoltage-tolerant but cannot be hot-swapped or powered up independent of the rest of the I^2C system.
- Fast-Mode Plus has an I_{OL} specification of 20 mA at a V_{OL} of 0.4 V. The GPIO cells can sink a maximum of 8 mA I_{OL} with a V_{OL} maximum of 0.6 V.
- Fast mode and Fast-Mode Plus specify minimum Fall times, which are not met with the GPIO cell; the Slow-Strong mode can help meet this spec depending on the bus load.

UART Mode: This is a full-feature UART operating at up to 1 Mbps. It supports automotive single-wire interface (LIN), infrared interface (IrDA), and SmartCard (ISO7816) protocols, all of which are minor variants of the basic UART protocol. In addition, it supports the 9-bit multiprocessor mode that allows the addressing of peripherals connected over common RX and TX lines. Common UART functions such as parity error, break detect, and frame error are supported. An 8-deep FIFO allows much greater CPU service latencies to be tolerated.

SPI Mode: The SPI mode supports full Motorola SPI, TI Secure Simple Pairing (SSP) (essentially adds a start pulse that is used to synchronize SPI Codecs), and National Microwire (half-duplex form of SPI). The SPI block can use the FIFO for transmit and receive.

GPIO

PSoC 4100_BLE has 36 GPIOs. The GPIO block implements the following:

- Eight drive-strength modes:
  - Analog input mode (input and output buffers disabled)
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL)
- Pins 0 and 1 of Port 5 are overvoltage-tolerant Pins
- Individual control of input and output buffer enabling/disabling in addition to drive-strength modes
- Hold mode for latching the previous state (used for retaining the I/O state in Deep-Sleep and Hibernate modes)
- Selectable slew rates for dV/dt-related noise control to improve EMI

The pins are organized in logical entities called ports, which are 8-bit in width. During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix (HSIOM) is used to multiplex between various signals that may connect to an I/O pin. Pin locations for fixed-function peripherals are also fixed to reduce internal multiplexing complexity (these signals do not go through the DSI network). DSI signals are not affected by this and any pin may be routed to any UDB through the DSI network.

Data output and pin-state registers store, respectively, the values to be driven on the pins and the states of the pins themselves.Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it (5 for PSoC 4100_BLE since it has 4.5 ports).

Table 2. PSoC 4100_BLE Pin List (WLCSP Package) *(continued)*

Pin	Name	Type	Pin Description
J2	P0.0	GPIO	Port 0 Pin 0, lcd, csd
J3	VDDR	POWER	1.9-V to 5.5-V radio supply
J6	VDDR	POWER	1.9-V to 5.5-V radio supply
J7	No Connect	-	-

High-speed I/O matrix (HSIOM) is a group of high-speed switches that routes GPIOs to the resources inside the device. These resources include CapSense, TCPWMs, I^2C, SPI, UART, and LCD. HSIOM_PORT_SELx are 32-bit-wide registers that control the routing of GPIOs. Each register controls one port; four dedicated bits are assigned to each GPIO in the port. This provides up to 16 different options for GPIO routing as shown in Table 3.

Table 3. HSIOM Port Settings

Value	Description
0	Firmware-controlled GPIO
1	Output is firmware-controlled, but Output Enable (OE) is controlled from DSI.
2	Both output and OE are controlled from DSI.
3	Output is controlled from DSI, but OE is firmware-controlled.
4	Pin is a CSD sense pin
5	Pin is a CSD shield pin
6	Pin is connected to AMUXA
7	Pin is connected to AMUXB
8	Pin-specific Active function #0
9	Pin-specific Active function #1
10	Pin-specific Active function #2
11	Reserved
12	Pin is an LCD common pin
13	Pin is an LCD segment pin
14	Pin-specific Deep-Sleep function #0
15	Pin-specific Deep-Sleep function #1

The selection of peripheral function for different GPIO pins is given in Table 4.

Table 4. Port Pin Connections

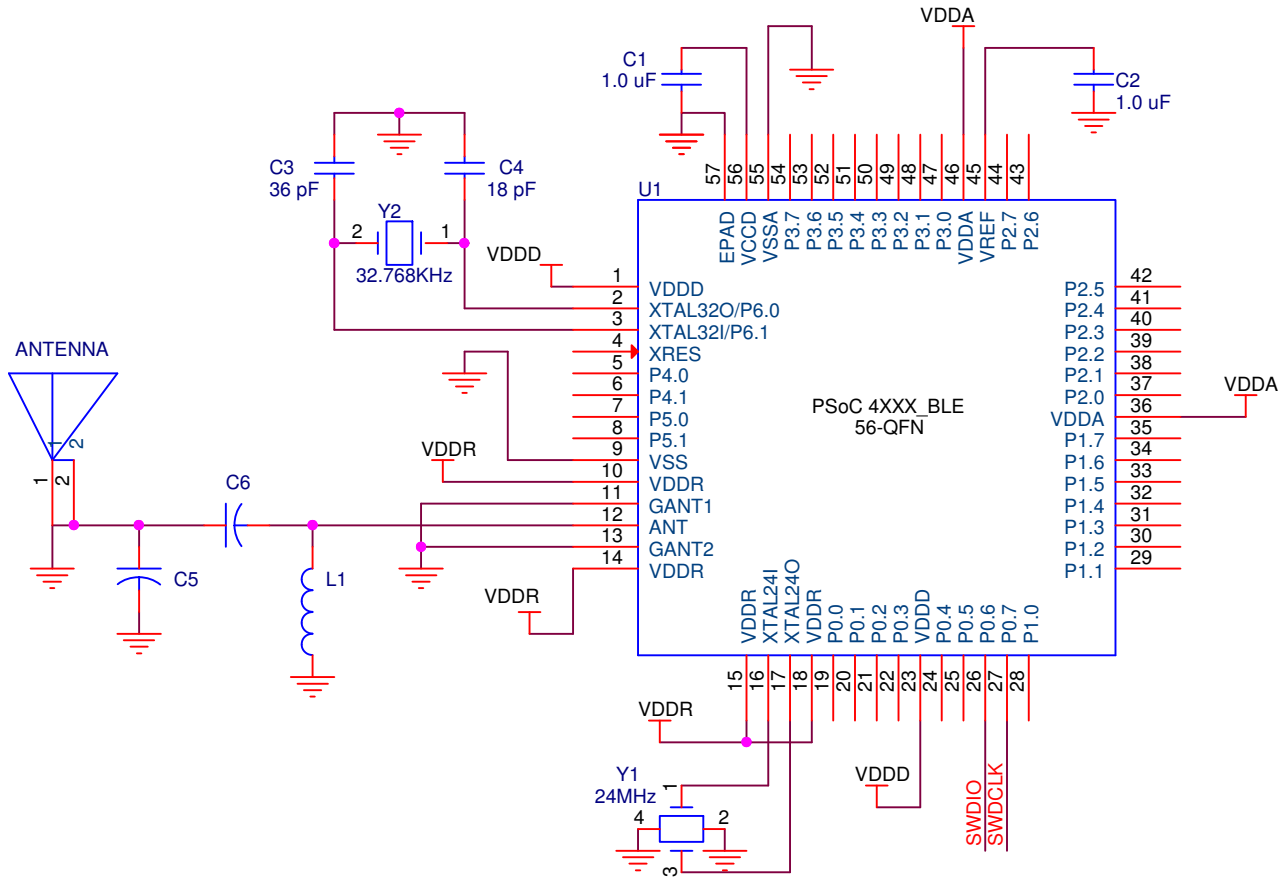
Name	Analog	Digital (HSIOM_PORT_SELx.SELy) ('x' denotes port number and 'y' denotes pin number)					
		0	8	9	10	14	15
		GPIO	Active #0	Active #1	Active #2	Deep-Sleep #0	Deep-Sleep #1
P0.0	COMP0_INP	GPIO	TCPWM0_P[3]	SCB1_UART_RX[1]		SCB1_I2C_SDA[1]	SCB1_SPI_MOSI[1]
P0.1	COMP0_INN	GPIO	TCPWM0_N[3]	SCB1_UART_TX[1]		SCB1_I2C_SCL[1]	SCB1_SPI_MISO[1]
P0.2		GPIO	TCPWM1_P[3]	SCB1_UART_RTS[1]		COMP0_OUT[0]	SCB1_SPI_SS0[1]
P0.3		GPIO	TCPWM1_N[3]	SCB1_UART_CTS[1]		COMP1_OUT[0]	SCB1_SPI_SCLK[1]
P0.4	COMP1_INP	GPIO	TCPWM1_P[0]	SCB0_UART_RX[1]	EXT_CLK[0]/ ECO_OUT[0]	SCB0_I2C_SDA[1]	SCB0_SPI_MOSI[1]
P0.5	COMP1_INN	GPIO	TCPWM1_N[0]	SCB0_UART_TX[1]		SCB0_I2C_SCL[1]	SCB0_SPI_MISO[1]
P0.6		GPIO	TCPWM2_P[0]	SCB0_UART_RTS[1]		SWDIO[0]	SCB0_SPI_SS0[1]
P0.7		GPIO	TCPWM2_N[0]	SCB0_UART_CTS[1]		SWDCLK[0]	SCB0_SPI_SCLK[1]
P1.0	CTBm1_OA0_INP	GPIO	TCPWM0_P[1]			COMP0_OUT[1]	WCO_OUT[2]
P1.1	CTBm1_OA0_INN	GPIO	TCPWM0_N[1]			COMP1_OUT[1]	SCB1_SPI_SS1
P1.2	CTBm1_OA0_OUT	GPIO	TCPWM1_P[1]				SCB1_SPI_SS2
P1.3	CTBm1_OA1_OUT	GPIO	TCPWM1_N[1]				SCB1_SPI_SS3

Table 4. Port Pin Connections *(continued)*

Name	Analog	Digital (HSIOM_PORT_SELx.SELy) ('x' denotes port number and 'y' denotes pin number)					
		0	8	9	10	14	15
		GPIO	Active #0	Active #1	Active #2	Deep-Sleep #0	Deep-Sleep #1
P1.4	CTBm1_OA1_INN	GPIO	TCPWM2_P[1]	SCB0_UART_RX[0]		SCB0_I2C_SDA[0]	SCB0_SPI_MOSI[1]
P1.5	CTBm1_OA1_INP	GPIO	TCPWM2_N[1]	SCB0_UART_TX[0]		SCB0_I2C_SCL[0]	SCB0_SPI_MISO[1]
P1.6	CTBm1_OA0_INP	GPIO	TCPWM3_P[1]	SCB0_UART_RTS[0]			SCB0_SPI_SS0[1]
P1.7	CTBm1_OA1_INP	GPIO	TCPWM3_N[1]	SCB0_UART_CTS[0]			SCB0_SPI_SCLK[1]
P2.0	CTBm0_OA0_INP	GPIO					SCB0_SPI_SS1
P2.1	CTBm0_OA0_INN	GPIO					SCB0_SPI_SS2
P2.2	CTBm0_OA0_OUT	GPIO				WAKEUP	SCB0_SPI_SS3
P2.3	CTBm0_OA1_OUT	GPIO					WCO_OUT[1]
P2.4	CTBm0_OA1_INN	GPIO					
P2.5	CTBm0_OA1_INP	GPIO					
P2.6	CTBm0_OA0_INP	GPIO					
P2.7	CTBm0_OA1_INP	GPIO			EXT_CLK[1]/ECO_OUT[1]		
P3.0	SARMUX_0	GPIO	TCPWM0_P[2]	SCB0_UART_RX[2]		SCB0_I2C_SDA[2]	
P3.1	SARMUX_1	GPIO	TCPWM0_N[2]	SCB0_UART_TX[2]		SCB0_I2C_SCL[2]	
P3.2	SARMUX_2	GPIO	TCPWM1_P[2]	SCB0_UART_RTS[2]			
P3.3	SARMUX_3	GPIO	TCPWM1_N[2]	SCB0_UART_CTS[2]			
P3.4	SARMUX_4	GPIO	TCPWM2_P[2]	SCB1_UART_RX[2]		SCB1_I2C_SDA[2]	
P3.5	SARMUX_5	GPIO	TCPWM2_N[2]	SCB1_UART_TX[2]		SCB1_I2C_SCL[2]	
P3.6	SARMUX_6	GPIO	TCPWM3_P[2]	SCB1_UART_RTS[2]			
P3.7	SARMUX_7	GPIO	TCPWM3_N[2]	SCB1_UART_CTS[2]			WCO_OUT[0]
P4.0	CMOD	GPIO	TCPWM0_P[0]	SCB1_UART_RTS[0]			SCB1_SPI_MOSI[0]
P4.1	CTANK	GPIO	TCPWM0_N[0]	SCB1_UART_CTS[0]			SCB1_SPI_MISO[0]
P5.0		GPIO	TCPWM3_P[0]	SCB1_UART_RX[0]	EXTPA_EN	SCB1_I2C_SDA[0]	SCB1_SPI_SS0[0]
P5.1		GPIO	TCPWM3_N[0]	SCB1_UART_TX[0]	EXT_CLK[2]/ECO_OUT[2]	SCB1_I2C_SCL[0]	SCB1_SPI_SCLK[0]
P6.0_XTAL32O		GPIO					
P6.1_XTAL32I		GPIO					

The possible pin connections are shown for all analog and digital peripherals (except the radio, LCD, and CSD blocks, which were shown in Table 1). A typical system application connection diagram is shown in Figure 5.

Figure 5. System Application Connection Diagram



Power

The PSoC 4100_BLE device can be supplied from batteries with a voltage range of 1.9 V to 5.5 V by directly connecting to the digital supply (VDDD), analog supply (VDDA), and radio supply (VDDR) pins. Internal LDOs in the device regulate the supply voltage to the required levels for different blocks. The device has one regulator for the digital circuitry and separate regulators for radio circuitry for noise isolation. Analog circuits run directly from the analog supply (VDDA) input. The device uses separate regulators for Deep-Sleep and Hibernate (lowered power supply and retention) modes to minimize the power consumption. The radio stops working below 1.9 V, but the device continues to function down to 1.71 V without RF. Note that VDDR must be supplied whenever VDDD is supplied.

Bypass capacitors must be used from VDDx (x = A, D, or R) to ground. The typical practice for systems in this frequency range is to use a capacitor in the 1-µF range in parallel with a smaller capacitor (for example, 0.1 µF). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

Power Supply	Bypass Capacitors
VDDD	0.1-µF ceramic at each pin plus bulk capacitor 1 µF to 10 µF.
VDDA	0.1-µF ceramic at each pin plus bulk capacitor 1 µF to 10 µF.
VDDR	0.1-µF ceramic at each pin plus bulk capacitor 1 µF to 10 µF.
VCCD	1-µF ceramic capacitor at the VCCD pin.
VREF (optional)	The internal bandgap may be bypassed with a 1-µF to 10-µF capacitor.

Development Support

The PSoC 4100_BLE family has a rich set of documentation, development tools, and online resources to assist you during your development process. Visit www.cypress.com/go/psoc4 to find out more.

Documentation

A suite of documentation supports the PSoC 4100_BLE family to ensure that you can find answers to your questions quickly. This section contains a list of some of the key documents.

Software User Guide: A step-by-step guide for using PSoC Creator. The software user guide shows you how the PSoC Creator build process works in detail, how to use source control with PSoC Creator, and much more.

Component Datasheets: The flexibility of PSoC allows the creation of new peripherals (Components) long after the device has gone into production. Component datasheets provide all of the information needed to select and use a particular Component, including a functional description, API documentation, example code, and AC/DC specifications.

Application Notes: PSoC application notes discuss a particular application of PSoC in depth; examples include creating standard and custom BLE profiles. Application notes often include example projects in addition to the application note document.

Technical Reference Manual: The Technical Reference Manual (TRM) contains all the technical detail you need to use a PSoC device, including a complete description of all PSoC registers. The TRM is available in the Documentation section at www.cypress.com/psoc4.

Online

In addition to print documentation, the Cypress PSoC forums connect you with fellow PSoC users and experts in PSoC from around the world, 24 hours a day, 7 days a week.

Tools

With industry standard cores, programming, and debugging interfaces, the PSoC 4100_BLE family is part of a development tool ecosystem. Visit us at www.cypress.com/go/psoccreator for the latest information on the revolutionary, easy to use PSoC Creator IDE, supported third party compilers, programmers, debuggers, and development kits.

Table 6. DC Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID19	I_{DD9}	Execute from flash; CPU at 24 MHz	–	7.1	–	mA	T = 25 °C, V_{DD} = 3.3 V
SID20	I_{DD10}	Execute from flash; CPU at 24 MHz	–	–	–	mA	T = –40 °C to 105 °C
SID21	I_{DD11}	Execute from flash; CPU at 48 MHz	–	13.4	–	mA	T = 25 °C, V_{DD} = 3.3 V
SID22	I_{DD12}	Execute from flash; CPU at 48 MHz	–	–	–	mA	T = –40 °C to 105 °C
Sleep Mode, V_{DD} = 1.8 V to 5.5 V							
SID23	I_{DD13}	IMO on	–	–	–	mA	T = 25 °C, VDD = 3.3 V, SYSCLK = 3 MHz
Sleep Mode, V_{DD} and V_{DDR} = 1.9 V to 5.5 V							
SID24	I_{DD14}	ECO on	–	–	–	mA	T = 25 °C, VDD = 3.3 V, SYSCLK = 3 MHz
Deep-Sleep Mode, V_{DD} = 1.8 V to 3.6 V							
SID25	I_{DD15}	WDT with WCO on	–	1.3	–	µA	T = 25 °C, V_{DD} = 3.3 V
SID26	I_{DD16}	WDT with WCO on	–	–	–	µA	T = –40 °C to 105 °C
Deep-Sleep Mode, V_{DD} = 3.6 V to 5.5 V							
SID27	I_{DD17}	WDT with WCO on	–	–	–	µA	T = 25 °C, V_{DD} = 5 V
SID28	I_{DD18}	WDT with WCO on	–	–	–	µA	T = –40 °C to 105 °C
Deep-Sleep Mode, V_{DD} = 1.71 V to 1.89 V (Regulator Bypassed)							
SID29	I_{DD19}	WDT with WCO on	–	–	–	µA	T = 25 °C
SID30	I_{DD20}	WDT with WCO on	–	–	–	µA	T = –40 °C to 105 °C
Deep-Sleep Mode, V_{DD} = 2.5 V to 3.6 V							
SID31	I_{DD21}	Opamp on	–	–	–	µA	T = 25 °C, V_{DD} = 3.3 V
SID32	I_{DD22}	Opamp on	–	–	–	µA	T = –40 °C to 105 °C
Deep-Sleep Mode, V_{DD} = 3.6 V to 5.5 V							
SID33	I_{DD23}	Opamp on	–	–	–	µA	T = 25 °C, V_{DD} = 5 V
SID34	I_{DD24}	Opamp on	–	–	–	µA	T = –40 °C to 105 °C
Hibernate Mode, V_{DD} = 1.8 V to 3.6 V							
SID37	I_{DD27}	GPIO and reset active	–	150	–	nA	T = 25 °C, V_{DD} = 3.3 V
SID38	I_{DD28}	GPIO and reset active	–	–	–	nA	T = –40 °C to 105 °C
Hibernate Mode, V_{DD} = 3.6 V to 5.5 V							
SID39	I_{DD29}	GPIO and reset active	–	–	–	nA	T = 25 °C, V_{DD} = 5 V
SID40	I_{DD30}	GPIO and reset active	–	–	–	nA	T = –40 °C to 105 °C
Hibernate Mode, V_{DD} = 1.71 V to 1.89 V (Regulator Bypassed)							
SID41	I_{DD31}	GPIO and reset active	–	–	–	nA	T = 25 °C
SID42	I_{DD32}	GPIO and reset active	–	–	–	nA	T = –40 °C to 105 °C

Table 6. DC Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
Stop Mode, V_{DD} = 1.8 V to 3.6 V							
SID43	I_{DD33}	Stop mode current (V_{DD})	–	20	–	nA	T = 25 °C, V_{DD} = 3.3 V
SID44	I_{DD34}	Stop mode current (V_{DDR})	–	40	–-	nA	T = 25 °C, V_{DDR} = 3.3 V
SID45	I_{DD35}	Stop mode current (V_{DD})	–	–	–	nA	T = –40 °C to 105 °C
SID46	I_{DD36}	Stop mode current (V_{DDR})	–	–	–	nA	T = –40 °C to 105 °C, V_{DDR} = 1.9 V to 3.6 V
Stop Mode, V_{DD} = 3.6 V to 5.5 V							
SID47	I_{DD37}	Stop mode current (V_{DD})	–	–	–	nA	T = 25 °C, V_{DD} = 5 V
SID48	I_{DD38}	Stop mode current (V_{DDR})	–	–	–	nA	T = 25 °C, V_{DDR} = 5 V
SID49	I_{DD39}	Stop mode current (V_{DD})	–	–	–	nA	T = –40 °C to 105 °C
SID50	I_{DD40}	Stop mode current (V_{DDR})	–	–	–	nA	T = –40 °C to 105 °C
Stop Mode, V_{DD} = 1.71 V to 1.89 V (Regulator Bypassed)							
SID51	I_{DD41}	Stop mode current (V_{DD})	–	–	–	nA	T = 25 °C
SID52	I_{DD42}	Stop mode current (V_{DD})	–	–	–	nA	T = –40 °C to 105 °C

Table 7. AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID53	F_{CPU}	CPU frequency	DC	–	24	MHz	1.71 V ≤ V_{DD} ≤ 5.5 V
SID54	T_{SLEEP}	Wakeup from Sleep mode	–	0	–	µs	Guaranteed by characterization
SID55	$T_{DEEPSLEEP}$	Wakeup from Deep-Sleep mode	–	–	25	µs	24-MHz IMO. Guaranteed by characterization
SID56	$T_{HIBERNATE}$	Wakeup from Hibernate mode	–	–	2	ms	Guaranteed by characterization
SID57	T_{STOP}	Wakeup from Stop mode	–	–	2	ms	Guaranteed by characterization

XRES

Table 12. XRES DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID87	V_{IH}	Input voltage HIGH threshold	0.7 × V_{DDD}	–	–	V	CMOS input
SID88	V_{IL}	Input voltage LOW threshold	–	–	0.3 × V_{DDD}	V	CMOS input
SID89	Rpullup	Pull-up resistor	3.5	5.6	8.5	kΩ	
SID90	C_{IN}	Input capacitance	–	3	–	pF	
SID91	$V_{HYSXRES}$	Input voltage hysteresis	–	100	–	mV	
SID92	I_{DIODE}	Current through protection diode to V_{DDD}/V_{SS}	–	–	100	µA	

Table 13. XRES AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID93	$T_{RESETWIDTH}$	Reset pulse width	1	–	–	µs	

Analog Peripherals

Opamp

Table 14. Opamp Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
I_{DD} (Opamp Block Current. V_{DD} = 1.8 V. No Load)							
SID94	I_{DD_HI}	Power = high	–	1000	1300	µA	
SID95	I_{DD_MED}	Power = medium	–	500	–	µA	
SID96	I_{DD_LOW}	Power = low	–	250	350	µA	
GBW (Load = 20 pF, 0.1 mA. V_{DDA} = 2.7 V)							
SID97	GBW_HI	Power = high	6	–	–	MHz	
SID98	GBW_MED	Power = medium	4	–	–	MHz	
SID99	GBW_LO	Power = low	–	1	–	MHz	
I_{OUT_MAX} (V_{DDA} ≥ 2.7 V, 500 mV from Rail)							
SID100	$I_{OUT\_MAX\_HI}$	Power = high	10	–	–	mA	
SID101	$I_{OUT\_MAX\_MID}$	Power = medium	10	–	–	mA	
SID102	$I_{OUT\_MAX\_LO}$	Power = low	–	5	–	mA	
I_{OUT} (V_{DDA} = 1.71 V, 500 mV from Rail)							
SID103	$I_{OUT\_MAX\_HI}$	Power = high	4	–	–	mA	
SID104	$I_{OUT\_MAX\_MID}$	Power = medium	4	–	–	mA	
SID105	$I_{OUT\_MAX\_LO}$	Power = low	–	2	–	mA	
SID106	V_{IN}	Charge pump on, V_{DDA} ≥ 2.7 V	–0.05	–	V_{DDA} – 0.2	V	
SID107	V_{CM}	Charge pump on, V_{DDA} ≥ 2.7 V	–0.05	–	V_{DDA} – 0.2	V	
V_{OUT} (V_{DDA} ≥ 2.7 V)							
SID108	V_{OUT_1}	Power = high, I_{LOAD}=10 mA	0.5	–	V_{DDA} – 0.5	V	
SID109	V_{OUT_2}	Power = high, I_{LOAD}=1 mA	0.2	–	V_{DDA} – 0.2	V	
SID110	V_{OUT_3}	Power = medium, I_{LOAD}=1 mA	0.2	–	V_{DDA} – 0.2	V	
SID111	V_{OUT_4}	Power = low, I_{LOAD}=0.1 mA	0.2	–	V_{DDA} – 0.2	V	
SID112	V_{OS_TR}	Offset voltage, trimmed	1	±0.5	1	mV	High mode

Table 14. Opamp Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID113	V_{OS_TR}	Offset voltage, trimmed	–	±1	–	mV	Medium mode
SID114	V_{OS_TR}	Offset voltage, trimmed	–	±2	–	mV	Low mode
SID115	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–10	±3	10	µV/°C	High mode
SID116	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–	±10	–	µV/°C	Medium mode
SID117	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–	±10	–	µV/°C	Low mode
SID118	CMRR	DC	65	70	–	dB	V_{DDD} = 3.6 V, High-power mode
SID119	PSRR	At 1 kHz, 100-mV ripple	70	85	–	dB	V_{DDD} = 3.6 V
Noise							
SID120	V_{N1}	Input referred, 1 Hz–1 GHz, power = high	–	94	–	µVrms	
SID121	V_{N2}	Input referred, 1 kHz, power = high	–	72	–	nV/rtHz	
SID122	V_{N3}	Input referred, 10 kHz, power = high	–	28	–	nV/rtHz	
SID123	V_{N4}	Input referred, 100 kHz, power = high	–	15	–	nV/rtHz	
SID124	C_{LOAD}	Stable up to maximum load. Performance specs at 50 pF	–	–	125	pF	
SID125	Slew_rate	Cload = 50 pF, Power = High, $V_{DDA} \geq 2.7$ V	6	–	–	V/µs	
SID126	T_op_wake	From disable to enable, no external RC dominating	–	300	–	µs	
Comp_mode (Comparator Mode; 50-mV Drive, $T_{RISE} = T_{FALL}$ (Approx.)							
SID127	T_{PD1}	Response time; power = high	–	150	–	ns	
SID128	T_{PD2}	Response time; power = medium	–	400	–	ns	
SID129	T_{PD3}	Response time; power = low	–	2000	–	ns	
SID130	Vhyst_op	Hysteresis	–	10	–	mV	
Deep-Sleep Mode (Deep-Sleep mode operation is only guaranteed for V_{DDA} > 2.5 V)							
SID131	GBW_DS	Gain bandwidth product	–	50	–	kHz	
SID132	IDD_DS	Current	–	15	–	µA	
SID133	Vos_DS	Offset voltage	–	5	–	mV	
SID134	Vos_dr_DS	Offset voltage drift	–	20	–	µV/°C	
SID135	Vout_DS	Output voltage	0.2	–	V_{DD}–0.2	V	
SID136	Vcm_DS	Common mode voltage	0.2	–	V_{DD}–1.8	V	

Table 15. Comparator DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID140	$V_{OFFSET1}$	Input offset voltage, Factory trim	–	–	±10	mV	
SID141	$V_{OFFSET2}$	Input offset voltage, Custom trim	–	–	±6	mV	
SID141A	$V_{OFFSET3}$	Input offset voltage, ultra-low-power mode	–	±12	–	mV	$V_{DDD} \geq 2.6$ V for Temp < 0 °C $V_{DDD} \geq 1.8$ V for Temp ≥ 0 °C
SID142	V_{HYST}	Hysteresis when enabled	–	10	35	mV	

Counter

Table 23. Counter DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID200	I_{CTR1}	Block current consumption at 3 MHz	–	–	42	µA	16-bit timer, 85 °C
SID200A			–	–	46	µA	16-bit timer, 105 °C
SID201	I_{CTR2}	Block current consumption at 12 MHz	–	–	130	µA	16-bit timer, 85 °C
SID201A			–	–	137	µA	16-bit timer, 105 °C
SID202	I_{CTR3}	Block current consumption at 48 MHz	–	–	535	µA	16-bit timer, 85 °C
SID202A			–	–	560	µA	16-bit timer, 105 °C

Table 24. Counter AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID203	$T_{CTRFREQ}$	Operating frequency	F_{CLK}	–	48	MHz	
SID204	$T_{CTRPWINT}$	Capture pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	
SID205	$T_{CTRPWEXT}$	Capture pulse width (external)	$2 \times T_{CLK}$	–	–	ns	
SID206	T_{CTRES}	Counter Resolution	T_{CLK}	–	–	ns	
SID207	$T_{CENWIDINT}$	Enable pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	
SID208	$T_{CENWIDEXT}$	Enable pulse width (external)	$2 \times T_{CLK}$	–	–	ns	
SID209	$T_{CTRRESWINT}$	Reset pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	
SID210	$T_{CTRRESWEXT}$	Reset pulse width (external)	$2 \times T_{CLK}$	–	–	ns	

Pulse Width Modulation (PWM)

Table 25. PWM DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID211	I_{PWM1}	Block current consumption at 3 MHz	–	–	42	µA	16-bit timer, 85 °C
SID211A			–	–	46	µA	16-bit timer, 105 °C
SID212	I_{PWM2}	Block current consumption at 12 MHz	–	–	130	µA	16-bit timer, 85 °C
SID212A			–	–	137	µA	16-bit timer, 105 °C
SID213	I_{PWM3}	Block current consumption at 48 MHz	–	–	535	µA	16-bit timer, 85 °C
SID213A			–	–	560	µA	16-bit timer, 105 °C

Table 26. PWM AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID214	$T_{PWMFREQ}$	Operating frequency	F_{CLK}	–	48	MHz	
SID215	$T_{PWMPWINT}$	Pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	
SID216	T_{PWMEXT}	Pulse width (external)	$2 \times T_{CLK}$	–	–	ns	
SID217	$T_{PWMKILLINT}$	Kill pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	
SID218	$T_{PWMKILLEXT}$	Kill pulse width (external)	$2 \times T_{CLK}$	–	–	ns	
SID219	$T_{PWMEINT}$	Enable pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	
SID220	$T_{PWMENEXT}$	Enable pulse width (external)	$2 \times T_{CLK}$	–	–	ns	
SID221	$T_{PWMRESWINT}$	Reset pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	
SID222	$T_{PWMRESWEXT}$	Reset pulse width (external)	$2 \times T_{CLK}$	–	–	ns	

SPI Specifications

Table 33. Fixed SPI DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID237	I_{SPI1}	Block current consumption at 1 Mbps	–	–	360	µA	
SID238	I_{SPI2}	Block current consumption at 4 Mbps	–	–	560	µA	
SID239	I_{SPI3}	Block current consumption at 8 Mbps	–	–	600	µA	

Table 34. Fixed SPI AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID240	F_{SPI}	SPI operating frequency (master; 6x oversampling)	–	–	8	MHz	

Table 35. Fixed SPI Master Mode AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID241	T_{DMO}	MOSI valid after Sclock driving edge	–	–	18	ns	
SID242	T_{DSI}	MISO valid before Sclock capturing edge. Full clock, late MISO sampling used	20	–	–	ns	Full clock, late MISO sampling
SID243	T_{HMO}	Previous MOSI data hold time	0	–	–	ns	Referred to Slave capturing edge

Table 36. Fixed SPI Slave Mode AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID244	T_{DMI}	MOSI valid before Sclock capturing edge	40	–	–	ns	
SID245	T_{DSO}	MISO valid after Sclock driving edge	–	–	42 + 3 × T_{SCB}	ns	
SID246	T_{DSO_ext}	MISO valid after Sclock driving edge in external clock mode	–	–	50	ns	V_{DD} < 3.0 V
SID247	T_{HSO}	Previous MISO data hold time	0	–	–	ns	
SID248	$T_{SSELSCK}$	SSEL valid to first SCK valid edge	100	–	–	ns	

Memory

Table 37. Flash DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID249	V_{PE}	Erase and program voltage	1.71	–	5.5	V	
SID310	T_{WS32}	Number of Wait states at 16–24 MHz	1	–	–		CPU execution from flash
SID311	T_{WS16}	Number of Wait states for 0–16 MHz	0	–	–		CPU execution from flash

Table 38. Flash AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID250	$T_{ROWWRITE}$[4]	Row (block) write time (erase and program)	–	–	20	ms	Row (block) = 128 bytes
SID251	$T_{ROWERASE}$[4]	Row erase time	–	–	13	ms	Row (block) = 128 bytes for 128-KB flash devices Row (block) = 256 bytes for 256-KB flash devices
SID252	$T_{ROWPROGRAM}$[4]	Row program time after erase	–	–	7	ms	
SID253	$T_{BULKERASE}$[4]	Bulk erase time (128 KB)	–	–	35	ms	
SID254	$T_{DEVPROG}$[4]	Total device program time	–	–	25	seconds	
SID255	F_{END}	Flash endurance	100 K	–	–	cycles	
SID256	F_{RET}	Flash retention. $T_A \leq 55$ °C, 100 K P/E cycles	20	–	–	years	
SID257	F_{RET2}	Flash retention. $T_A \leq 85$ °C, 10 K P/E cycles	10	–	–	years	
SID257A	F_{RET3}	Flash retention. $T_A \leq 105$ °C, 10 K P/E cycles	3	–	–	years	For $T_A \geq 85$ °C

System Resources

Power-on-Reset (POR)

Table 39. POR DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID258	$V_{RISEIPOR}$	Rising trip voltage	0.80	–	1.45	V	
SID259	$V_{FALLIPOR}$	Falling trip voltage	0.75	–	1.40	V	
SID260	$V_{IPORHYST}$	Hysteresis	15	–	200	mV	

Table 40. POR AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID264	T_{PPOR_TR}	PPOR response time in Active and Sleep modes	–	–	1	µs	

Note
4. It can take as much as 20 milliseconds to write to flash. During this time, the device should not be reset, or flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.

SWD Interface

Table 45. SWD Interface Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID283	F_SWDCLK1	3.3 V ≤ V_{DD} ≤ 5.5 V	–	–	14	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID284	F_SWDCLK2	1.71 V ≤ V_{DD} ≤ 3.3 V	–	–	7	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID285	T_SWDI_SETUP	T = 1/f SWDCLK	0.25 × T	–	–	ns	
SID286	T_SWDI_HOLD	T = 1/f SWDCLK	0.25 × T	–	–	ns	
SID287	T_SWDO_VALID	T = 1/f SWDCLK	–	–	0.5 × T	ns	
SID288	T_SWDO_HOLD	T = 1/f SWDCLK	1	–	–	ns	

Internal Main Oscillator

Table 46. IMO DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID289	I_{IMO1}	IMO operating current at 48 MHz	–	–	1000	µA	
SID290	I_{IMO2}	IMO operating current at 24 MHz	–	–	325	µA	
SID291	I_{IMO3}	IMO operating current at 12 MHz	–	–	225	µA	
SID292	I_{IMO4}	IMO operating current at 6 MHz	–	–	180	µA	
SID293	I_{IMO5}	IMO operating current at 3 MHz	–	–	150	µA	

Table 47. IMO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID296	$F_{IMOTOL3}$	Frequency variation from 3 to 48 MHz	–	–	±2	%	With API-called calibration
SID297	$F_{IMOTOL3}$	IMO startup time	–	–	12	µs	

Internal Low-Speed Oscillator

Table 48. ILO DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID298	I_{ILO2}	ILO operating current at 32 kHz	–	0.3	1.05	µA	Guaranteed by design

Table 49. ILO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID299	$T_{STARTILO1}$	ILO startup time	–	–	2	ms	
SID300	$F_{ILOTRIM1}$	32-kHz trimmed frequency	15	32	50	kHz	

Table 52. BLE Subsystem *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID365	FTX, ACC	Frequency accuracy	–150	–	150	kHz	RF-PHY Specification (TRM-LE/CA/06/C)
SID366	FTX, MAXDR	Maximum frequency drift	–50	–	50	kHz	RF-PHY Specification (TRM-LE/CA/06/C)
SID367	FTX, INITDR	Initial frequency drift	–20	–	20	kHz	RF-PHY Specification (TRM-LE/CA/06/C)
SID368	FTX, DR	Maximum drift rate	–20	–	20	kHz/ 50 µs	RF-PHY Specification (TRM-LE/CA/06/C)
SID369	IBSE1	In-band spurious emission at 2-MHz offset	–	–	–20	dBm	RF-PHY Specification (TRM-LE/CA/03/C)
SID370	IBSE2	In-band spurious emission at ≥3-MHz offset	–	–	-30	dBm	RF-PHY Specification (TRM-LE/CA/03/C)
SID371	TXSE1	Transmitter spurious emissions (average), <1.0 GHz	–	–	-55.5	dBm	FCC-15.247
SID372	TXSE2	Transmitter spurious emissions (average), >1.0 GHz	–	–	-41.5	dBm	FCC-15.247
RF Current Specifications							
SID373	IRX	Receive current in normal mode	–	18.7	–	mA	
SID373A	IRX_RF	Radio receive current in normal mode	–	16.4	–	mA	Measured at V_{DDR}
SID374	IRX, HIGHGAIN	Receive current in high-gain mode	–	21.5	–	mA	
SID375	ITX, 3dBm	TX current at 3-dBm setting (PA10)	–	20	–	mA	
SID376	ITX, 0dBm	TX current at 0-dBm setting (PA7)	–	16.5	–	mA	
SID376A	ITX_RF, 0dBm	Radio TX current at 0 dBm setting (PA7)	–	15.6	–	mA	Measured at V_{DDR}
SID376B	ITX_RF, 0dBm	Radio TX current at 0 dBm excluding Balun loss	–	14.2	–	mA	Guaranteed by design simulation
SID377	ITX,-3dBm	TX current at –3-dBm setting (PA4)	–	15.5	–	mA	
SID378	ITX,-6dBm	TX current at –6-dBm setting (PA3)	–	14.5	–	mA	
SID379	ITX,-12dBm	TX current at –12-dBm setting (PA2)	–	13.2	–	mA	
SID380	ITX,-18dBm	TX current at –18-dBm setting (PA1)	–	12.5	–	mA	
SID380A	Iavg_1sec, 0dBm	Average current at 1-second BLE connection interval	–	17.1	–	µA	TXP: 0 dBm; ±20-ppm master and slave clock accuracy.
SID380B	Iavg_4sec, 0dBm	Average current at 4-second BLE connection interval	–	6.1	–	µA	TXP: 0 dBm; ±20-ppm master and slave clock accuracy.
General RF Specifications							
SID381	FREQ	RF operating frequency	2400	–	2482	MHz	
SID382	CHBW	Channel spacing	–	2	–	MHz	
SID383	DR	On-air data rate	–	1000	–	kbps	
SID384	IDLE2TX	BLE.IDLE to BLE. TX transition time	–	120	140	µs	
SID385	IDLE2RX	BLE.IDLE to BLE. RX transition time	–	75	120	µs	

Table 52. BLE Subsystem *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
RSSI Specifications							
SID386	RSSI, ACC	RSSI accuracy	–	±5	–	dB	
SID387	RSSI, RES	RSSI resolution	–	1	–	dB	
SID388	RSSI, PER	RSSI sample period	–	6	–	µs	

Table 53. ECO Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID389	F_{ECO}	Crystal frequency	–	24	–	MHz	
SID390	F_{TOL}	Frequency tolerance	–50	–	50	ppm	
SID391	ESR	Equivalent series resistance	–	–	60	Ω	
SID392	PD	Drive level	–	–	100	µW	
SID393	T_{START1}	Startup time (Fast Charge on)	–	–	850	µs	
SID394	T_{START2}	Startup time (Fast Charge off)	–	–	3	ms	
SID395	C_L	Load capacitance	–	8	–	pF	
SID396	C0	Shunt capacitance	–	1.1	–	pF	
SID397	I_{ECO}	Operating current	–	1400	–	µA	Includes LDO+BG current

Table 54. WCO Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID398	F_{WCO}	Crystal frequency	–	32.768	–	kHz	
SID399	FTOL	Frequency tolerance	–	50	–	ppm	
SID400	ESR	Equivalent series resistance	–	50	–	kΩ	
SID401	PD	Drive level	–	–	1	µW	
SID402	T_{START}	Startup time	–	–	500	ms	
SID403	C_L	Crystal load capacitance	6	–	12.5	pF	
SID404	C0	Crystal shunt capacitance	–	1.35	–	pF	
SID405	I_{WCO1}	Operating current (High-Power mode)	–	–	8	µA	
SID406	I_{WCO2}	Operating current (low-power mode)	–	–	1	µA	85 °C
SID406A			–	–	2.6	µA	105 °C

Packaging

Table 55. Package Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
T_A	Operating ambient temperature	–	–40	25.00	105	°C
T_J	Operating junction temperature	–	–40	–	125	°C
T_{JA}	Package θ_{JA} (56-pin QFN)	–	–	16.9	–	°C/watt
T_{JC}	Package θ_{JC} (56-pin QFN)	–	–	9.7	–	°C/watt
T_{JA}	Package θ_{JA} (76-ball WLCSP)	–	–	20.1	–	°C/watt
T_{JC}	Package θ_{JC} (76-ball WLCSP)	–	–	0.19	–	°C/watt
T_{JA}	Package θ_{JA} (76-ball Thin WLCSP)	–	–	20.9	–	°C/watt
T_{JC}	Package θ_{JC} (76-ball Thin WLCSP)	–	–	0.17	–	°C/watt
T_{JA}	Package θ_{JA} (68-ball WLCSP)		–	16.6	–	°C/watt
T_{JC}	Package θ_{JC} (68-ball WLCSP)		–	0.19	–	°C/watt
T_{JA}	Package θ_{JA} (68-ball Thin WLCSP)		–	16.6	–	°C/watt
T_{JC}	Package θ_{JC} (68-ball Thin WLCSP)		–	0.19	–	°C/watt

Table 56. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time at Peak Temperature
All packages	260 °C	30 seconds

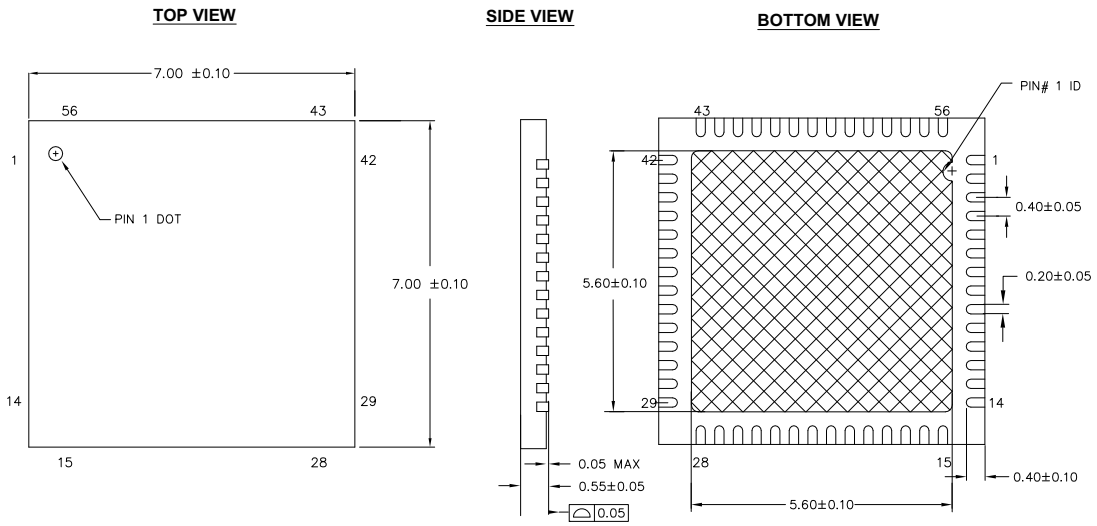
Table 57. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Package	MSL
56-pin QFN	MSL 3
All WLCSP packages	MSL 1

Table 58. Package Details

Spec ID	Package	Description
001-58740 Rev. *C	56-pin QFN	7.0 mm × 7.0 mm × 0.6 mm
001-96603 Rev. *A	76-ball WLCSP	4.04 mm × 3.87 mm × 0.55 mm
002-10658, Rev. **	76-ball thin WLCSP	4.04 mm × 3.87 mm × 0.4 mm
001-92343 Rev. *A	68-ball WLCSP	3.52 mm × 3.91 mm × 0.55 mm
001-99408 Rev **	68-ball Thin WLCSP	52 mm × 3.91 mm × 0.4 mm

Figure 6. 56-Pin QFN 7 mm × 7 mm × 0.6 mm



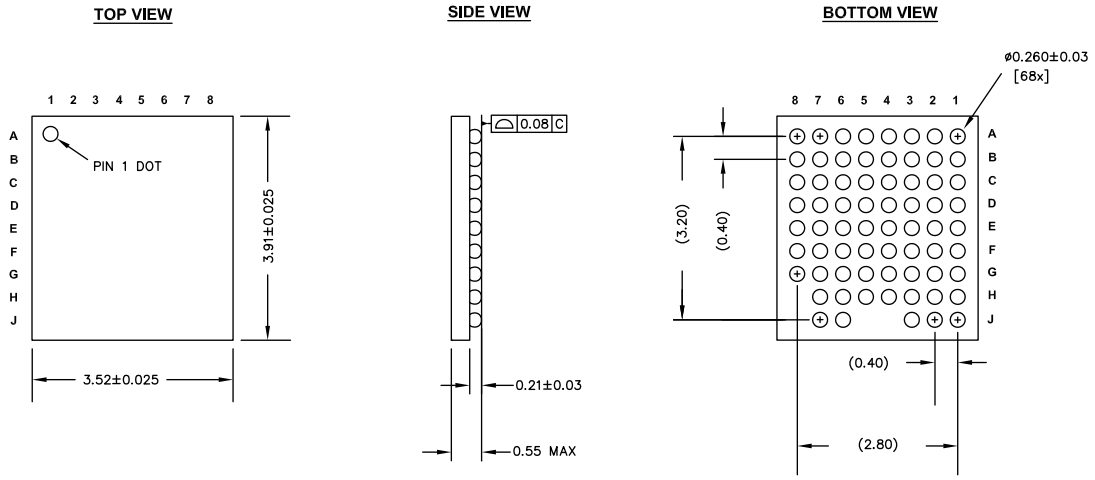
NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. BASED ON REF JEDEC # MO-248
3. ALL DIMENSIONS ARE IN MILLIMETERS

001-58740 *C

The center pad on the QFN package must be connected to ground (V_{SS}) for the proper operation of the device.

Figure 8. 68-Ball WLCSP Package Outline

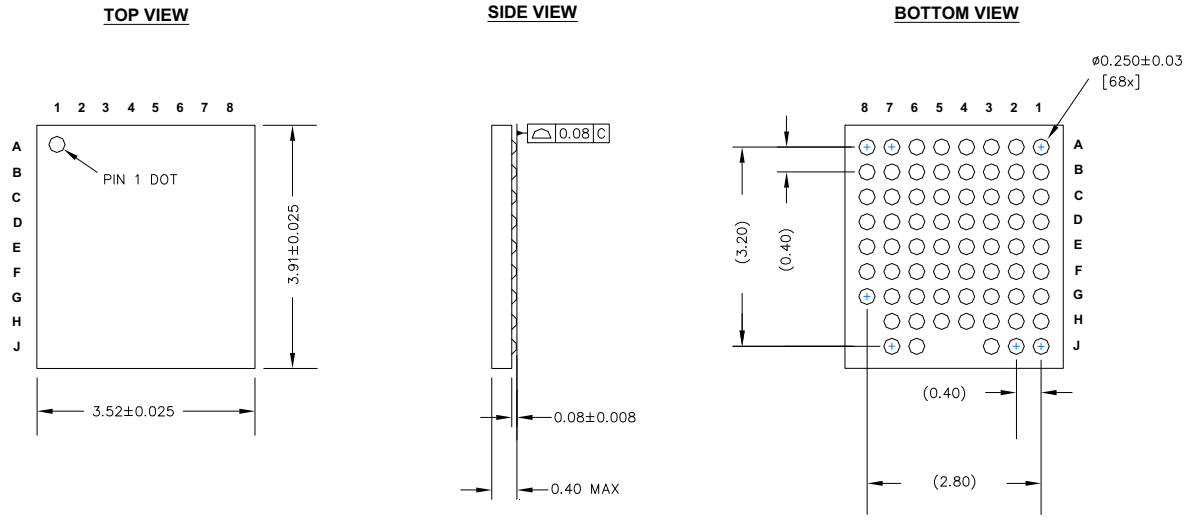


NOTES:

1. REFERENCE JEDEC PUBLICATION 95, DESIGN GUIDE 4.18
2. ALL DIMENSIONS ARE IN MILLIMETERS

001-92343 *A

Figure 9. 68-Ball Thin WLCSP

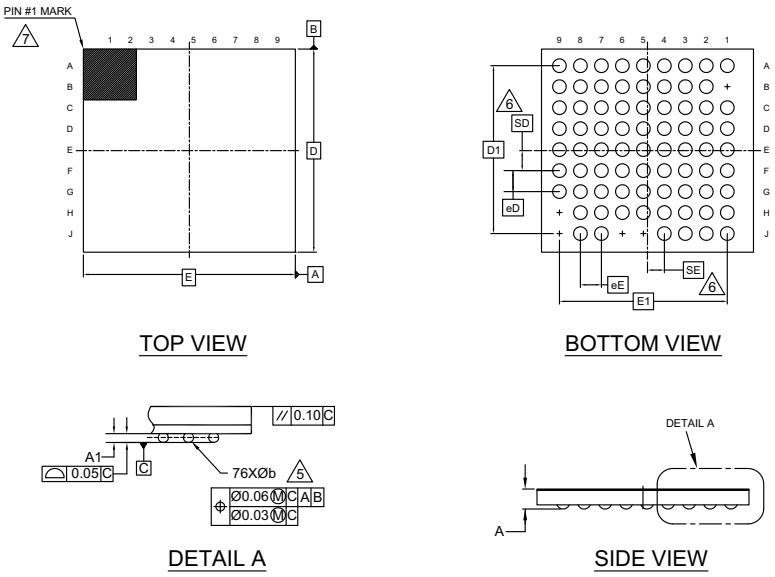


NOTES:

1. REFERENCE JEDEC PUBLICATION 95, DESIGN GUIDE 4.18
2. ALL DIMENSIONS ARE IN MILLIMETERS

001-99408 **

Figure 10. 76-Ball WLCSP Package Outline



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	0.55
A1	0.18	0.21	0.24
D	3.87 BSC		
E	4.04 BSC		
D1	3.20 BSC		
E1	3.20 BSC		
MD	9		
ME	9		
N	76		
Ø b	0.23	0.26	0.29
eD	0.40 BSC		
eE	0.40 BSC		
SD	0.381 BSC		
SE	0.321 BSC		

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
3. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
4. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
6. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
7. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.
9. JEDEC SPECIFICATION NO. REF : N/A

001-96603 *B

Document Conventions

Units of Measure

Table 60. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
dB	decibel
dBm	decibel-milliwatts
fF	femtofarads
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
Khr	kilohour
kHz	kilohertz
kΩ	kilo ohm
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
µA	microampere
µF	microfarad
µH	microhenry
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
sqrtHz	square root of hertz
V	volt