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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Not For New Designs
Core Processor	ST7
Core Size	8-Bit
Speed	8MHz
Connectivity	CANbus, I ² C, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	48
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3.8V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st72f521ar6t6

4 FLASH PROGRAM MEMORY

4.1 Introduction

The ST7 dual voltage High Density Flash (HDFlash) is a non-volatile memory that can be electrically erased as a single block or by individual sectors and programmed on a Byte-by-Byte basis using an external V_{PP} supply.

The HDFlash devices can be programmed and erased off-board (plugged in a programming tool) or on-board using ICP (In-Circuit Programming) or IAP (In-Application Programming).

The array matrix organisation allows each sector to be erased and reprogrammed without affecting other sectors.

4.2 Main Features

- Three Flash programming modes:
 - Insertion in a programming tool. In this mode, all sectors including option bytes can be programmed or erased.
 - ICP (In-Circuit Programming). In this mode, all sectors including option bytes can be programmed or erased without removing the device from the application board.
 - IAP (In-Application Programming). In this mode, all sectors except Sector 0, can be programmed or erased without removing the device from the application board and while the application is running.
- ICT (In-Circuit Testing) for downloading and executing user application test patterns in RAM
- Read-out protection
- Register Access Security System (RASS) to prevent accidental programming or erasing

4.3 Structure

The Flash memory is organised in sectors and can be used for both code and data storage.

Depending on the overall Flash memory size in the microcontroller device, there are up to three user

sectors (see Table 3). Each of these sectors can be erased independently to avoid unnecessary erasing of the whole Flash memory when only a partial erasing is required.

The first two sectors have a fixed size of 4 Kbytes (see Figure 5). They are mapped in the upper part of the ST7 addressing space so the reset and interrupt vectors are located in Sector 0 (F000h-FFFFh).

Table 3. Sectors available in Flash devices

Flash Size (bytes)	Available Sectors
4K	Sector 0
8K	Sectors 0,1
> 8K	Sectors 0,1, 2

4.3.1 Read-out Protection

Read-out protection, when selected, provides a protection against Program Memory content extraction and against write access to Flash memory. Even if no protection can be considered as totally unbreakable, the feature provides a very high level of protection for a general purpose microcontroller.

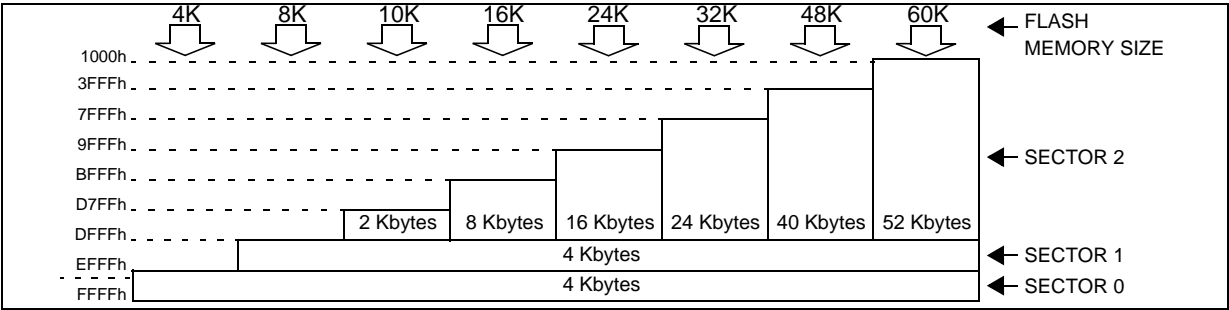
In flash devices, this protection is removed by reprogramming the option. In this case, the entire program memory is first automatically erased and the device can be reprogrammed.

Read-out protection selection depends on the device type:

- In Flash devices it is enabled and removed through the FMP_R bit in the option byte.
- In ROM devices it is enabled by mask option specified in the Option List.

Note: In flash devices, the LVD is not supported if read-out protection is enabled.

Figure 5. Memory Map and Sector Address



WATCHDOG TIMER (Cont'd)

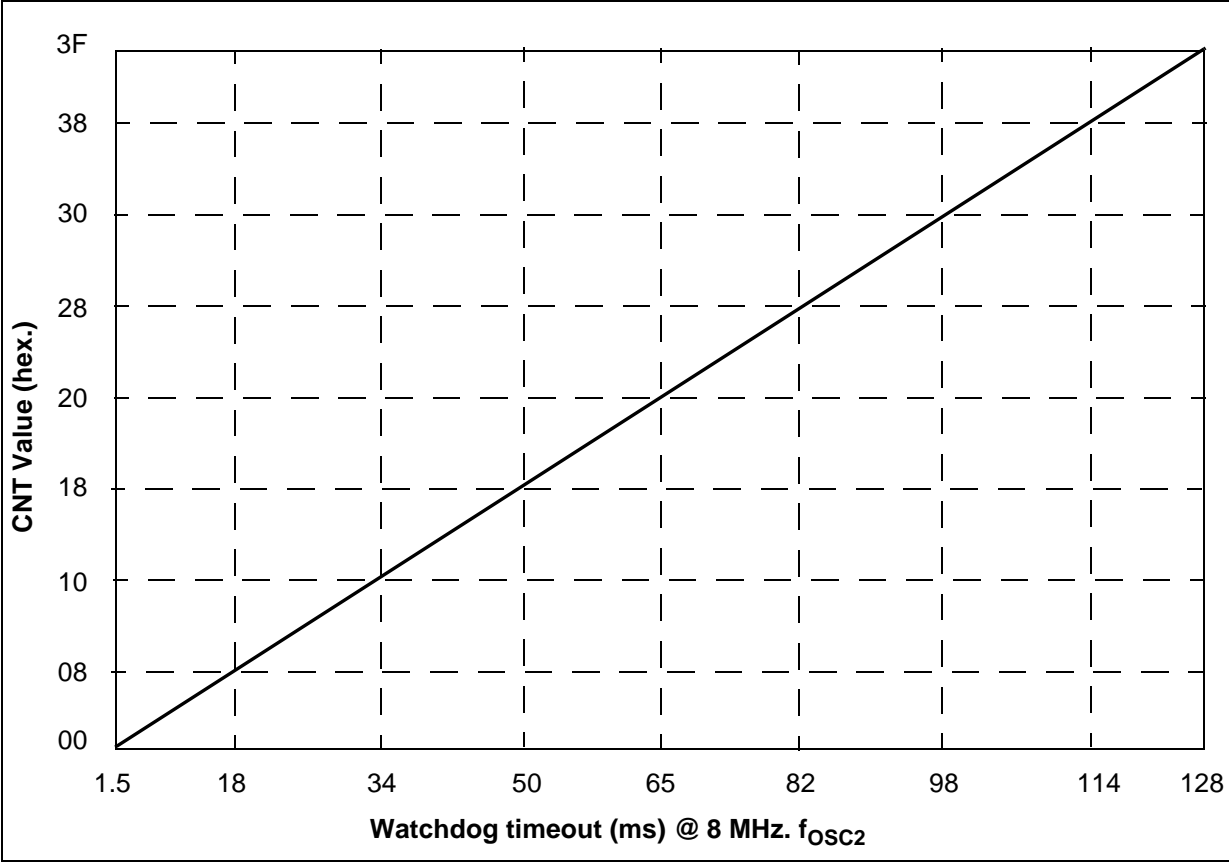
10.1.4 How to Program the Watchdog Timeout

Figure 33 shows the linear relationship between the 6-bit value to be loaded in the Watchdog Counter (CNT) and the resulting timeout duration in milliseconds. This can be used for a quick calculation without taking the timing variations into account. If

more precision is needed, use the formulae in Figure 34.

Caution: When writing to the WDGCR register, always write 1 in the T6 bit to avoid generating an immediate reset.

Figure 33. Approximate Timeout Duration



WATCHDOG TIMER (Cont'd)**Figure 34. Exact Timeout Duration (t_{\min} and t_{\max})****WHERE:**

$$t_{\min 0} = (\text{LSB} + 128) \times 64 \times t_{\text{OSC2}}$$

$$t_{\max 0} = 16384 \times t_{\text{OSC2}}$$

$$t_{\text{OSC2}} = 125\text{ns if } f_{\text{OSC2}} = 8\text{ MHz}$$

CNT = Value of T[5:0] bits in the WDGCR register (6 bits)

MSB and LSB are values from the table below depending on the timebase selected by the TB[1:0] bits in the MCCR register

TB1 Bit (MCCR Reg.)	TB0 Bit (MCCR Reg.)	Selected MCCR Timebase	MSB	LSB
0	0	2ms	4	59
0	1	4ms	8	53
1	0	10ms	20	35
1	1	25ms	49	54

To calculate the minimum Watchdog Timeout (t_{\min}):

$$\text{IF } \text{CNT} < \left\lceil \frac{\text{MSB}}{4} \right\rceil \quad \text{THEN} \quad t_{\min} = t_{\min 0} + 16384 \times \text{CNT} \times t_{\text{osc2}}$$

$$\text{ELSE} \quad t_{\min} = t_{\min 0} + \left[16384 \times \left(\text{CNT} - \left\lceil \frac{4\text{CNT}}{\text{MSB}} \right\rceil \right) + (192 + \text{LSB}) \times 64 \times \left\lceil \frac{4\text{CNT}}{\text{MSB}} \right\rceil \right] \times t_{\text{osc2}}$$

To calculate the maximum Watchdog Timeout (t_{\max}):

$$\text{IF } \text{CNT} \leq \left\lceil \frac{\text{MSB}}{4} \right\rceil \quad \text{THEN} \quad t_{\max} = t_{\max 0} + 16384 \times \text{CNT} \times t_{\text{osc2}}$$

$$\text{ELSE} \quad t_{\max} = t_{\max 0} + \left[16384 \times \left(\text{CNT} - \left\lceil \frac{4\text{CNT}}{\text{MSB}} \right\rceil \right) + (192 + \text{LSB}) \times 64 \times \left\lceil \frac{4\text{CNT}}{\text{MSB}} \right\rceil \right] \times t_{\text{osc2}}$$

Note: In the above formulae, division results must be rounded down to the next integer value.

Example:

With 2ms timeout selected in MCCR register

Value of T[5:0] Bits in WDGCR Register (Hex.)	Min. Watchdog Timeout (ms) t_{\min}	Max. Watchdog Timeout (ms) t_{\max}
00	1.496	2.048
3F	128	128.552

Table 13. Watchdog Timer Register Map and Reset Values

Address (Hex.)	Register Label	7	6	5	4	3	2	1	0
002Ah	WDGCR Reset Value	WDGA 0	T6 1	T5 1	T4 1	T3 1	T2 1	T1 1	T0 1

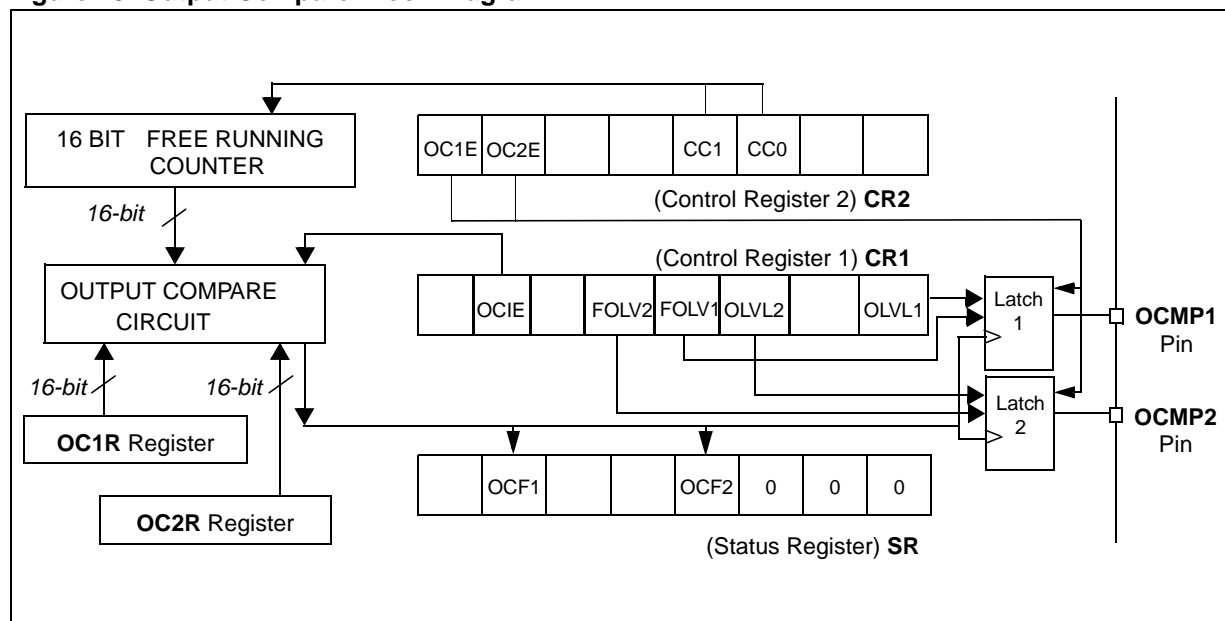
16-BIT TIMER (Cont'd)**Notes:**

1. After a processor write cycle to the OC $\overline{\text{I}}\text{HR}$ register, the output compare function is inhibited until the OC $\overline{\text{I}}\text{LR}$ register is also written.
2. If the OC $\overline{\text{I}}\text{E}$ bit is not set, the OCMP $\overline{\text{i}}$ pin is a general I/O port and the OLV $\overline{\text{L}}\text{i}$ bit will not appear when a match is found but an interrupt could be generated if the OC $\overline{\text{I}}\text{E}$ bit is set.
3. When the timer clock is $f_{\text{CPU}}/2$, OCF $\overline{\text{i}}$ and OCMP $\overline{\text{i}}$ are set while the counter value equals the OC $\overline{\text{I}}\text{R}$ register value (see [Figure 49 on page 78](#)). This behaviour is the same in OPM or PWM mode.
When the timer clock is $f_{\text{CPU}}/4$, $f_{\text{CPU}}/8$ or in external clock mode, OCF $\overline{\text{i}}$ and OCMP $\overline{\text{i}}$ are set while the counter value equals the OC $\overline{\text{I}}\text{R}$ register value plus 1 (see [Figure 50 on page 78](#)).
4. The output compare functions can be used both for generating external events on the OCMP $\overline{\text{i}}$ pins even if the input capture mode is also used.
5. The value in the 16-bit OC $\overline{\text{I}}\text{R}$ register and the OLV $\overline{\text{L}}\text{i}$ bit should be changed after each successful comparison in order to control an output waveform or establish a new elapsed timeout.

Forced Compare Output capability

When the FOLV $\overline{\text{i}}$ bit is set by software, the OLV $\overline{\text{L}}\text{i}$ bit is copied to the OCMP $\overline{\text{i}}$ pin. The OLV $\overline{\text{L}}\text{i}$ bit has to be toggled in order to toggle the OCMP $\overline{\text{i}}$ pin when it is enabled (OC $\overline{\text{I}}\text{E}$ bit=1). The OCF $\overline{\text{i}}$ bit is then not set by hardware, and thus no interrupt request is generated.

The FOLV $\overline{\text{L}}\text{i}$ bits have no effect in both one pulse mode and PWM mode.

Figure 48. Output Compare Block Diagram

16-BIT TIMER (Cont'd)**CONTROL/STATUS REGISTER (CSR)**

Read/Write (bits 7:3 read only)

Reset Value: xxxx x0xx (xxh)

7							0
ICF1	OCF1	TOF	ICF2	OCF2	TIMD	0	0

Bit 7 = **ICF1** *Input Capture Flag 1*.

0: No input capture (reset value).

1: An input capture has occurred on the ICAP1 pin or the counter has reached the OC2R value in PWM mode. To clear this bit, first read the SR register, then read or write the low byte of the IC1R (IC1LR) register.

Bit 6 = **OCF1** *Output Compare Flag 1*.

0: No match (reset value).

1: The content of the free running counter has matched the content of the OC1R register. To clear this bit, first read the SR register, then read or write the low byte of the OC1R (OC1LR) register.

Bit 5 = **TOF** *Timer Overflow Flag*.

0: No timer overflow (reset value).

1: The free running counter rolled over from FFFFh to 0000h. To clear this bit, first read the SR register, then read or write the low byte of the CR (CLR) register.

Note: Reading or writing the ACLR register does not clear TOF.

Bit 4 = **ICF2** *Input Capture Flag 2*.

0: No input capture (reset value).

1: An input capture has occurred on the ICAP2 pin. To clear this bit, first read the SR register, then read or write the low byte of the IC2R (IC2LR) register.

Bit 3 = **OCF2** *Output Compare Flag 2*.

0: No match (reset value).

1: The content of the free running counter has matched the content of the OC2R register. To clear this bit, first read the SR register, then read or write the low byte of the OC2R (OC2LR) register.

Bit 2 = **TIMD** *Timer disable*.

This bit is set and cleared by software. When set, it freezes the timer prescaler and counter and disabled the output functions (OCMP1 and OCMP2 pins) to reduce power consumption. Access to the timer registers is still available, allowing the timer configuration to be changed, or the counter reset, while it is disabled.

0: Timer enabled

1: Timer prescaler, counter and outputs disabled

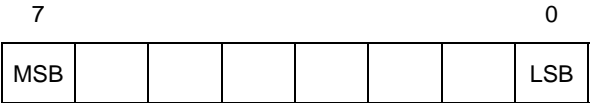
Bits 1:0 = Reserved, must be kept cleared.

16-BIT TIMER (Cont'd)

INPUT CAPTURE 1 HIGH REGISTER (IC1HR)

Read Only
Reset Value: Undefined

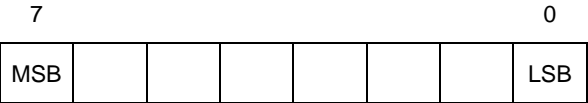
This is an 8-bit read only register that contains the high part of the counter value (transferred by the input capture 1 event).



OUTPUT COMPARE 1 HIGH REGISTER (OC1HR)

Read/Write
Reset Value: 1000 0000 (80h)

This is an 8-bit register that contains the high part of the value to be compared to the CHR register.



INPUT CAPTURE 1 LOW REGISTER (IC1LR)

Read Only
Reset Value: Undefined

This is an 8-bit read only register that contains the low part of the counter value (transferred by the input capture 1 event).



OUTPUT COMPARE 1 LOW REGISTER (OC1LR)

Read/Write
Reset Value: 0000 0000 (00h)

This is an 8-bit register that contains the low part of the value to be compared to the CLR register.



SERIAL COMMUNICATIONS INTERFACE (Cont'd)

10.6.4 Functional Description

The block diagram of the Serial Control Interface, is shown in [Figure 60](#). It contains 6 dedicated registers:

- Two control registers (SCICR1 & SCICR2)
- A status register (SCISR)
- A baud rate register (SCIBRR)
- An extended prescaler receiver register (SCIERP)
- An extended prescaler transmitter register (SCIETPR)

Refer to the register descriptions in [Section 10.6.7](#) for the definitions of each bit.

10.6.4.1 Serial Data Format

Word length may be selected as being either 8 or 9 bits by programming the M bit in the SCICR1 register (see [Figure 60](#)).

The TDO pin is in low state during the start bit.

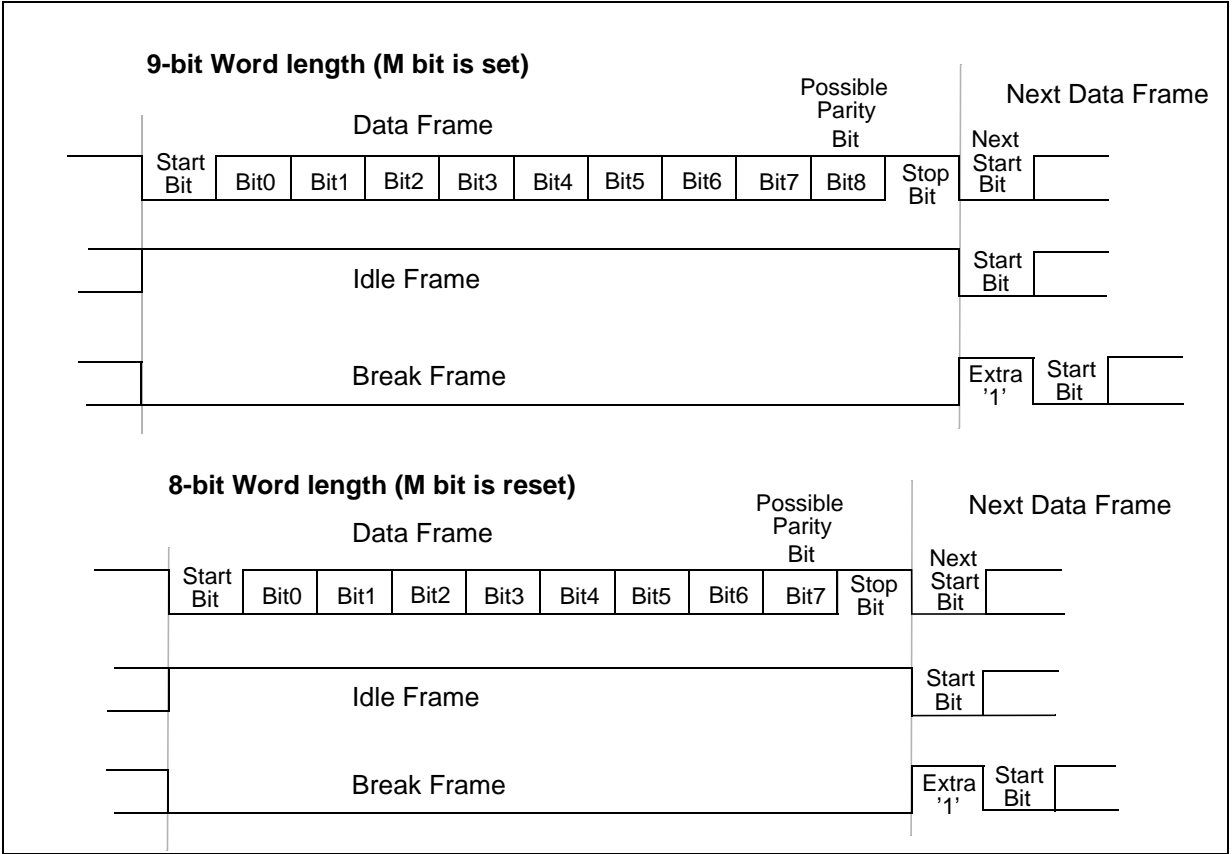
The TDO pin is in high state during the stop bit.

An Idle character is interpreted as an entire frame of “1”s followed by the start bit of the next frame which contains data.

A Break character is interpreted on receiving “0”s for some multiple of the frame period. At the end of the last break frame the transmitter inserts an extra “1” bit to acknowledge the start bit.

Transmission and reception are driven by their own baud rate generator.

Figure 61. Word Length Programming



SERIAL COMMUNICATIONS INTERFACE (Cont'd)

10.6.4.2 Transmitter

The transmitter can send data words of either 8 or 9 bits depending on the M bit status. When the M bit is set, word length is 9 bits and the 9th bit (the MSB) has to be stored in the T8 bit in the SCICR1 register.

Character Transmission

During an SCI transmission, data shifts out least significant bit first on the TDO pin. In this mode, the SCIDR register consists of a buffer (TDR) between the internal bus and the transmit shift register (see [Figure 60](#)).

Procedure

- Select the M bit to define the word length.
- Select the desired baud rate using the SCIBRR and the SCIETPR registers.
- Set the TE bit to assign the TDO pin to the alternate function and to send a idle frame as first transmission.
- Access the SCISR register and write the data to send in the SCIDR register (this sequence clears the TDRE bit). Repeat this sequence for each data to be transmitted.

Clearing the TDRE bit is always performed by the following software sequence:

1. An access to the SCISR register
2. A write to the SCIDR register

The TDRE bit is set by hardware and it indicates:

- The TDR register is empty.
- The data transfer is beginning.
- The next data can be written in the SCIDR register without overwriting the previous data.

This flag generates an interrupt if the TIE bit is set and the I bit is cleared in the CCR register.

When a transmission is taking place, a write instruction to the SCIDR register stores the data in the TDR register and which is copied in the shift register at the end of the current transmission.

When no transmission is taking place, a write instruction to the SCIDR register places the data directly in the shift register, the data transmission starts, and the TDRE bit is immediately set.

When a frame transmission is complete (after the stop bit or after the break frame) the TC bit is set and an interrupt is generated if the TCIE is set and the I bit is cleared in the CCR register.

Clearing the TC bit is performed by the following software sequence:

1. An access to the SCISR register
2. A write to the SCIDR register

Note: The TDRE and TC bits are cleared by the same software sequence.

Break Characters

Setting the SBK bit loads the shift register with a break character. The break frame length depends on the M bit (see [Figure 61](#)).

As long as the SBK bit is set, the SCI send break frames to the TDO pin. After clearing this bit by software the SCI insert a logic 1 bit at the end of the last break frame to guarantee the recognition of the start bit of the next frame.

Idle Characters

Setting the TE bit drives the SCI to send an idle frame before the first data frame.

Clearing and then setting the TE bit during a transmission sends an idle frame after the current word.

Note: Resetting and setting the TE bit causes the data in the TDR register to be lost. Therefore the best time to toggle the TE bit is when the TDRE bit is set i.e. before writing the next byte in the SCIDR.

SERIAL COMMUNICATIONS INTERFACE (Cont'd)**10.6.7 Register Description****STATUS REGISTER (SCISR)**

Read Only

Reset Value: 1100 0000 (C0h)

7							0
TDRE	TC	RDRF	IDLE	OR	NF	FE	PE

Bit 7 = TDRE *Transmit data register empty.*

This bit is set by hardware when the content of the TDR register has been transferred into the shift register. An interrupt is generated if the TIE bit=1 in the SCICR2 register. It is cleared by a software sequence (an access to the SCISR register followed by a write to the SCIDR register).

0: Data is not transferred to the shift register

1: Data is transferred to the shift register

Note: Data will not be transferred to the shift register unless the TDRE bit is cleared.**Bit 6 = TC** *Transmission complete.*

This bit is set by hardware when transmission of a frame containing Data is complete. An interrupt is generated if TCIE=1 in the SCICR2 register. It is cleared by a software sequence (an access to the SCISR register followed by a write to the SCIDR register).

0: Transmission is not complete

1: Transmission is complete

Note: TC is not set after the transmission of a Preamble or a Break.**Bit 5 = RDRF** *Received data ready flag.*

This bit is set by hardware when the content of the RDR register has been transferred to the SCIDR register. An interrupt is generated if RIE=1 in the SCICR2 register. It is cleared by a software sequence (an access to the SCISR register followed by a read to the SCIDR register).

0: Data is not received

1: Received data is ready to be read

Bit 4 = IDLE *Idle line detect.*

This bit is set by hardware when a Idle Line is detected. An interrupt is generated if the ILIE=1 in the SCICR2 register. It is cleared by a software sequence (an access to the SCISR register followed by a read to the SCIDR register).

0: No Idle Line is detected

1: Idle Line is detected

Note: The IDLE bit will not be set again until the RDRF bit has been set itself (i.e. a new idle line occurs).**Bit 3 = OR** *Overrun error.*

This bit is set by hardware when the word currently being received in the shift register is ready to be transferred into the RDR register while RDRF=1. An interrupt is generated if RIE=1 in the SCICR2 register. It is cleared by a software sequence (an access to the SCISR register followed by a read to the SCIDR register).

0: No Overrun error

1: Overrun error is detected

Note: When this bit is set RDR register content will not be lost but the shift register will be overwritten.**Bit 2 = NF** *Noise flag.*

This bit is set by hardware when noise is detected on a received frame. It is cleared by a software sequence (an access to the SCISR register followed by a read to the SCIDR register).

0: No noise is detected

1: Noise is detected

Note: This bit does not generate interrupt as it appears at the same time as the RDRF bit which itself generates an interrupt.**Bit 1 = FE** *Framing error.*

This bit is set by hardware when a de-synchronization, excessive noise or a break character is detected. It is cleared by a software sequence (an access to the SCISR register followed by a read to the SCIDR register).

0: No Framing error is detected

1: Framing error or break character is detected

Note: This bit does not generate interrupt as it appears at the same time as the RDRF bit which itself generates an interrupt. If the word currently being transferred causes both frame error and overrun error, it will be transferred and only the OR bit will be set.**Bit 0 = PE** *Parity error.*

This bit is set by hardware when a parity error occurs in receiver mode. It is cleared by a software sequence (a read to the status register followed by an access to the SCIDR data register). An interrupt is generated if PIE=1 in the SCICR1 register.

0: No parity error

1: Parity error

CONTROLLER AREA NETWORK (Cont'd)

10.8.3.3 Modes of Operation

The CAN Core unit assumes one of the seven states described below:

- **STANDBY.** Standby mode is entered either on a chip reset or on resetting the RUN bit in the Control/Status Register (CSR). Any on-going transmission or reception operation is not interrupted and completes normally before the Bit Time Logic and the clock prescaler are turned off for minimum power consumption. This state is signalled by the RUN bit being read-back as 0. Once in standby, the only event monitored is the reception of a dominant bit which causes a wake-up interrupt if the SCIE bit of the Interrupt Control Register (ICR) is set.

The STANDBY mode is left by setting the RUN

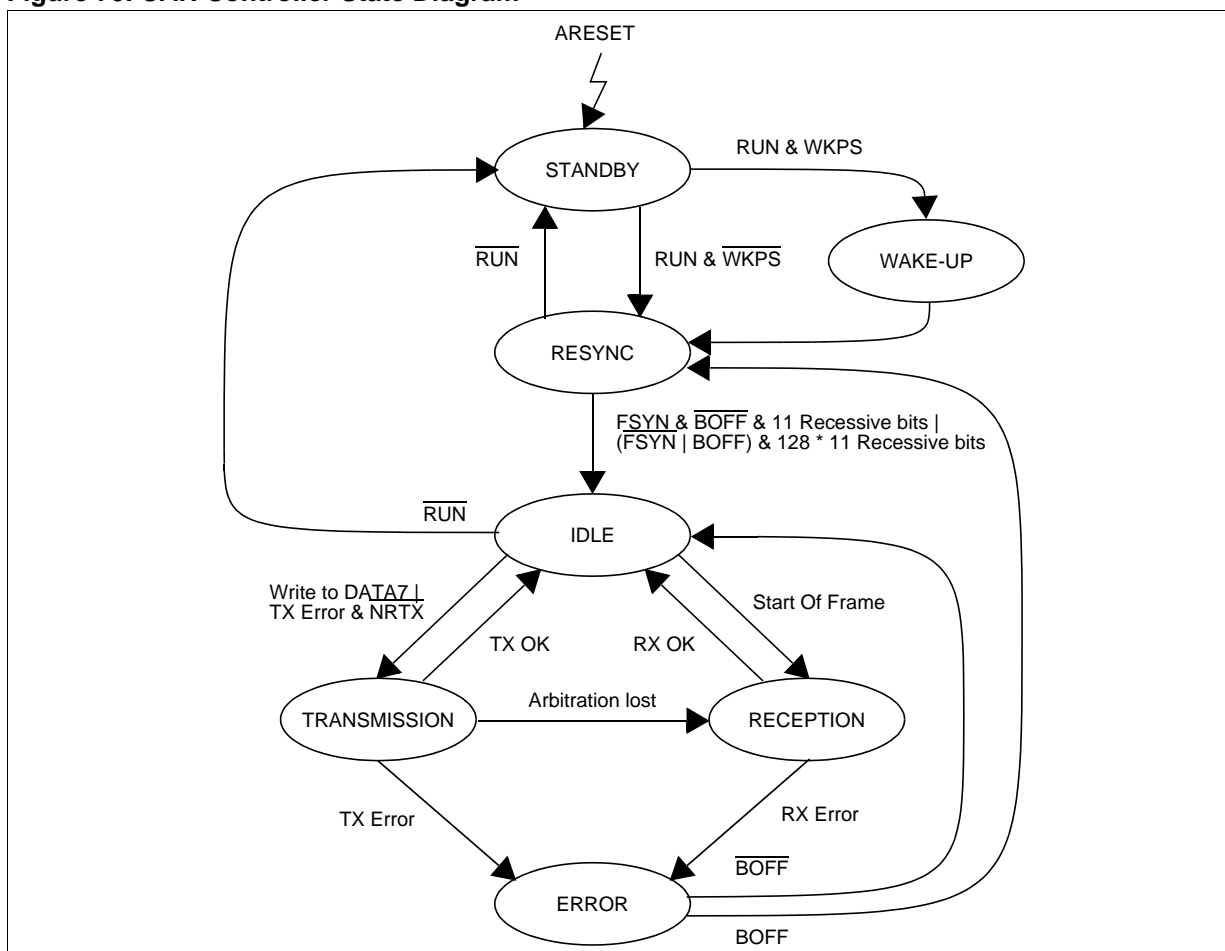
bit. If the WKPS bit is set in the CSR register, then the controller passes through WAKE-UP otherwise it enters RESYNC directly.

It is important to note that the wake-up mechanism is software-driven and therefore carries a significant time overhead. All messages received after the wake-up bit and before the controller is set to run and has completed synchronization are ignored.

Note: Standby mode is not entered on resetting the RUN bit in the Control/Status register (CSR) if the CANRX pin is shorted to GND.

- **WAKE-UP.** The CAN bus line is forced to dominant for one bit time signalling the wake-up condition to all other bus members.

Figure 70. CAN Controller State Diagram



10-BIT A/D CONVERTER (ADC) (Cont'd)

10.9.3 Functional Description

The conversion is monotonic, meaning that the result never decreases if the analog input does not and never increases if the analog input does not.

If the input voltage (V_{AIN}) is greater than V_{AREF} (high-level voltage reference) then the conversion result is FFh in the ADCDRH register and 03h in the ADCDRL register (without overflow indication).

If the input voltage (V_{AIN}) is lower than V_{SSA} (low-level voltage reference) then the conversion result in the ADCDRH and ADCDRL registers is 00 00h.

The A/D converter is linear and the digital result of the conversion is stored in the ADCDRH and ADCDRL registers. The accuracy of the conversion is described in the Electrical Characteristics Section.

R_{AIN} is the maximum recommended impedance for an analog input signal. If the impedance is too high, this will result in a loss of accuracy due to leakage and sampling not being completed in the allotted time.

10.9.3.1 A/D Converter Configuration

The analog input ports must be configured as input, no pull-up, no interrupt. Refer to the «I/O ports» chapter. Using these pins as analog inputs does not affect the ability of the port to be read as a logic input.

In the ADCCSR register:

- Select the CS[3:0] bits to assign the analog channel to convert.

10.9.3.2 Starting the Conversion

In the ADCCSR register:

- Set the ADON bit to enable the A/D converter and to start the conversion. From this time on, the ADC performs a continuous conversion of the selected channel.

When a conversion is complete:

- The EOC bit is set by hardware.
- The result is in the ADCDR registers.

A read to the ADCDRH resets the EOC bit.

To read the 10 bits, perform the following steps:

1. Poll the EOC bit
2. Read the ADCDRL register
3. Read the ADCDRH register. This clears EOC automatically.

Note: The data is not latched, so both the low and the high data register must be read before the next conversion is complete, so it is recommended to disable interrupts while reading the conversion result.

To read only 8 bits, perform the following steps:

1. Poll the EOC bit
2. Read the ADCDRH register. This clears EOC automatically.

10.9.3.3 Changing the conversion channel

The application can change channels during conversion. When software modifies the CH[3:0] bits in the ADCCSR register, the current conversion is stopped, the EOC bit is cleared, and the A/D converter starts converting the newly selected channel.

10.9.4 Low Power Modes

Note: The A/D converter may be disabled by resetting the ADON bit. This feature allows reduced power consumption when no conversion is needed and between single shot conversions.

Mode	Description
WAIT	No effect on A/D Converter
HALT	A/D Converter disabled. After wakeup from Halt mode, the A/D Converter requires a stabilization time t_{STAB} (see Electrical Characteristics) before accurate conversions can be performed.

10.9.5 Interrupts

None.

CLOCK AND TIMING CHARACTERISTICS (Cont'd)

12.5.3 Crystal and Ceramic Resonator Oscillators

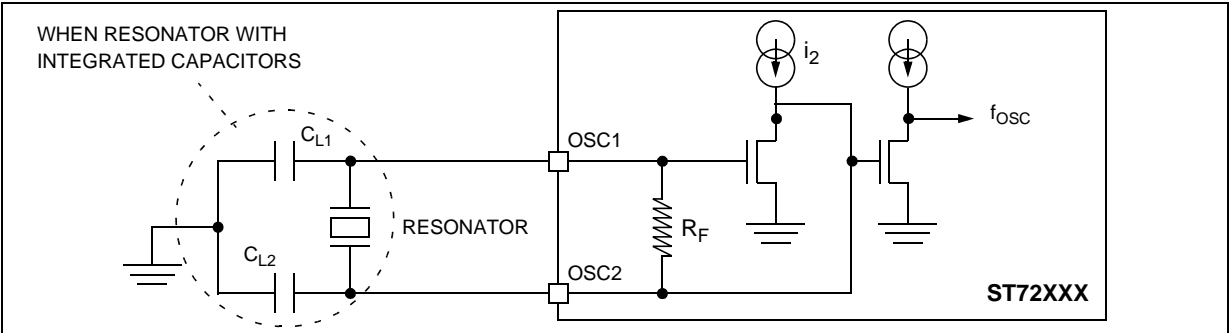
The ST7 internal clock can be supplied with four different Crystal/Ceramic resonator oscillators. All the information given in this paragraph are based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as

close as possible to the oscillator pins in order to minimize output distortion and start-up stabilization time. Refer to the crystal/ceramic resonator manufacturer for more details (frequency, package, accuracy...).

Symbol	Parameter	Conditions	Min	Max	Unit
f_{OSC}	Oscillator Frequency ¹⁾	LP: Low power oscillator MP: Medium power oscillator MS: Medium speed oscillator HS: High speed oscillator	1 >2 >4 >8	2 4 8 16	MHz
R_F	Feedback resistor ²⁾		20	40	k Ω
C_{L1} C_{L2}	Recommended load capacitance versus equivalent serial resistance of the crystal or ceramic resonator (R_S)	$R_S=200\Omega$ LP oscillator $R_S=200\Omega$ MP oscillator $R_S=200\Omega$ MS oscillator $R_S=100\Omega$ HS oscillator	22 22 18 15	56 46 33 33	pF

Symbol	Parameter	Conditions	Typ	Max	Unit
i_2	OSC2 driving current	$V_{DD}=5V$ LP oscillator $V_{IN}=V_{SS}$ MP oscillator MS oscillator HS oscillator	80 160 310 610	150 250 460 910	μA

Figure 92. Typical Application with a Crystal or Ceramic Resonator



Notes:

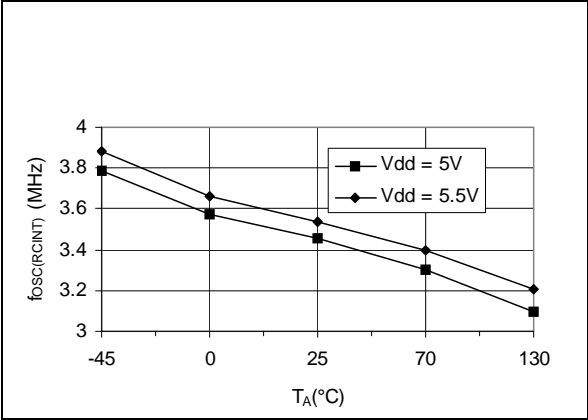
- 1. The oscillator selection can be optimized in terms of supply current using an high quality resonator with small R_S value. Refer to crystal/ceramic resonator manufacturer for more details.
- 2. Data based on characterisation results, not tested in production.

CLOCK CHARACTERISTICS (Cont'd)

12.5.4 RC Oscillators

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f _{OSC (RCINT)}	Internal RC oscillator frequency See Figure 93	T _A =25°C, V _{DD} =5V	2	3.5	5.6	MHz

Figure 93. Typical f_{OSC(RCINT)} vs T_A



Note: To reduce disturbance to the RC oscillator, it is recommended to place decoupling capacitors between V_{DD} and V_{SS} as shown in [Figure 113](#)

EMC CHARACTERISTICS (Cont'd)**12.7.3 Absolute Maximum Ratings (Electrical Sensitivity)**

Based on three different tests (ESD, LU and DLU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

12.7.3.1 Electro-Static Discharge (ESD)

Electro-Static Discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). Two models can be simulated: Human Body Model and Machine Model. This test conforms to the JESD22-A114A/A115A standard.

Absolute Maximum Ratings

Symbol	Ratings	Conditions	Maximum value ¹⁾	Unit
$V_{\text{ESD(HBM)}}$	Electro-static discharge voltage (Human Body Model)	$T_A=+25^{\circ}\text{C}$	2000	V
$V_{\text{ESD(MM)}}$	Electro-static discharge voltage (Machine Model)	$T_A=+25^{\circ}\text{C}$	200	

Notes:

1. Data based on characterization results, not tested in production.

12.7.3.2 Static and Dynamic Latch-Up

■ **LU:** 3 complementary static tests are required on 10 parts to assess the latch-up performance. A supply overvoltage (applied to each power supply pin) and a current injection (applied to each input, output and configurable I/O pin) are performed on each sample. This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.

■ **DLU:** Electro-Static Discharges (one positive then one negative test) are applied to each pin of 3 samples when the micro is running to assess the latch-up performance in dynamic mode. Power supplies are set to the typical values, the oscillator is connected as near as possible to the pins of the micro and the component is put in reset mode. This test conforms to the IEC1000-4-2 and SAEJ1752/3 standards. For more details, refer to the application note AN1181.

Electrical Sensitivities

Symbol	Parameter	Conditions	Class ¹⁾
LU	Static latch-up class	$T_A=+25^{\circ}\text{C}$	A
		$T_A=+85^{\circ}\text{C}$	A
		$T_A=+125^{\circ}\text{C}$	A
DLU	Dynamic latch-up class	$V_{\text{DD}}=5.5\text{V}$, $f_{\text{OSC}}=4\text{MHz}$, $T_A=+25^{\circ}\text{C}$	A

Notes:

1. Class description: A Class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications, that means when a device belongs to Class A it exceeds the JEDEC standard. B Class strictly covers all the JEDEC criteria (international standard).

ADC CHARACTERISTICS (Cont'd)

12.12.1 Analog Power Supply and Reference Pins

Depending on the MCU pin count, the package may feature separate V_{AREF} and V_{SSA} analog power supply pins. These pins supply power to the A/D converter cell and function as the high and low reference voltages for the conversion.

Separation of the digital and analog power pins allow board designers to improve A/D performance. Conversion accuracy can be impacted by voltage drops and noise in the event of heavily loaded or badly decoupled power supply lines (see [Section 12.12.2 General PCB Design Guidelines](#)).

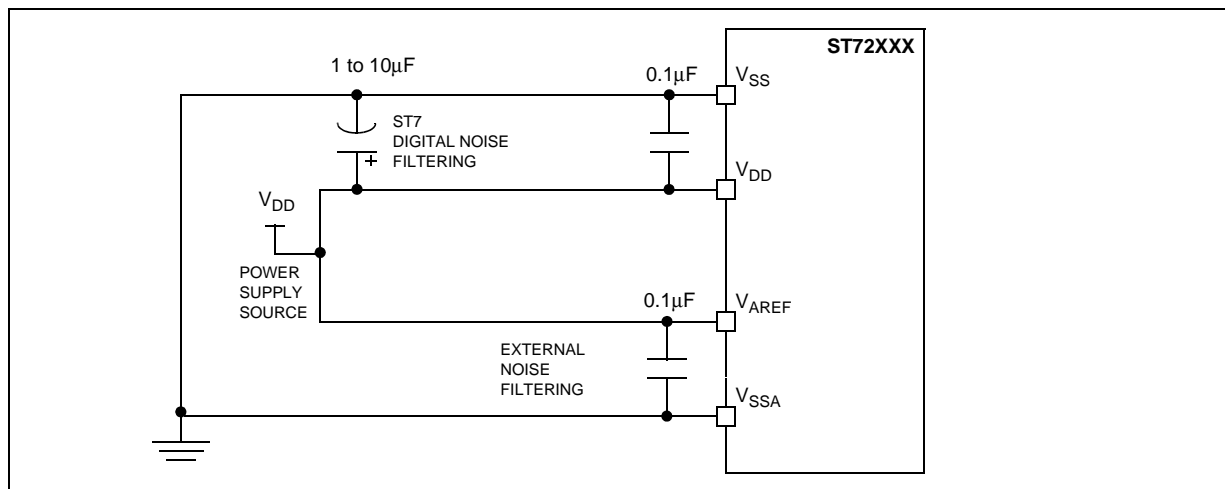
12.12.2 General PCB Design Guidelines

To obtain best results, some general design and layout rules should be followed when designing the application PCB to shield the noise-sensitive, analog physical interface from noise-generating CMOS logic signals.

- Use separate digital and analog planes. The analog ground plane should be connected to the digital ground plane via a single point on the PCB.

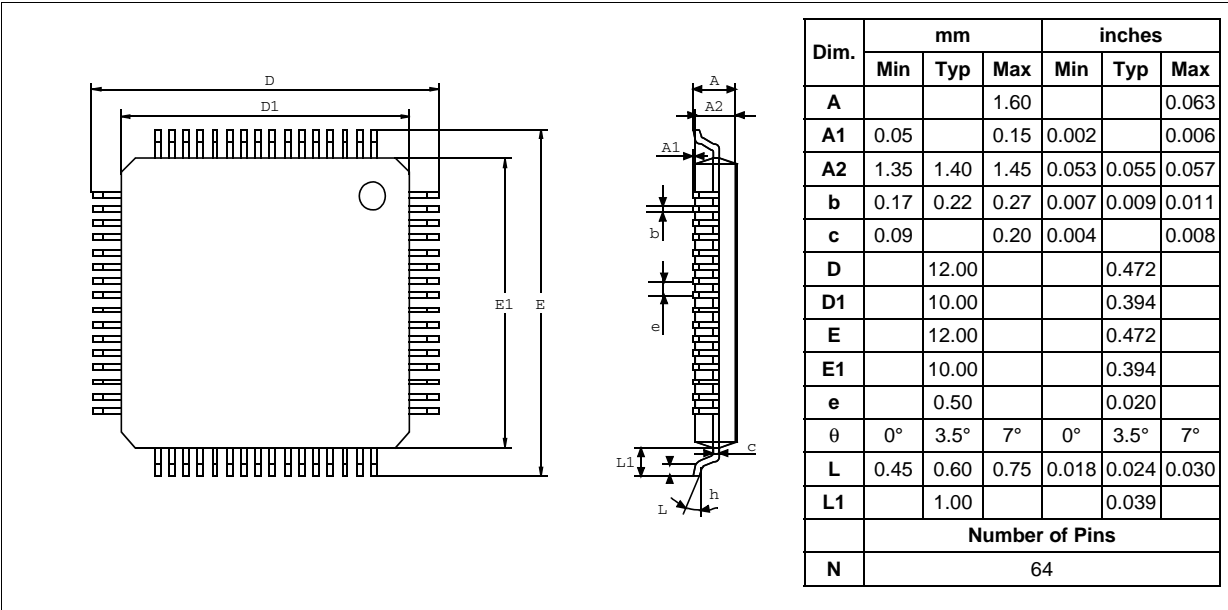
- Filter power to the analog power planes. It is recommended to connect capacitors, with good high frequency characteristics, between the power and ground lines, placing $0.1\mu\text{F}$ and optionally, if needed 10pF capacitors as close as possible to the ST7 power supply pins and a 1 to $10\mu\text{F}$ capacitor close to the power source (see [Figure 113](#)).
- The analog and digital power supplies should be connected in a star network. Do not use a resistor, as V_{AREF} is used as a reference voltage by the A/D converter and any resistance would cause a voltage drop and a loss of accuracy.
- Properly place components and route the signal traces on the PCB to shield the analog inputs. Analog signals paths should run over the analog ground plane and be as short as possible. Isolate analog signals from digital signals that may switch while the analog inputs are being sampled by the A/D converter. Do not toggle digital outputs on the same I/O port as the A/D input being converted.

Figure 113. Power Supply Filtering



PACKAGE MECHANICAL DATA (Cont'd)

Figure 117. 64-Pin Thin Quad Flat Package



13.2 THERMAL CHARACTERISTICS

Symbol	Ratings	Value	Unit
R_{thJA}	Package thermal resistance (junction to ambient)		
	TQFP80 14x14	55	°C/W
	TQFP64 14x14	47	
	TQFP64 10x10	50	
P_D	Power dissipation ¹⁾	500	mW
T_{Jmax}	Maximum junction temperature ²⁾	150	°C

Notes:

1. The power dissipation is obtained from the formula $P_D = P_{INT} + P_{PORT}$ where P_{INT} is the chip internal power ($I_{DD} \times V_{DD}$) and P_{PORT} is the port power dissipation determined by the user.
2. The average chip-junction temperature can be obtained from the formula $T_J = T_A + P_D \times R_{thJA}$.

ST72521 DEVICE CONFIGURATION AND ORDERING INFORMATION (Cont'd)

14.2 DEVICE ORDERING INFORMATION AND TRANSFER OF CUSTOMER CODE

Customer code is made up of the ROM/FAS-TROM contents and the list of the selected options (if any). The ROM/FASTROM contents are to be sent on diskette, or by electronic means, with the S19 hexadecimal file generated by the develop-ment tool. All unused bytes must be set to FFh.

The selected options are communicated to STMicroelectronics using the correctly completed OPTION LIST appended.

Refer to application note AN1635 for information on the counter listing returned by ST after code has been transferred.

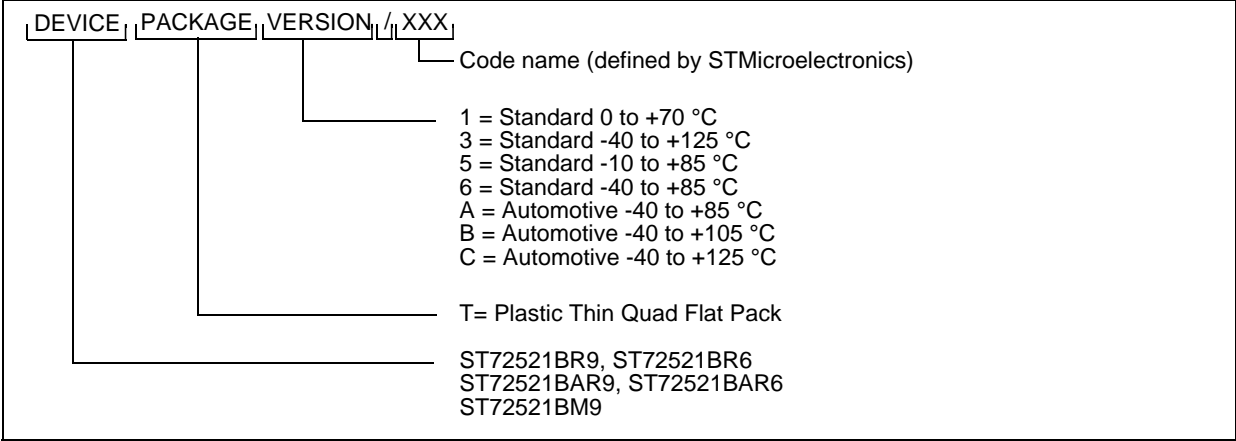
The STMicroelectronics Sales Organization will be pleased to provide detailed information on con-tractual points.

14.2.1 Version-Specific Sales Conditions

To satisfy the different customer requirements and to ensure that ST Standard Microcontrollers will consistently meet or exceed the expectations of each Market Segment, the Codification System for Standard Microcontrollers clearly distinguishes products intended for use in automotive environ-ments, from products intended for use in non-auto-motive environments.

It is the responsibility of the Customer to select the appropriate product for his application.

Figure 118. ROM Factory Coded Device Types



KNOWN LIMITATIONS (Cont'd)**15.1.6 SCI Wrong Break duration****Description**

A single break character is sent by setting and re-setting the SBK bit in the SCICR2 register. In some cases, the break character may have a longer duration than expected:

- 20 bits instead of 10 bits if M=0
- 22 bits instead of 11 bits if M=1.

In the same way, as long as the SBK bit is set, break characters are sent to the TDO pin. This may lead to generate one break more than expected.

Occurrence

The occurrence of the problem is random and proportional to the baudrate. With a transmit frequency of 19200 baud ($f_{CPU}=8\text{MHz}$ and $\text{SCI-BRR}=0\text{x}C9$), the wrong break duration occurrence is around 1%.

Workaround

If this wrong duration is not compliant with the communication protocol in the application, software can request that an Idle line be generated before the break character. In this case, the break duration is always correct assuming the application is not doing anything between the idle and the break. This can be ensured by temporarily disabling interrupts.

The exact sequence is:

- Disable interrupts
- Reset and Set TE (IDLE request)
- Set and Reset SBK (Break Request)
- Re-enable interrupts

15.1.7 16-bit Timer PWM Mode

In PWM mode, the first PWM pulse is missed after writing the value FFFCh in the OC1R register (OC1HR, OC1LR). It leads to either full or no PWM during a period, depending on the OVLV1 and OVLV2 settings.

15.1.8 CAN Cell Limitations

Limitation ¹	Flash	ROM
Omitted SOF bit	x	x
CPU write access (more than one cycle) corrupts CAN frame	x	x
Unexpected Message transmission	x ²	
Bus Off State Not Entered		x ⁴
WKPS Functionality		x ³

x=limitation present

¹For details see [section 10.8.5 on page 146](#)

²Software workaround possible using modified WKPS bit.

³Functionality modified for Unexpected Message Transmission workaround in Flash.

⁴Limitation present on ROM Rev W and Rev Z. Not present in Flash and ROM Rev Y.

15.1.9 I2C Multimaster

In multimaster configurations, if the ST7 I2C receives a START condition from another I2C master after the START bit is set in the I2CCR register and before the START condition is generated by the ST7 I2C, it may ignore the START condition from the other I2C master. In this case, the ST7 master will receive a NACK from the other device. On reception of the NACK, ST7 can send a re-start and Slave address to re-initiate communication