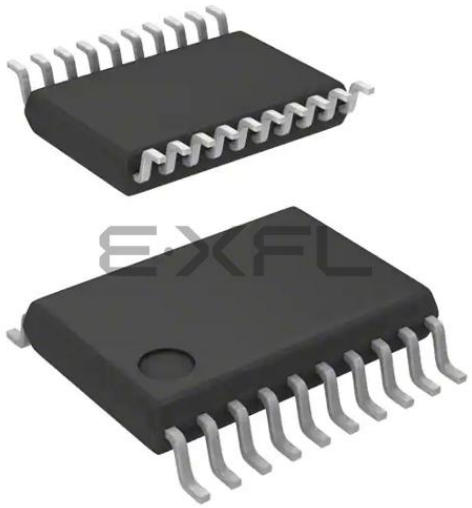
Renesas Electronics America Inc - R5F21162SP#U0 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, SIO, UART/USART
Peripherals	LED, POR, Voltage Detect, WDT
Number of I/O	13
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21162sp-u0

1. Overview

This MCU is built using the high-performance silicon gate CMOS process using the R8C/Tiny Series CPU core and is packaged in a 20-pin plastic molded LSSOP. This MCU operates using sophisticated instructions featuring a high level of instruction efficiency. With 1 Mbyte of address space, it is capable of executing instructions at high speed.
Furthermore, the data flash ROM (1KB × 2blocks) is embedded in the R8C/17 group.
The difference between the R8C/16 and R8C/17 groups is only the existence of the data flash ROM. Their peripheral functions are the same.

1.1 Applications

Electric household appliance, office equipment, housing equipment (sensor, security), general industrial equipment, audio, etc.

1.2 Performance Overview

Table 1.1 lists the Performance Outline of the R8C/16 Group and Table 1.2 lists the Performance Outline of the R8C/17 Group.

Table 1.1 Performance Outline of the R8C/16 Group

Item		Performance
CPU	Number of Basic Instructions	89 instructions
	Minimum Instruction Execution Time	50ns(f(XIN)=20MHz, VCC=3.0 to 5.5V) 100ns(f(XIN)=10MHz, VCC=2.7 to 5.5V)
	Operating Mode	Single-chip
	Address Space	1 Mbyte
	Memory Capacity	See **Table 1.3 R8C/16 Group Product Information**
Peripheral Function	Port	I/O port : 13 pins (including LED drive port), Input : 2 pins
	LED Drive Port	I/O port: 4 pins
	Timer	Timer X: 8 bits × 1 channel, Timer Z: 8 bits × 1 channel (Each timer equipped with 8-bit prescaler) Timer C: 16 bits × 1 channel (Circuits of input capture and output compare)
	Serial Interface	1 channel Clock synchronous serial I/O, UART
	I²C bus Interface (IIC)(1)	1 channel
	A/D Converter	10-bit A/D converter: 1 circuit, 4 channels
	Watchdog Timer	15 bits × 1 channel (with prescaler) Reset start selectable, Count source protection mode
	Interrupt	Internal: 9 factors, External: 4 factors, Software: 4 factors Priority level: 7 levels
	Clock Generation Circuit	2 circuits Main clock oscillation circuit (Equipped with a built-in feedback resistor) On-chip oscillator (high speed, low speed) Equipped with frequency adjustment function on high-speed on-chip oscillator
	Oscillation Stop Detection Function	Main clock oscillation stop detection function
	Voltage Detection Circuit	Included
	Power-on Reset Circuit	Included
Electric Characteristics	Supply Voltage	VCC=3.0 to 5.5V (f(XIN)=20MHz) VCC=2.7 to 5.5V (f(XIN)=10MHz)
	Power Consumption	Typ. 9mA (VCC=5.0V, f(XIN)=20MHz) Typ. 5mA (VCC=3.0V, f(XIN)=10MHz) Typ. 35μA (VCC=3.0V, wait mode, peripheral clock off) Typ. 0.7μA (VCC=3.0V, stop mode)
Flash Memory	Program/Erase Supply Voltage	VCC=2.7 to 5.5V
	Program/Erase Endurance	100 times
Operating Ambient Temperature		-20 to 85°C -40 to 85°C (D Version)
Package		20-pin plastic mold LSSOP

NOTES:
1. I²C bus is a trademark of Koninklijke Philips Electronics N. V.

1.3 Block Diagram

Figure 1.1 shows a Block Diagram.

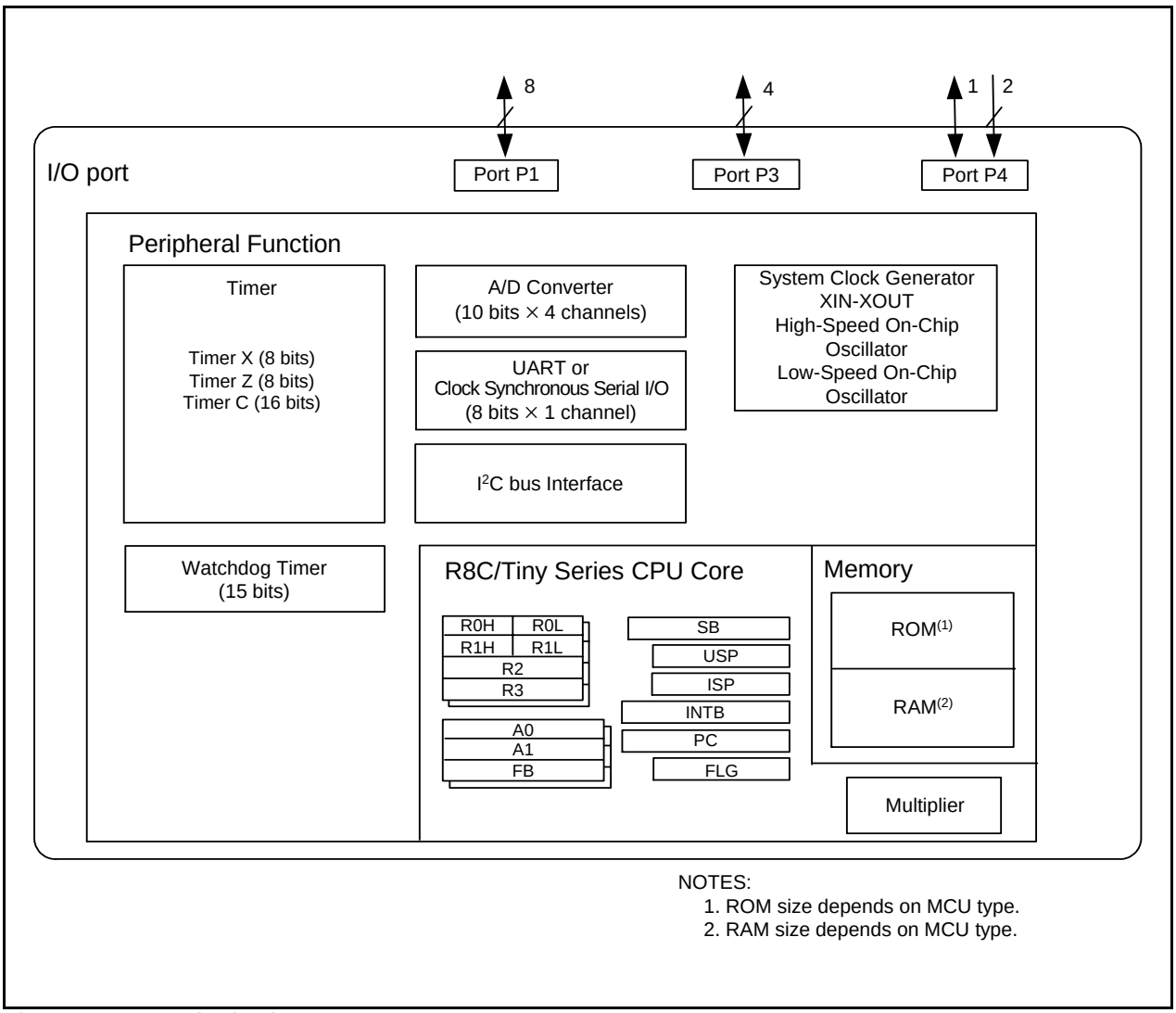


Figure 1.1 Block Diagram

1.4 Product Information

Table 1.3 lists the Product Information of R8C/16 Group and Table 1.4 lists the Product Information of R8C/17 Group.

Table 1.3 Product Information of R8C/16 Group **As of Jan 2006**

Type No.	ROM Capacity	RAM Capacity	Package Type	Remarks
R5F21162SP	8 Kbytes	512 bytes	PLSP0020JB-A	Flash Memory Version
R5F21163SP	12 Kbytes	768 bytes	PLSP0020JB-A	
R5F21164SP	16 Kbytes	1 Kbyte	PLSP0020JB-A	
R5F21162DSP	8 Kbytes	512 bytes	PLSP0020JB-A	D Version
R5F21163DSP	12 Kbytes	768 bytes	PLSP0020JB-A	
R5F21164DSP	16 Kbytes	1 Kbyte	PLSP0020JB-A	

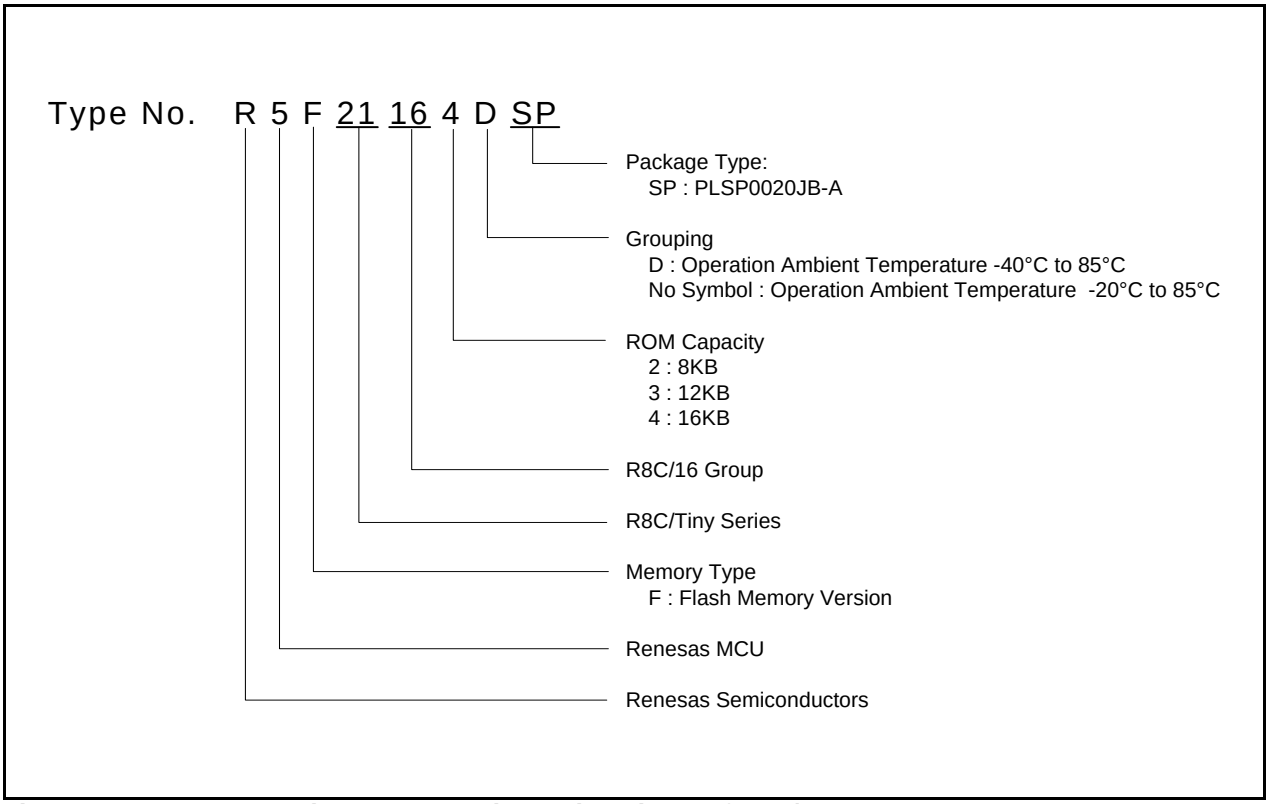


Figure 1.2 Part Number, Memory Size and Package of R8C/16 Group

1.5 Pin Assignments

Figure 1.4 shows the PLSP0020JB-A Package Pin Assignment (top view).

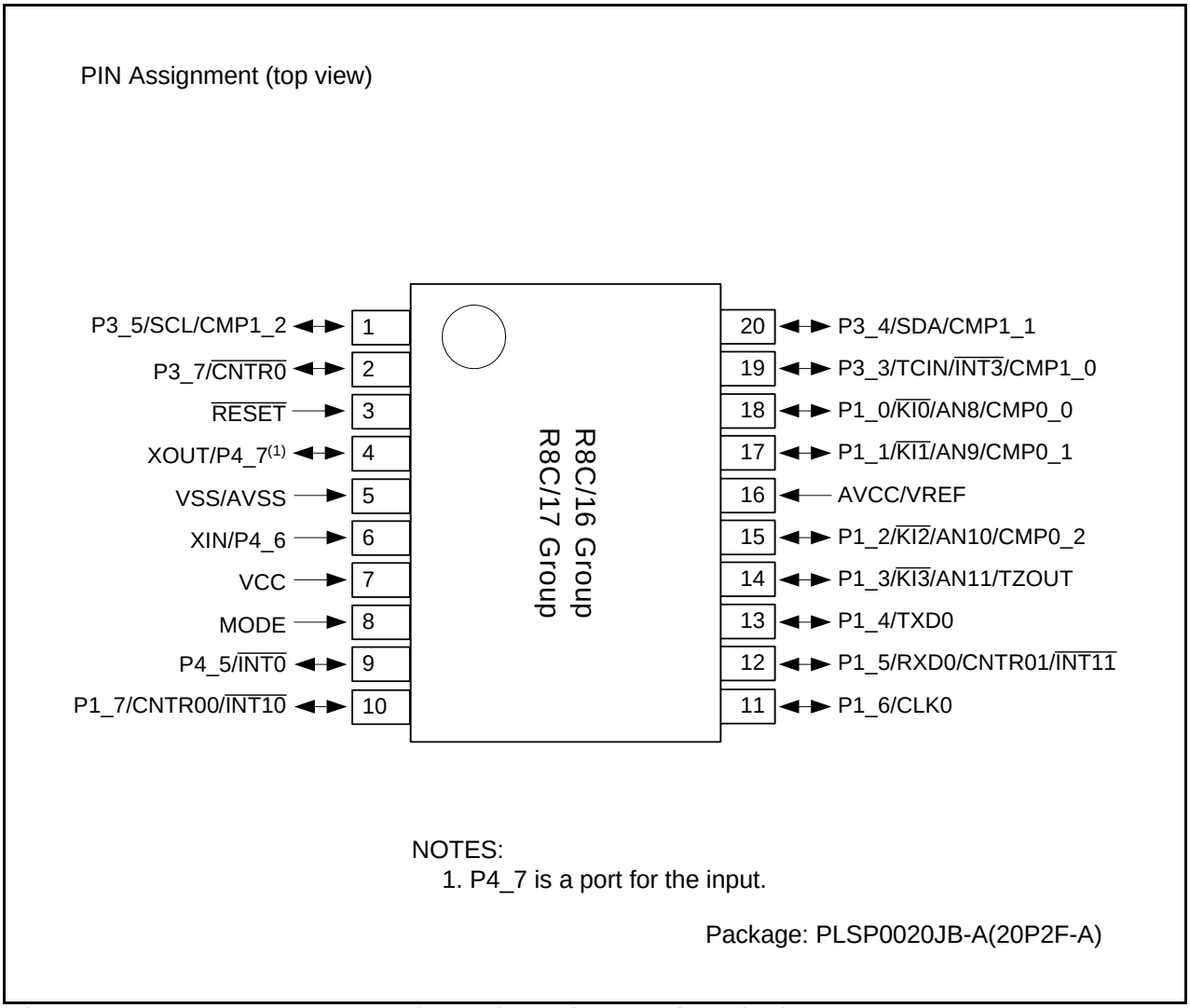


Figure 1.4 PLSP0020JB-A Package Pin Assignment (top view)

Table 1.6 Pin Name Information by Pin Number

Pin Number	Control Pin	Port	I/O Pin of Peripheral Functions				
			Interrupt	Timer	Serial Interface	I²C bus Interface	A/D Converter
1		P3_5		CMP1_2		SCL	
2		P3_7		$\overline{\text{CNTR0}}$			
3	$\overline{\text{RESET}}$						
4	XOUT	P4_7					
5	VSS/AVSS						
6	XIN	P4_6					
7	VCC						
8	MODE						
9		P4_5	$\overline{\text{INT0}}$				
10		P1_7	$\overline{\text{INT10}}$	CNTR00			
11		P1_6			CLK0		
12		P1_5	$\overline{\text{INT11}}$	CNTR01	RXD0		
13		P1_4			TXD0		
14		P1_3	$\overline{\text{KI3}}$	TZOUT			AN11
15		P1_2	$\overline{\text{KI2}}$	CMP0_2			AN10
16	AVCC/VREF						
17		P1_1	$\overline{\text{KI1}}$	CMP0_1			AN9
18		P1_0	$\overline{\text{KI0}}$	CMP0_0			AN8
19		P3_3	$\overline{\text{INT3}}$	TCIN/CMP1_0			
20		P3_4		CMP1_1		SDA	

2.1 Data Registers (R0, R1, R2 and R3)

R0 is a 16-bit register for transfer, arithmetic and logic operations. The same applies to R1 to R3. The R0 can be split into high-order bit (R0H) and low-order bit (R0L) to be used separately as 8-bit data registers. The same applies to R1H and R1L as R0H and R0L. R2 can be combined with R0 to be used as a 32-bit data register (R2R0). The same applies to R3R1 as R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. They also are used for transfer, arithmetic and logic operations. The same applies to A1 as A0. A0 can be combined with A0 to be used as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register indicates the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC, 20 bits wide, indicates the address of an instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointer (SP), USP and ISP, are 16 bits wide each. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is a 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic logic unit.

2.8.2 Debug Flag (D)

The D flag is for debug only. Set to “0”.

2.8.3 Zero Flag (Z)

The Z flag is set to “1” when an arithmetic operation resulted in 0; otherwise, “0”.

2.8.4 Sign Flag (S)

The S flag is set to “1” when an arithmetic operation resulted in a negative value; otherwise, “0”.

2.8.5 Register Bank Select Flag (B)

The register bank 0 is selected when the B flag is “0”. The register bank 1 is selected when this flag is set to “1”.

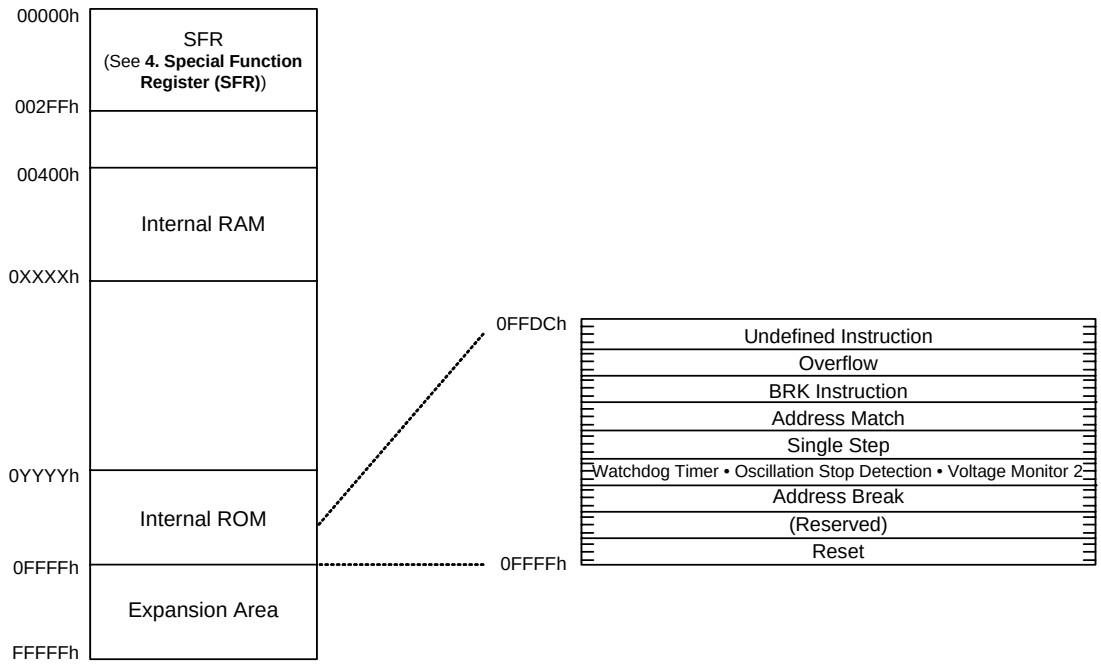
2.8.6 Overflow Flag (O)

The O flag is set to “1” when the operation resulted in an overflow; otherwise, “0”.

3. Memory

3.1 R8C/16 Group

Figure 3.1 is a Memory Map of the R8C/16 group. The R8C/16 group provides 1-Mbyte address space from addresses 00000h to FFFFFh.
The internal ROM is allocated lower addresses beginning with address 0FFFFh. For example, a 16-Kbyte internal ROM is allocated addresses 0C000h to 0FFFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.
The internal RAM is allocated higher addresses beginning with address 00400h. For example, a 1-Kbyte internal RAM is allocated addresses 00400h to 007FFh. The internal RAM is used not only for storing data but for calling subroutines and stacks when interrupt request is acknowledged.
Special function registers (SFR) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated them. All addresses, which have nothing allocated within the SFR, are reserved area and cannot be accessed by users.



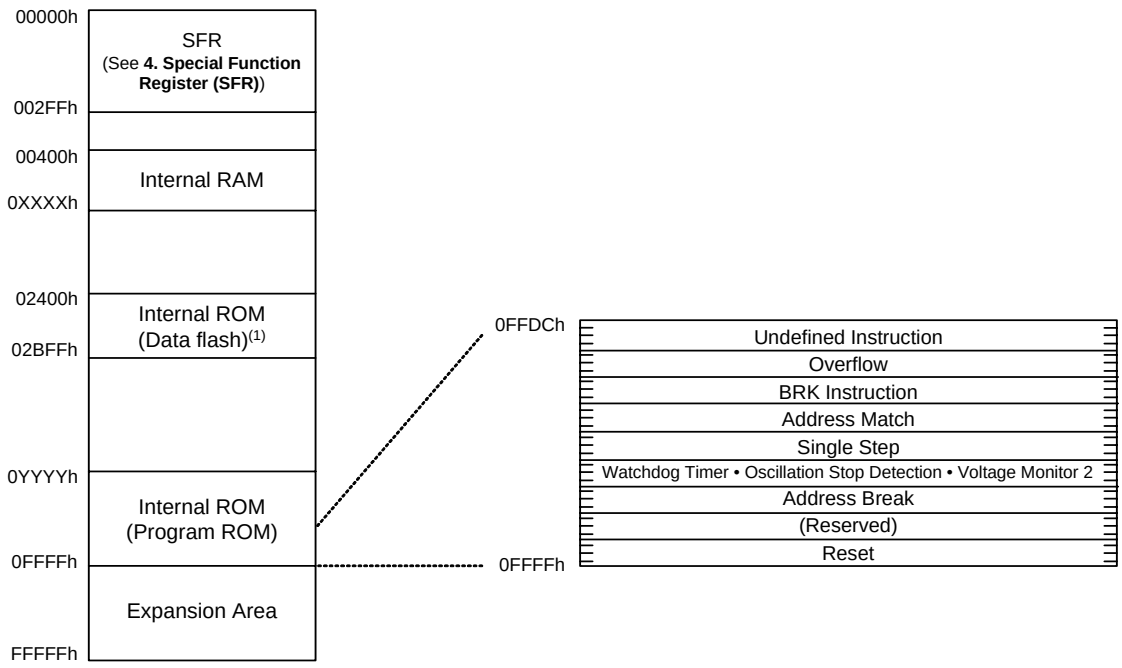
NOTES:
1. Blank spaces are reserved. No access is allowed.

Part Number	Internal ROM		Internal RAM	
	Size	0YYYYh	Size	0XXXXh
R5F21164SP, R5F21164DSP	16 Kbytes	0C000h	1 Kbyte	007FFh
R5F21163SP, R5F21163DSP	12 Kbytes	0D000h	768 bytes	006FFh
R5F21162SP, R5F21162DSP	8 Kbytes	0E000h	512 bytes	005FFh

Figure 3.1 Memory Map of R8C/16 Group

3.2 R8C/17 Group

Figure 3.2 is a memory map of the R8C/17 group. The R8C/17 group provides 1-Mbyte address space from addresses 00000h to FFFFFh.
The internal ROM (program ROM) is allocated lower addresses beginning with address 0FFFFh. For example, a 16-Kbyte internal ROM is allocated addresses 0C000h to 0FFFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.
The internal ROM (data flash) is allocated addresses 02400h to 02BFFh.
The internal RAM is allocated higher addresses beginning with address 00400h. For example, a 1-Kbyte internal RAM is allocated addresses 00400h to 007FFh. The internal RAM is used not only for storing data but for calling subroutines and stacks when interrupt request is acknowledged.
Special function registers (SFR) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated them. All addresses, which have nothing allocated within the SFR, are reserved area and cannot be accessed by users.



NOTES:
1. The data flash block A (1 Kbyte) and block B (1 Kbyte) are shown.
2. Blank spaces are reserved. No access is allowed.

Part Number	Internal ROM		Internal RAM	
	Size	0YYYYh	Size	0XXXXh
R5F21174SP, R5F21174DSP	16 Kbytes	0C000h	1 Kbyte	007FFh
R5F21173SP, R5F21173DSP	12 Kbytes	0D000h	768 bytes	006FFh
R5F21172SP, R5F21172DSP	8 Kbytes	0E000h	512 bytes	005FFh

Figure 3.2 Memory Map of R8C/17 Group

4. Special Function Register (SFR)

SFR (Special Function Register) is the control register of peripheral functions. Tables 4.1 to 4.4 list the SFR information.

Table 4.1 SFR Information(1)[1]

Address	Register	Symbol	After Reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	01101000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h			
0009h	Address Match Interrupt Enable Register	AIER	00h
000Ah	Protect Register	PRCR	00h
000Bh			
000Ch	Oscillation Stop Detection register	OCD	00000100b
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDC	00011111b
0010h	Address Match Interrupt Register 0	RMAD0	00h
0011h			00h
0012h			X0h
0013h			
0014h	Address Match Interrupt Register 1	RMAD1	00h
0015h			00h
0016h			X0h
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	00h
001Dh			
001Eh	$\overline{\text{INT0}}$ Input Filter Select Register	INT0F	00h
001Fh			
0020h	High-Speed On-Chip Oscillator Control Register 0	HRA0	00h
0021h	High-Speed On-Chip Oscillator Control Register 1	HRA1	When shipping
0022h	High-Speed On-Chip Oscillator Control Register 2	HRA2	00h
0023h			
002Ah			
002Bh			
002Ch			
002Dh			
002Eh			
002Fh			
0030h			
0031h	Voltage Detection Register 1[2]	VCA1	00001000b
0032h	Voltage Detection Register 2[2]	VCA2	00h[3] 01000000b[4]
0033h			
0034h			
0035h			
0036h	Voltage Monitor 1 Circuit Control Register [2]	VW1C	0000X000b[3] 0100X001b[4]
0037h	Voltage Monitor 2 Circuit Control Register [5]	VW2C	00h
0038h			
0039h			
003Ah			
003Bh			
003Ch			
003Dh			
003Eh			
003Fh			

X: Undefined

NOTES:

1. Blank spaces are reserved. No access is allowed.
2. Software reset, the watchdog timer reset or the voltage monitor 2 reset does not affect this register.
3. Owing to Hardware reset.
4. Owing to Power-on reset or the voltage monitor 1 reset.
5. Software reset, the watchdog timer reset or the voltage monitor 2 reset does not affect the b2 and b3.

5. Electrical Characteristics

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated value	Unit
V_{CC}	Supply Voltage	V_{CC} = AV_{CC}	-0.3 to 6.5	V
AV_{CC}	Analog Supply Voltage	V_{CC} = AV_{CC}	-0.3 to 6.5	V
V_I	Input Voltage		-0.3 to V_{CC}+0.3	V
V_O	Output Voltage		-0.3 to V_{CC}+0.3	V
P_d	Power Dissipation	T_{opr} = 25°C	300	mW
T_{opr}	Operating Ambient Temperature		-20 to 85 / -40 to 85 (D version)	°C
T_{stg}	Storage Temperature		-65 to 150	°C

Table 5.2 Recommended Operating Conditions

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
V_{CC}	Supply Voltage			2.7	–	5.5	V
AV_{CC}	Analog Supply Voltage			–	V_{CC}(3)	–	V
V_{SS}	Supply Voltage			–	0	–	V
AV_{SS}	Analog Supply Voltage			–	0	–	V
V_{IH}	Input “H” Voltage			0.8V_{CC}	–	V_{CC}	V
V_{IL}	Input “L” Voltage			0	–	0.2V_{CC}	V
$I_{OH(sum)}$	Peak Sum Output “H” Current	Sum of All Pins $I_{OH\ (peak)}$		–	–	-60	mA
$I_{OH(peak)}$	Peak Output “H” Current			–	–	-10	mA
$I_{OH(avg)}$	Average Output “H” Current			–	–	-5	mA
$I_{OL(sum)}$	Peak Sum Output “L” Currents	Sum of All Pins $I_{OL\ (peak)}$		–	–	60	mA
$I_{OL(peak)}$	Peak Output “L” Currents	Except P1_0 to P1_3		–	–	10	mA
		P1_0 to P1_3	Drive Capacity HIGH	–	–	30	mA
			Drive Capacity LOW	–	–	10	mA
$I_{OL(avg)}$	Average Output “L” Current	Except P1_0 to P1_3		–	–	5	mA
		P1_0 to P1_3	Drive Capacity HIGH	–	–	15	mA
			Drive Capacity LOW	–	–	5	mA
$f_{(XIN)}$	Main Clock Input Oscillation Frequency		3.0V ≤ V_{CC} ≤ 5.5V	0	–	20	MHz
			2.7V ≤ V_{CC} < 3.0V	0	–	10	MHz

NOTES:
1. V_{CC} = AV_{CC} = 2.7 to 5.5V at T_{opr} = -20 to 85 °C / -40 to 85 °C, unless otherwise specified.
2. The typical values when average output current is 100ms.
3. Hold V_{CC} = AV_{CC}.

Table 5.4 Flash Memory (Program ROM) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/Erase Endurance(2)	R8C/16 Group	100(3)	–	–	times
		R8C/17 Group	1,000(3)	–	–	times
–	Byte Program Time	V_{CC} = 5.0 V at T_{opr} = 25 °C	–	50	400	µs
–	Block Erase Time	V_{CC} = 5.0 V at T_{opr} = 25 °C	–	0.4	9	s
$t_{d(SR-ES)}$	Time Delay from Suspend Request until Erase Suspend		–	–	8	ms
–	Erase Suspend Request Interval		10	–	–	ms
–	Program, Erase Voltage		2.7	–	5.5	V
–	Read Voltage		2.7	–	5.5	V
–	Program, Erase Temperature		0	–	60	°C
–	Data Hold Time(7)	Ambient temperature = 55 °C	20	–	–	year

NOTES:
1. V_{CC} = AVcc = 2.7 to 5.5V at T_{opr} = 0 to 60 °C, unless otherwise specified.
2. Definition of program and erase
   The program and erase endurance shows an erase endurance for every block.
   If the program and erase endurance is “n” times (n = 100, 10000), “n” times erase can be performed for every block.
   For example, if performing 1-byte write to the distinct addresses on Block A of 1Kbyte block 1,024 times and then erasing that block, program and erase endurance is counted as one time.
   However, do not perform multiple programs to the same address for one time ease.(disable overwriting).
3. Endurance to guarantee all electrical characteristics after program and erase.(1 to “Min.” value can be guaranateed).
4. In the case of a system to execute multiple programs, perform one erase after programming as reducing effective reprogram endurance not to leave blank area as possible such as programming write addresses in turn. If programming a set of 16 bytes, programming up to 128 sets and then erasing them one time can reduce effective reprogram endurance. Additionally, averaging erase endurance for Block A and B can reduce effective reprogram endurance more. To leave erase endurance for every block as information and determine the restricted endurance are recommended.
5. If error occurs during block erase, attempt to execute the clear status register command, then the block erase command at least three times until the erase error does not occur.
6. Customers desiring Program/Erase failure rate information should contact their Renesas technical support representative.
7. The data hold time incudes time that the power supply is off or the clock is not supplied.

Table 5.10 High-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
–	High-Speed On-Chip Oscillator Frequency When the Reset is Deasserted	V_{CC} = 5.0V, T_{opr} = 25 °C	–	8	–	MHz
–	High-Speed On-Chip Oscillator Frequency Temperature • Supplay Voltage Dependence	0 to +60 °C / 5 V ± 5 %(2)	7.44	–	8.56	MHz
		–20 to +85 °C / 2.7 to 5.5 V(2)	7.04	–	8.96	MHz
		–40 to +85 °C / 2.7 to 5.5 V(2)	6.80	–	9.20	MHz

NOTES:
1. The measurement condition is V_{CC} = AV_{CC} = 5.0V and T_{opr} = 25 °C.
2. The standard value shows when the HRA1 register is assumed as the value in shipping and the HRA2 register value is set to 00h.

Table 5.11 Power Supply Circuit Timing Characteristics

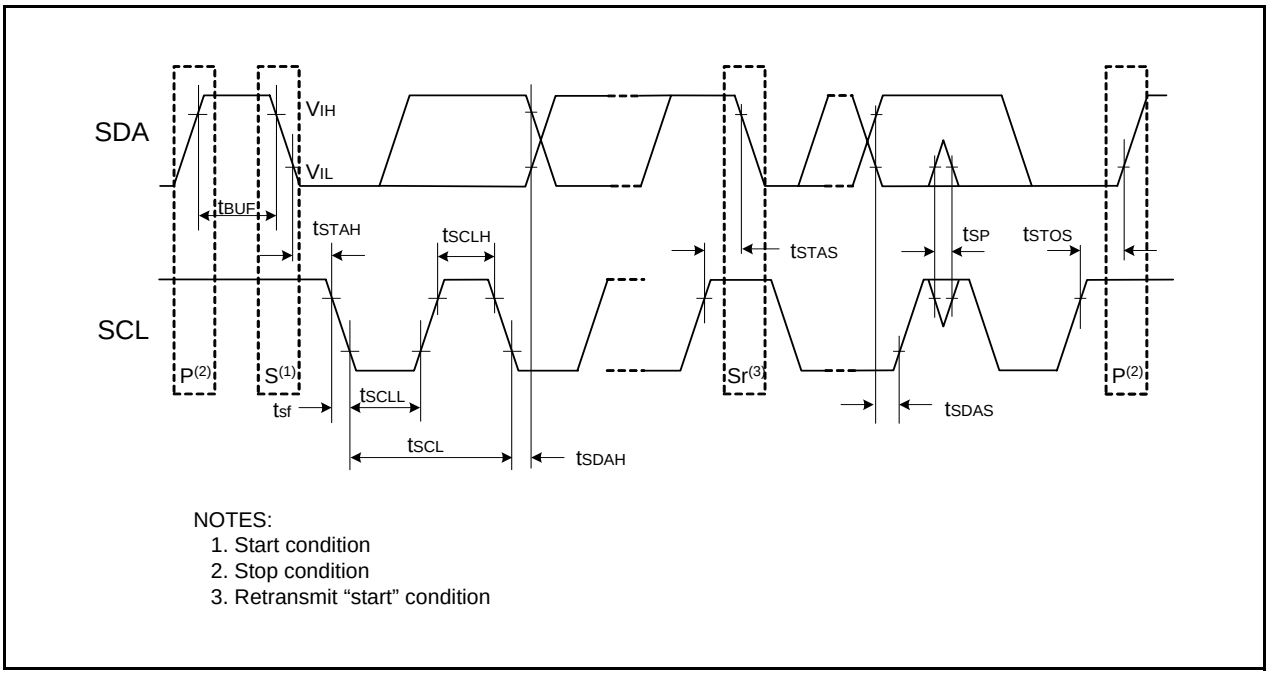
Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for Internal Power Supply Stabilization during Power-On(2)		1	–	2000	µs
$t_{d(R-S)}$	STOP Exit Time(3)		–	–	150	µs

NOTES:
1. The measurement condition is V_{CC} = AV_{CC} = 2.7 to 5.5V and T_{opr} = 25 °C.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.
3. Time until CPU clock supply starts since the interrupt is acknowledged to exit stop mode.

Table 5.12 Timing Requirements of I²C bus Interface (IIC) (1)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t_{SCL}	SCL Input Cycle Time		$12t_{CYC}+600^{(2)}$	–	–	ns
t_{SCLH}	SCL Input “H” Width		$3t_{CYC}+300^{(2)}$	–	–	ns
t_{SCLL}	SCL Input “L” Width		$5t_{CYC}+300^{(2)}$	–	–	ns
t_{sf}	SCL, SDA Input Fall Time		–	–	300	ns
t_{SP}	SCL, SDA Input Spike Pulse Rejection Time		–	–	$1t_{CYC}^{(2)}$	ns
t_{BUF}	SDA Input Bus-Free Time		$5t_{CYC}^{(2)}$	–	–	ns
t_{STAH}	Start Condition Input Hold Time		$3t_{CYC}^{(2)}$	–	–	ns
t_{STAS}	Retransmit Start Condition Input SetUp Time		$3t_{CYC}^{(2)}$	–	–	ns
t_{STOS}	Stop Condition Input SetUp Time		$3t_{CYC}^{(2)}$	–	–	ns
t_{SDAS}	Data Input SetUp Time		$1t_{CYC}+20^{(2)}$	–	–	ns
t_{SDAH}	Data Input Hold Time		0	–	–	ns

NOTES:
1. V_{CC} = AV_{CC} = 2.7 to 5.5V, V_{SS} = 0V and Topr = -20 to 85 °C / -40 to 85 °C, unless otherwise specified.
2. $1t_{CYC}=1/f1(s)$



NOTES:
1. Start condition
2. Stop condition
3. Retransmit “start” condition

Figure 5.4 I/O Timing of I²C bus Interface (IIC)

Table 5.13 Electrical Characteristics (1) [Vcc = 5V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” Voltage	Except X_{OUT}	I_{OH} = -5mA		V_{CC} – 2.0	–	V_{CC}	V
			I_{OH} = -200µA		V_{CC} – 0.3	–	V_{CC}	V
		X_{OUT}	Drive capacity HIGH	I_{OH} = -1mA	V_{CC} – 2.0	–	V_{CC}	V
			Drive capacity LOW	I_{OH} = -500µA	V_{CC} – 2.0	–	V_{CC}	V
V_{OL}	Output “L” Voltage	Except P1_0 to P1_3, X_{OUT}	I_{OL} = 5mA		–	–	2.0	V
			I_{OL} = 200µA		–	–	0.45	V
		P1_0 to P1_3	Drive capacity HIGH	I_{OL} = 15mA	–	–	2.0	V
			Drive capacity LOW	I_{OL} = 5mA	–	–	2.0	V
			Drive capacity LOW	I_{OL} = 200µA	–	–	0.45	V
		X_{OUT}	Drive capacity HIGH	I_{OL} = 1mA	–	–	2.0	V
			Drive capacity LOW	I_{OL} = 500µA	–	–	2.0	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, CNTR0, CNTR1, TCIN, RXD0			0.2	–	1.0	V
		$\overline{RESET}$			0.2	–	2.2	V
I_{IH}	Input “H” current		VI = 5V		–	–	5.0	µA
I_{IL}	Input “L” current		VI = 0V		–	–	-5.0	µA
R_{PULLUP}	Pull-Up Resistance		VI = 0V		30	50	167	kΩ
R_{fXIN}	Feedback Resistance	XIN			–	1.0	–	MΩ
f_{RING-S}	Low-Speed On-Chip Oscillator Frequency				40	125	250	kHz
V_{RAM}	RAM Hold Voltage		During stop mode		2.0	–	–	V

NOTES:
1. V_{CC} = AV_{CC} = 4.2 to 5.5V at T_{opr} = -20 to 85 °C / -40 to 85 °C, f(XIN)=20MHz, unless otherwise specified.

Table 5.14 Electrical Characteristics (2) [Vcc = 5V] (Topr = -40 to 85 °C, unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
I_{CC}	Power Supply Current (V_{CC}=3.3 to 5.5V) In single-chip mode, the output pins are open and other pins are V_{SS}	High-Speed Mode	XIN = 20MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz No division	–	9	15	mA
			XIN = 16MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz No division	–	8	14	mA
			XIN = 10MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz No division	–	5	–	mA
		Medium-Speed Mode	XIN = 20MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz Divide-by-8	–	4	–	mA
			XIN = 16MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz Divide-by-8	–	3	–	mA
			XIN = 10MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz Divide-by-8	–	2	–	mA
		High-Speed On-Chip Oscillator Mode	Main clock off High-speed on-chip oscillator on=8MHz Low-speed on-chip oscillator on=125kHz No division	–	4	8	mA
			Main clock off High-speed on-chip oscillator on=8MHz Low-speed on-chip oscillator on=125kHz Divide-by-8	–	1.5	–	mA
		Low-Speed On-Chip Oscillator Mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz Divide-by-8	–	470	900	µA
		Wait Mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz While a WAIT instruction is executed Peripheral clock operation VCA26 = VCA27 = 0	–	40	80	µA
		Wait Mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz While a WAIT instruction is executed Peripheral clock off VCA26 = VCA27 = 0	–	38	76	µA
		Stop Mode	Main clock off, Topr = 25 °C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA26 = VCA27 = 0	–	0.8	3.0	µA

Timing Requirements (Unless otherwise specified: Vcc = 5V, Vss = 0V at Topr = 25 °C) [Vcc = 5V]

Table 5.15 XIN Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN Input Cycle Time	50	–	ns
$t_{WH(XIN)}$	XIN Input “H” Width	25	–	ns
$t_{WL(XIN)}$	XIN Input “L” Width	25	–	ns

Table 5.16 CNTR0 Input, CNTR1 Input, $\overline{INT1}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CNTR0)}$	CNTR0 Input Cycle Time	100	–	ns
$t_{WH(CNTR0)}$	CNTR0 Input “H” Width	40	–	ns
$t_{WL(CNTR0)}$	CNTR0 input “L” Width	40	–	ns

Table 5.17 TCIN Input, $\overline{INT3}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TCIN)}$	TCIN Input Cycle Time	400(1)	–	ns
$t_{WH(TCIN)}$	TCIN Input “H” Width	200(2)	–	ns
$t_{WL(TCIN)}$	TCIN input “L” Width	200(2)	–	ns

NOTES:
1. When using Timer C input capture mode, adjust the cycle time (1/ Timer C count source frequency x 3) or above.
2. When using Timer C input capture mode, adjust the width (1/ Timer C count source frequency x 1.5) or above.

Table 5.18 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi Input Cycle Time	200	–	ns
$t_{W(CKH)}$	CLKi Input “H” Width	100	–	ns
$t_{W(CKL)}$	CLKi Input “L” Width	100	–	ns
$t_{d(C-Q)}$	TXDi Output Delay Time	–	50	ns
$t_{h(C-Q)}$	TXDi Hold Time	0	–	ns
$t_{su(D-C)}$	RXDi Input Setup Time	50	–	ns
$t_{h(C-D)}$	RCDi Input Hold Time	90	–	ns

Table 5.19 External Interrupt $\overline{INT0}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INT0}$ Input “H” Width	250(1)	–	ns
$t_{W(INL)}$	$\overline{INT0}$ Input “L” Width	250(2)	–	ns

NOTES:
1. When selecting the digital filter by the $\overline{INT0}$ input filter select bit, use the $\overline{INT0}$ input HIGH width to the greater value, either (1/ digital filter clock frequency x 3) or the minimum value of standard.
2. When selecting the digital filter by the $\overline{INT0}$ input filter select bit, use the $\overline{INT0}$ input LOW width to the greater value, either (1/ digital filter clock frequency x 3) or the minimum value of standard.

Timing requirements (Unless otherwise specified: Vcc = 3V, Vss = 0V at Topr = 25 °C) [Vcc = 3V]

Table 5.22 XIN Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN Input Cycle Time	100	–	ns
$t_{WH(XIN)}$	XIN Input “H” Width	40	–	ns
$t_{WL(XIN)}$	XIN Input “L” Width	40	–	ns

Table 5.23 CNTR0 Input, CNTR1 Input, $\overline{INT1}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CNTR0)}$	CNTR0 Input Cycle Time	300	–	ns
$t_{WH(CNTR0)}$	CNTR0 Input “H” Width	120	–	ns
$t_{WL(CNTR0)}$	CNTR0 Input “L” Width	120	–	ns

Table 5.24 TCIN Input, $\overline{INT3}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TCIN)}$	TCIN Input Cycle Time	1,200(1)	–	ns
$t_{WH(TCIN)}$	TCIN Input “H” Width	600(2)	–	ns
$t_{WL(TCIN)}$	TCIN Input “L” Width	600(2)	–	ns

NOTES:
1. When using the Timer C input capture mode, adjust the cycle time (1/ Timer C count source frequency x 3) or above.
2. When using the Timer C input capture mode, adjust the width (1/ Timer C count source frequency x 1.5) or above.

Table 5.25 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi Input Cycle Time	300	–	ns
$t_{W(CKH)}$	CLKi Input “H” Width	150	–	ns
$t_{W(CKL)}$	CLKi Input “L” Width	150	–	ns
$t_{d(C-Q)}$	TXDi Output Delay Time	–	80	ns
$t_{h(C-Q)}$	TXDi Hold Time	0	–	ns
$t_{su(D-C)}$	RXDi Input Setup Time	70	–	ns
$t_{h(C-D)}$	RCDi Input Hold Time	90	–	ns

Table 5.26 External Interrupt $\overline{INT0}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INT0}$ Input “H” Width	380(1)	–	ns
$t_{W(INL)}$	$\overline{INT0}$ Input “L” Width	380(2)	–	ns

NOTES:
1. When selecting the digital filter by the $\overline{INT0}$ input filter select bit, use the $\overline{INT0}$ input HIGH width to the greater value, either (1/ digital filter clock frequency x 3) or the minimum value of standard.
2. When selecting the digital filter by the $\overline{INT0}$ input filter select bit, use the $\overline{INT0}$ input LOW width to the greater value, either (1/ digital filter clock frequency x 3) or the minimum value of standard.

REVISION HISTORY	R8C/16 Group, R8C/17 Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.10	Sep 06, 2004	–	First Edition issued
1.00	Feb 25, 2005	2-3	Tables 1.1 and 1.2 revised
		5	Table 1.3 and figure 1.2 revised
		6	Table 1.4 and figure 1.3 revised
		7-8	Figures 1.4 and 1.5 revised
		16	Table 4.1 revised: - 000Fh: 000XXXXXb → 00011111b - 0036h: 00001000b → 0000X000b and 01001001b → 0100X001b
		18	Tabel 4.3 revised: - 009Ch: FFh → 00h; NOTES2 added - 009Dh: FFh → 00h
		21	Table 5.3 revised
		22	Tables 5.4 and 5.5 revised
		24	Tables 5.8 and 5.9 revised
		25	Table 5.11 revised
		26	Table 5.12 and figure 5.4 added
		27	Table 5.13 revised
		28	Table 5.14 revised
		29, 33	Table 5.16 and 5.23 revised: Table title “INT2” → “INT1”
		31	Table 5.20 revised; NOTE revised
		32	Table 5.21 revised
		35	Package Dimensions revised
1.10	May 26, 2005	5, 6	Tables 1.3 and 1.4 revised
		16	Table 4.1 revised: - 0009h: XXXXXX00b → 00h - 000Ah: 00XXX000b → 00h - 001Eh: XXXXX000b → 00h
		22	Table 5.5 revised; NOTE revised
		26	Fig 5.4 revised
		27	Table 5.13 revised
		31	Table 5.20 revised
2.00	Jan 30, 2006	1	1. Overview; “20-pin plastic molded LSSOP or SDIP” → “20-pin plastic molded LSSOP” revised
		2	Table 1.1 Performance Outline of the R8C/16 Group; Package: “20-pin plastic molded SDIP” deleted
		3	Table 1.2 Performance Outline of the R8C/17 Group; Package: “20-pin plastic molded SDIP” deleted, Flash Memory: (Data area) → (Data flash) (Program area) → (Program ROM) revised
		4	Figure 1.1 Block Diagram; “Peripheral Function” added, “System Clock Generation” → “System Clock Generator” revised
		5, 6	Table 1.3 Product Information of R8C/16 Group, Table 1.4 Product Information of R8C/17 Group; revised. Figure 1.2 Part Number, Memory Size and Package of R8C/16 Group, Figure 1.3 Part Number, Memory Size and Package of R8C/17 Group; Package type: “DD : PRDP0020BA-A” deleted

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