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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Not For New Designs
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I <sup>2</sup> C, SIO, UART/USART
Peripherals	LED, POR, Voltage Detect, WDT
Number of I/O	13
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-LSSOP
Purchase URL	<a href="https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21172sp-u0">https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21172sp-u0</a>

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## 1.2 Performance Overview

Table 1.1 lists the Performance Outline of the R8C/16 Group and Table 1.2 lists the Performance Outline of the R8C/17 Group.

**Table 1.1 Performance Outline of the R8C/16 Group**

Item		Performance
CPU	Number of Basic Instructions	89 instructions
	Minimum Instruction Execution Time	50ns(f(XIN)=20MHz, VCC=3.0 to 5.5V) 100ns(f(XIN)=10MHz, VCC=2.7 to 5.5V)
	Operating Mode	Single-chip
	Address Space	1 Mbyte
	Memory Capacity	See <b>Table 1.3 R8C/16 Group Product Information</b>
Peripheral Function	Port	I/O port : 13 pins (including LED drive port), Input : 2 pins
	LED Drive Port	I/O port: 4 pins
	Timer	Timer X: 8 bits × 1 channel, Timer Z: 8 bits × 1 channel (Each timer equipped with 8-bit prescaler) Timer C: 16 bits × 1 channel (Circuits of input capture and output compare)
	Serial Interface	1 channel Clock synchronous serial I/O, UART
	I <sup>2</sup> C bus Interface (IIC) <sup>(1)</sup>	1 channel
	A/D Converter	10-bit A/D converter: 1 circuit, 4 channels
	Watchdog Timer	15 bits × 1 channel (with prescaler) Reset start selectable, Count source protection mode
	Interrupt	Internal: 9 factors, External: 4 factors, Software: 4 factors Priority level: 7 levels
	Clock Generation Circuit	2 circuits Main clock oscillation circuit (Equipped with a built-in feedback resistor) On-chip oscillator (high speed, low speed) Equipped with frequency adjustment function on high-speed on-chip oscillator
	Oscillation Stop Detection Function	Main clock oscillation stop detection function
	Voltage Detection Circuit	Included
	Power-on Reset Circuit	Included
Electric Characteristics	Supply Voltage	VCC=3.0 to 5.5V (f(XIN)=20MHz) VCC=2.7 to 5.5V (f(XIN)=10MHz)
	Power Consumption	Typ. 9mA (VCC=5.0V, f(XIN)=20MHz) Typ. 5mA (VCC=3.0V, f(XIN)=10MHz) Typ. 35μA (VCC=3.0V, wait mode, peripheral clock off) Typ. 0.7μA (VCC=3.0V, stop mode)
Flash Memory	Program/Erase Supply Voltage	VCC=2.7 to 5.5V
	Program/Erase Endurance	100 times
Operating Ambient Temperature		-20 to 85°C -40 to 85°C (D Version)
Package		20-pin plastic mold LSSOP

**NOTES:**

1. I<sup>2</sup>C bus is a trademark of Koninklijke Philips Electronics N. V.

**Table 1.2 Performance Outline of the R8C/17 Group**

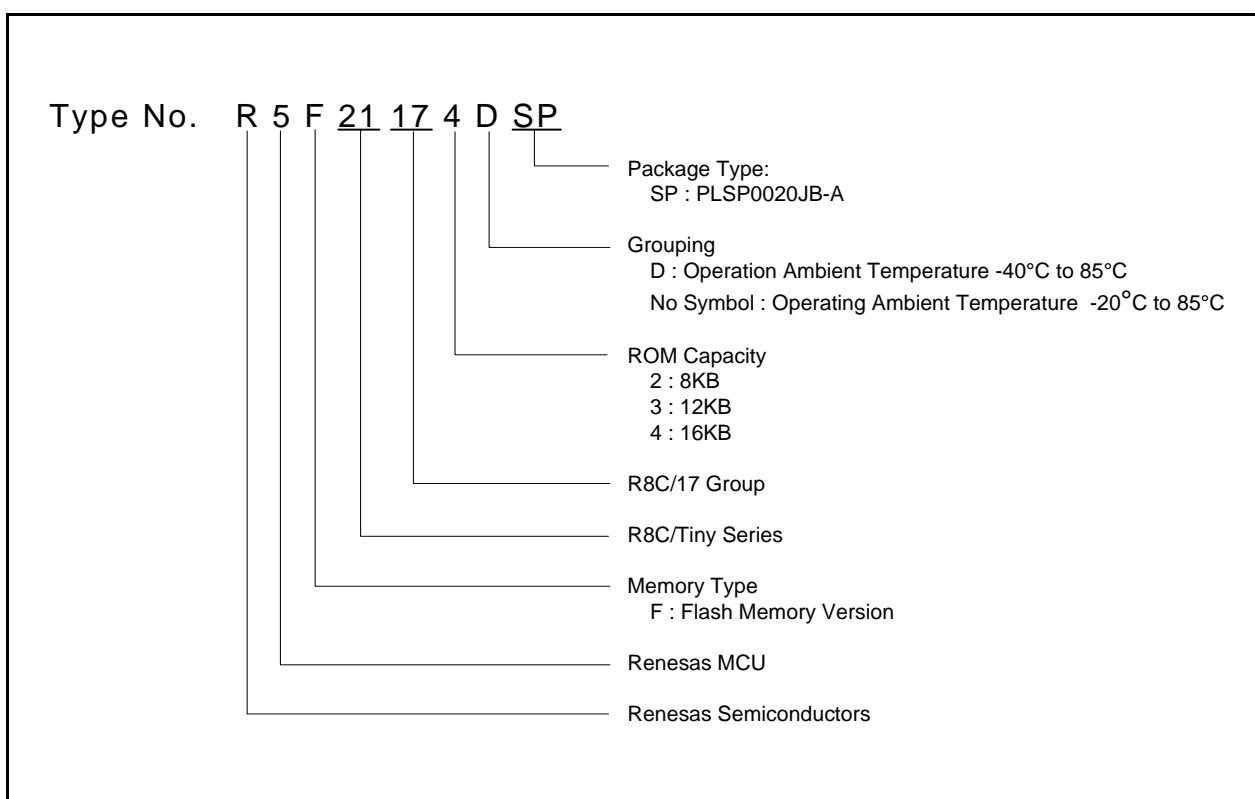
Item		Performance
CPU	Number of Basic Instructions	89 instructions
	Minimum Instruction Execution Time	50ns(f(XIN)=20MHz, VCC=3.0 to 5.5V) 100ns(f(XIN)=10MHz, VCC=2.7 to 5.5V)
	Operating Mode	Single-chip
	Address Space	1 Mbyte
	Memory Capacity	See <b>Table 1.4 R8C/17 Group Product Information</b>
Peripheral Function	Port	I/O : 13 pins (including LED drive port), Input : 2 pin
	LED drive port	I/O port: 4 pins
	Timer	Timer X: 8 bits × 1 channel, Timer Z: 8 bits × 1 channel (Each timer equipped with 8-bit prescaler) Timer C: 16 bits × 1 channel (Circuits of input capture and output compare)
	Serial Interface	1 channel Clock synchronous serial I/O, UART
	I <sup>2</sup> C bus Interface (IIC) <sup>(1)</sup>	1 channel
	A/D Converter	10-bit A/D converter: 1 circuit, 4 channels
	Watchdog Timer	15 bits × 1 channel (with prescaler) Reset start selectable, Count source protection mode
	Interrupt	Internal: 9 factors, External: 4 factors, Software: 4 factors Priority level: 7 levels
	Clock Generation Circuit	2 circuits Main clock generation circuit (Equipped with a built-in feedback resistor) On-chip oscillator (high speed, low speed) Equipped with frequency adjustment function on high-speed on-chip oscillator
	Oscillation Stop Detection Function	Main clock oscillation stop detection function
	Voltage Detection Circuit	Included
	Power-on Reset Circuit	Included
Electric Characteristics	Supply Voltage	VCC=3.0 to 5.5V (f(XIN)=20MHz) VCC=2.7 to 5.5V (f(XIN)=10MHz)
	Power Consumption	Typ. 9mA (VCC = 5.0V, f(XIN) = 20MHz) Typ. 5mA (VCC = 3.0V, f(XIN) = 10MHz) Typ. 35μA (VCC = 3.0V, wait mode, peripheral clock off) Typ. 0.7μA (VCC = 3.0V, stop mode)
Flash Memory	Program/Erase Supply Voltage	VCC=2.7 to 5.5V
	Program and Erase	10,000 times (Data flash)
	Endurance	1,000 times (Program ROM)
Operating Ambient Temperature		-20 to 85°C -40 to 85°C (D Version)
Package		20-pin plastic mold LSSOP

## NOTES:

1. I<sup>2</sup>C bus is a trademark of Koninklijke Philips Electronics N. V.

**Table 1.4 Product Information of R8C/17 Group****As of Jan 2006**

Type No.	ROM Capacity		RAM Capacity	Package Type	Remarks
	Program ROM	Data flash			
R5F21172SP	8 Kbytes	1 Kbyte × 2	512 bytes	PLSP0020JB-A	Flash Memory Version
R5F21173SP	12 Kbytes	1 Kbyte × 2	768 bytes	PLSP0020JB-A	
R5F21174SP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLSP0020JB-A	
R5F21172DSP	8 Kbytes	1 Kbyte × 2	512 bytes	PLSP0020JB-A	D Version
R5F21173DSP	12 Kbytes	1 Kbyte × 2	768 bytes	PLSP0020JB-A	
R5F21174DSP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLSP0020JB-A	

**Figure 1.3 Part Number, Memory Size and Package of R8C/17 Group**

## 1.5 Pin Assignments

Figure 1.4 shows the PLSP0020JB-A Package Pin Assignment (top view).

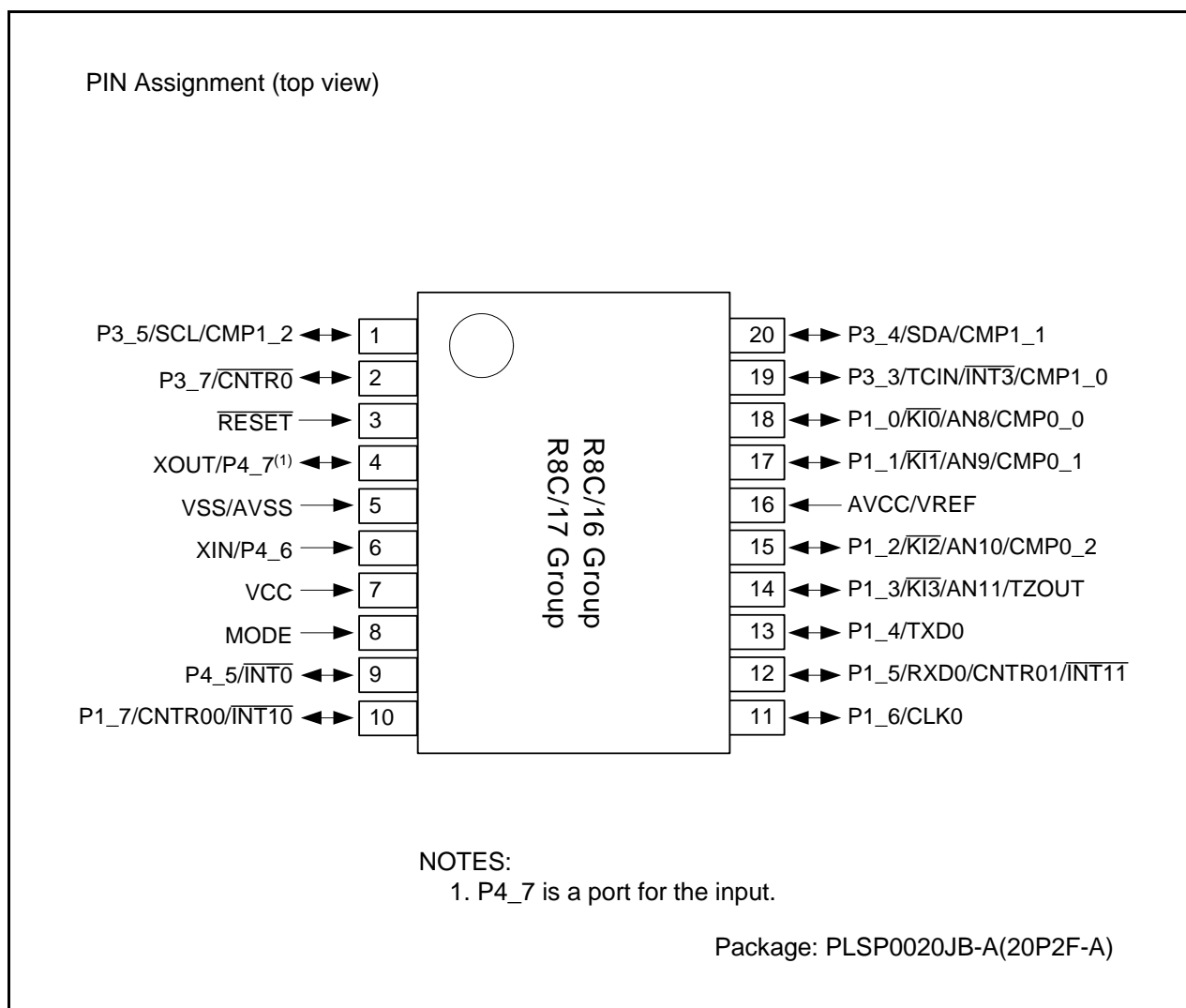


Figure 1.4 PLSP0020JB-A Package Pin Assignment (top view)

**Table 1.6 Pin Name Information by Pin Number**

Pin Number	Control Pin	Port	I/O Pin of Peripheral Functions				
			Interrupt	Timer	Serial Interface	I <sup>2</sup> C bus Interface	A/D Converter
1		P3_5		CMP1_2		SCL	
2		P3_7		CNTR0			
3	RESET						
4	XOUT	P4_7					
5	VSS/AVSS						
6	XIN	P4_6					
7	VCC						
8	MODE						
9		P4_5	INT0				
10		P1_7	INT10	CNTR00			
11		P1_6			CLK0		
12		P1_5	INT11	CNTR01	RXD0		
13		P1_4			TXD0		
14		P1_3	KI3	TZOUT			AN11
15		P1_2	KI2	CMP0_2			AN10
16	AVCC/VREF						
17		P1_1	KI1	CMP0_1			AN9
18		P1_0	KI0	CMP0_0			AN8
19		P3_3	INT3	TCIN/CMP1_0			
20		P3_4		CMP1_1		SDA	

### 3. Memory

#### 3.1 R8C/16 Group

Figure 3.1 is a Memory Map of the R8C/16 group. The R8C/16 group provides 1-Mbyte address space from addresses 00000h to FFFFFh.

The internal ROM is allocated lower addresses beginning with address 0C000h. For example, a 16-Kbyte internal ROM is allocated addresses 0C000h to 0FFFFh.

The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.

The internal RAM is allocated higher addresses beginning with address 00400h. For example, a 1-Kbyte internal RAM is allocated addresses 00400h to 007FFh. The internal RAM is used not only for storing data but for calling subroutines and stacks when interrupt request is acknowledged.

Special function registers (SFR) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated them. All addresses, which have nothing allocated within the SFR, are reserved area and cannot be accessed by users.

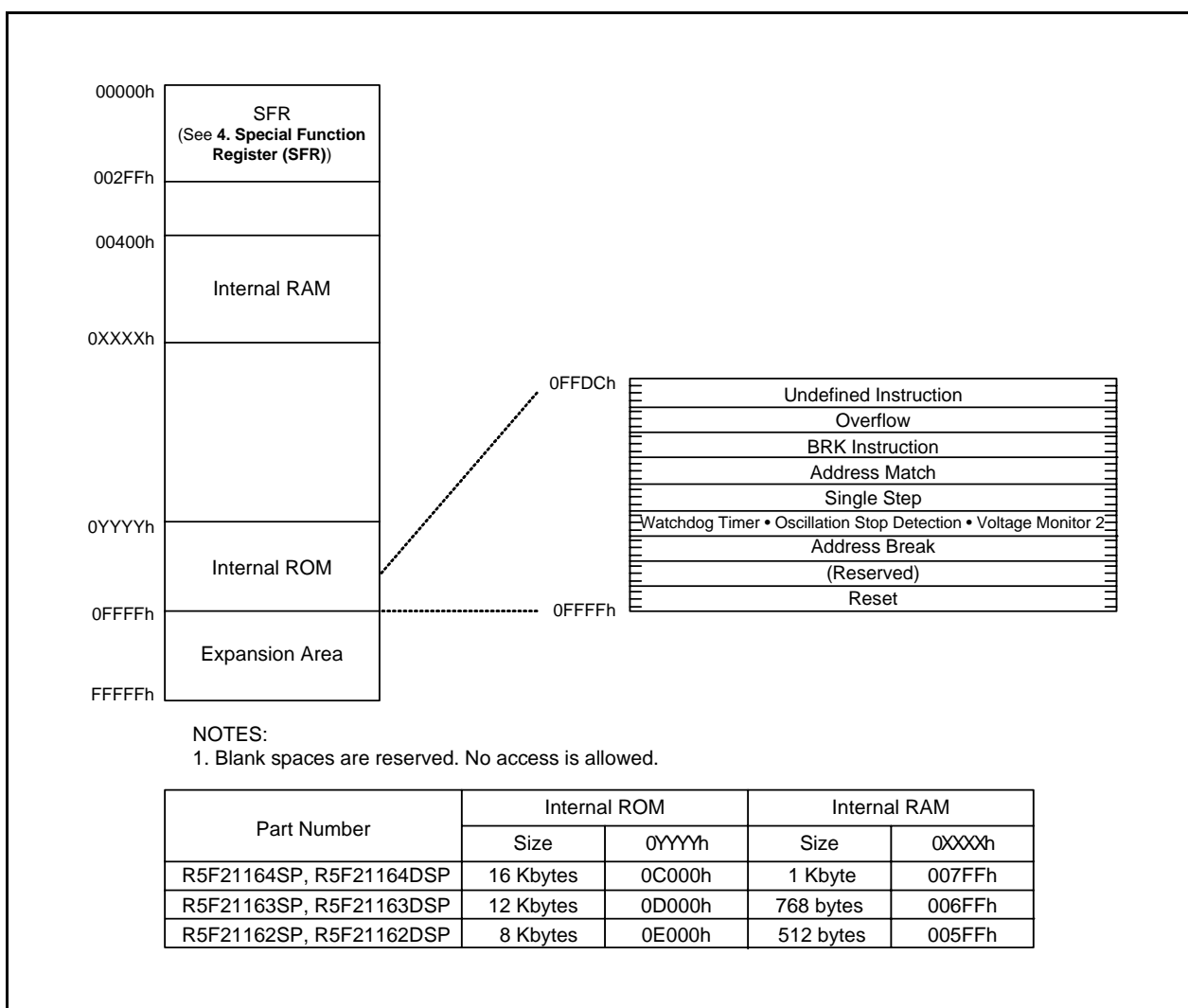


Figure 3.1 Memory Map of R8C/16 Group



### 3.2 R8C/17 Group

Figure 3.2 is a memory map of the R8C/17 group. The R8C/17 group provides 1-Mbyte address space from addresses 00000h to FFFFFh.

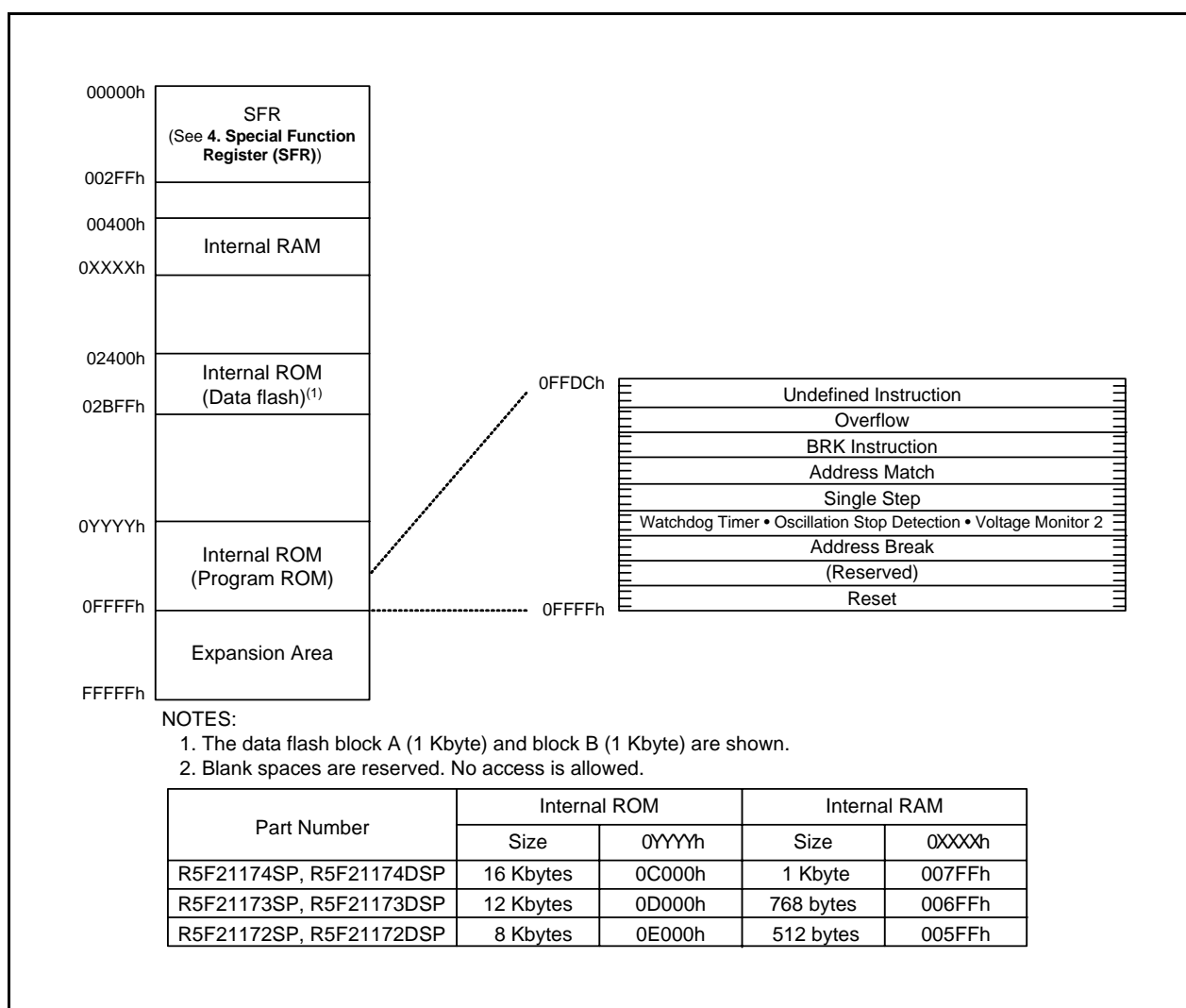
The internal ROM (program ROM) is allocated lower addresses beginning with address 0FFFFh. For example, a 16-Kbyte internal ROM is allocated addresses 0C000h to 0FFFFh.

The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.

The internal ROM (data flash) is allocated addresses 02400h to 02BFFh.

The internal RAM is allocated higher addresses beginning with address 00400h. For example, a 1-Kbyte internal RAM is allocated addresses 00400h to 007FFh. The internal RAM is used not only for storing data but for calling subroutines and stacks when interrupt request is acknowledged.

Special function registers (SFR) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated them. All addresses, which have nothing allocated within the SFR, are reserved area and cannot be accessed by users.



**Figure 3.2 Memory Map of R8C/17 Group**

## 4. Special Function Register (SFR)

SFR (Special Function Register) is the control register of peripheral functions. Tables 4.1 to 4.4 list the SFR information.

**Table 4.1 SFR Information(1)(1)**

Address	Register	Symbol	After Reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	01101000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h			
0009h	Address Match Interrupt Enable Register	AIER	00h
000Ah	Protect Register	PRCR	00h
000Bh			
000Ch	Oscillation Stop Detection register	OSD	00000100b
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDC	00011111b
0010h	Address Match Interrupt Register 0	RMAD0	00h
0011h			00h
0012h			X0h
0013h			
0014h	Address Match Interrupt Register 1	RMAD1	00h
0015h			00h
0016h			X0h
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	00h
001Dh			
001Eh	INT0 Input Filter Select Register	INT0F	00h
001Fh			
0020h	High-Speed On-Chip Oscillator Control Register 0	HRA0	00h
0021h	High-Speed On-Chip Oscillator Control Register 1	HRA1	When shipping
0022h	High-Speed On-Chip Oscillator Control Register 2	HRA2	00h
0023h			
0024h			
0025h			
0026h			
0027h			
0028h			
0029h			
002Ah			
002Bh			
002Ch			
002Dh			
002Eh			
002Fh			
0030h			
0031h	Voltage Detection Register 1 <sup>(2)</sup>	VCA1	00001000b
0032h	Voltage Detection Register 2 <sup>(2)</sup>	VCA2	00h <sup>(3)</sup> 01000000b <sup>(4)</sup>
0033h			
0034h			
0035h			
0036h	Voltage Monitor 1 Circuit Control Register <sup>(2)</sup>	VW1C	0000X000b <sup>(3)</sup> 0100X001b <sup>(4)</sup>
0037h	Voltage Monitor 2 Circuit Control Register <sup>(5)</sup>	VW2C	00h
0038h			
0039h			
003Ah			
003Bh			
003Ch			
003Dh			
003Eh			
003Fh			

X: Undefined

**NOTES:**

- Blank spaces are reserved. No access is allowed.
- Software reset, the watchdog timer reset or the voltage monitor 2 reset does not affect this register.
- Owing to Hardware reset.
- Owing to Power-on reset or the voltage monitor 1 reset.
- Software reset, the watchdog timer reset or the voltage monitor 2 reset does not affect the b2 and b3.

**Table 4.3 SFR Information(3)(1)**

Address	Register	Symbol	After Reset
0080h	Timer Z Mode Register	TZMR	00h
0081h			
0082h			
0083h			
0084h	Timer Z Waveform Output Control Register	PUM	00h
0085h	Prescaler Z Register	PREZ	FFh
0086h	Timer Z Secondary Register	TZSC	FFh
0087h	Timer Z Primary Register	TZPR	FFh
0088h			
0089h			
008Ah	Timer Z Output Control Register	TZOC	00h
008Bh	Timer X Mode Register	TXMR	00h
008Ch	Prescaler X Register	PREX	FFh
008Dh	Timer X Register	TX	FFh
008Eh	Timer Count Source Setting Register	TCSS	00h
008Fh			
0090h	Timer C Register	TC	00h
0091h			00h
0092h			
0093h			
0094h			
0095h			
0096h	External Input Enable Register	INTEN	00h
0097h			
0098h	Key Input Enable Register	KIEN	00h
0099h			
009Ah	Timer C Control Register 0	TCC0	00h
009Bh	Timer C Control Register 1	TCC1	00h
009Ch	Capture, Compare 0 Register	TM0	00h
009Dh	Compare 1 Register	TM1	00h <sup>(2)</sup>
009Eh			FFh
009Fh			FFh
00A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h			XXh
00A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00A5h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00A6h	UART0 Receive Buffer Register	U0RB	XXh
00A7h			XXh
00A8h			
00A9h			
00AAh			
00ABh			
00ACh			
00ADh			
00AEh			
00AFh			
00B0h	UART Transmit/Receive Control Register 2	U0CON	00h
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h	IIC bus Control Register 1	ICCR1	00h
00B9h	IIC bus Control Register 2	ICCR2	7Dh
00BAh	IIC bus Mode Register	ICMR	18h
00BBh	IIC bus Interrupt Enable Register	ICIER	00h
00BCh	IIC bus Status Register	ICSR	00h
00BDh	Slave Address Register	SAR	00h
00BEh	IIC bus Transmit Data Register	ICDRT	FFh
00BFh	IIC bus Receive Data Register	ICDRR	FFh

X: Undefined

**NOTES:**

- Blank spaces are reserved. No access is allowed.
- When output compare mode (the TCC13 bit in the TCC1 register = 1) is selected, the value after reset is "FFFFh".

**Table 4.4 SFR Information(4)(1)**

Address	Register	Symbol	After reset
00C0h	A/D Register	AD	XXh
00C1h			XXh
00C2h			
00C3h			
00C4h			
00C5h			
00C6h			
00C7h			
00C8h			
00C9h			
00CAh			
00CBh			
00CCh			
00CDh			
00CEh			
00CFh			
00D0h	A/D Control Register 2	ADCON2	00h
00D1h			
00D2h			
00D3h			
00D4h			
00D5h			
00D6h			
00D7h			
00D8h			
00D9h			
00DAh			
00DBh			
00DCh			
00DDh			
00DEh			
00DFh			
00E0h	A/D Control Register 0	ADCON0	00000XXXb
00E1h			
00E2h			
00E3h			
00E4h			
00E5h			
00E6h			
00E7h			
00E8h			
00E9h			
00EAh			
00EBh			
00ECh			
00EDh			
00EEh			
00EFh			
00F0h	A/D Control Register 1	ADCON1	00h
00F1h			
00F2h			
00F3h			
00F4h			
00F5h			
00F6h			
00F7h			
00F8h			
00F9h			
00FAh			
00FBh			
00FCh			
00FDh			
00FEh			
00FFh			
00E0h	Port P1 Register	P1	XXh
00E1h	Port P1 Direction Register	PD1	00h
00E2h			
00E3h	Port P3 Register	P3	XXh
00E4h	Port P3 Direction Register	PD3	00h
00E5h			
00E6h	Port P4 Register	P4	XXh
00E7h	Port P4 Direction Register	PD4	00h
00E8h			
00E9h			
00EAh			
00EBh			
00ECh			
00EDh			
00EEh			
00EFh			
00F0h			
00F1h			
00F2h			
00F3h			
00F4h			
00F5h			
00F6h			
00F7h			
00F8h			
00F9h			
00FAh			
00FBh			
00FCh	Pull-Up Control Register 0	PUR0	00XX0000b
00FDh	Pull-Up Control Register 1	PUR1	XXXXXX0Xb
00FEh	Port P1 Drive Capacity Control Register	DRR	00h
00FFh	Timer C Output Control Register	TCOUT	00h
01B3h	Flash Memory Control Register 4	FMR4	01000000b
01B4h			
01B5h	Flash Memory Control Register 1	FMR1	1000000Xb
01B6h			
01B7h	Flash Memory Control Register 0	FMR0	00000001b
0FFFh	Optional Function Select Register	OFS	(2)

X: Undefined

## NOTES:

- Blank columns, 0100h to 01B2h and 01B8h to 02FFh are all reserved. No access is allowed.
- The OFS register cannot be changed by program. Use a flash programmer to write to it.

**Table 5.4 Flash Memory (Program ROM) Electrical Characteristics**

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/Erase Endurance <sup>(2)</sup>	R8C/16 Group	100 <sup>(3)</sup>	–	–	times
		R8C/17 Group	1,000 <sup>(3)</sup>	–	–	times
–	Byte Program Time	V <sub>CC</sub> = 5.0 V at T <sub>opr</sub> = 25 °C	–	50	400	μs
–	Block Erase Time	V <sub>CC</sub> = 5.0 V at T <sub>opr</sub> = 25 °C	–	0.4	9	s
t <sub>d</sub> (SR-ES)	Time Delay from Suspend Request until Erase Suspend		–	–	8	ms
–	Erase Suspend Request Interval		10	–	–	ms
–	Program, Erase Voltage		2.7	–	5.5	V
–	Read Voltage		2.7	–	5.5	V
–	Program, Erase Temperature		0	–	60	°C
–	Data Hold Time <sup>(7)</sup>	Ambient temperature = 55 °C	20	–	–	year

**NOTES:**

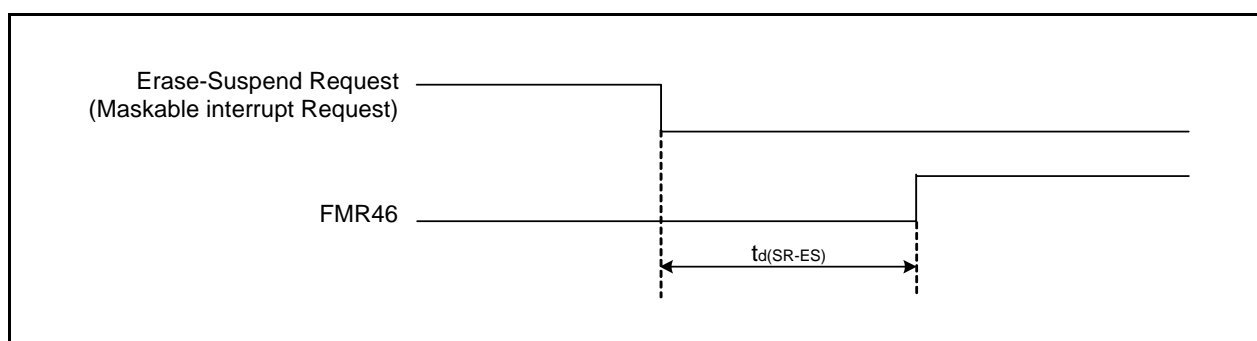
1. V<sub>CC</sub> = AV<sub>CC</sub> = 2.7 to 5.5V at T<sub>opr</sub> = 0 to 60 °C, unless otherwise specified.
2. Definition of program and erase  
The program and erase endurance shows an erase endurance for every block.  
If the program and erase endurance is “n” times (n = 100, 10000), “n” times erase can be performed for every block.  
For example, if performing 1-byte write to the distinct addresses on Block A of 1Kbyte block 1,024 times and then erasing that block, program and erase endurance is counted as one time.  
However, do not perform multiple programs to the same address for one time erase.(disable overwriting).
3. Endurance to guarantee all electrical characteristics after program and erase.(1 to “Min.” value can be guaranteed).
4. In the case of a system to execute multiple programs, perform one erase after programming as reducing effective reprogram endurance not to leave blank area as possible such as programming write addresses in turn. If programming a set of 16 bytes, programming up to 128 sets and then erasing them one time can reduce effective reprogram endurance. Additionally, averaging erase endurance for Block A and B can reduce effective reprogram endurance more. To leave erase endurance for every block as information and determine the restricted endurance are recommended.
5. If error occurs during block erase, attempt to execute the clear status register command, then the block erase command at least three times until the erase error does not occur.
6. Customers desiring Program/Erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

**Table 5.5 Flash Memory (Data flash Block A, Block B) Electrical Characteristics**

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
—	Program/Erase Endurance <sup>(2)</sup>		10,000 <sup>(3)</sup>	—	—	times
—	Byte Program Time (Program/Erase Endurance ≤ 1,000 Times)	V <sub>CC</sub> = 5.0 V at T <sub>opr</sub> = 25 °C	—	50	400	μs
	Byte Program Time (Program/Erase Endurance > 1,000 Times)	V <sub>CC</sub> = 5.0 V at T <sub>opr</sub> = 25 °C	—	65	—	μs
	Block Erase Time (Program/Erase Endurance ≤ 1,000 Times)	V <sub>CC</sub> = 5.0 V at T <sub>opr</sub> = 25 °C	—	0.2	9	s
—	Block Erase Time (Program/Erase Endurance > 1,000 Times)	V <sub>CC</sub> = 5.0 V at T <sub>opr</sub> = 25 °C	—	0.3	—	s
t <sub>d</sub> (SR-ES)	Time Delay from Suspend Request until Erase Suspend		—	—	8	ms
—	Erase Suspend Request Interval		10	—	—	ms
—	Program, Erase Voltage		2.7	—	5.5	V
—	Read Voltage		2.7	—	5.5	V
—	Program, Erase Temperature		-20 <sup>(8)</sup>	—	85	°C
—	Data Hold Time <sup>(9)</sup>	Ambient temperature = 55 °C	20	—	—	year

**NOTES:**

1. V<sub>CC</sub> = AV<sub>CC</sub> = 2.7 to 5.5V at T<sub>opr</sub> = -20 to 85 °C / -40 to 85 °C, unless otherwise specified.
2. Definition of program and erase  
The program and erase endurance shows an erase endurance for every block.  
If the program and erase endurance is "n" times (n = 100, 10000), "n" times erase can be performed for every block.  
For example, if performing 1-byte write to the distinct addresses on Block A of 1Kbyte block 1,024 times and then erasing that block, program and erase endurance is counted as one time.  
However, do not perform multiple programs to the same address for one time erase.(disable overwriting).
3. Endurance to guarantee all electrical characteristics after program and erase.(1 to "Min." value can be guaranteed).
4. Standard of Block A and Block B when program and erase endurance exceeds 1,000 times. Byte program time to 1,000 times are the same as that in program area.
5. In the case of a system to execute multiple programs, perform one erase after programming as reducing effective reprogram endurance not to leave blank area as possible such as programming write addresses in turn. If programming a set of 16 bytes, programming up to 128 sets and then erasing them one time can reduce effective reprogram endurance. Additionally, averaging erase endurance for Block A and B can reduce effective reprogram endurance more. To leave erase endurance for every block as information and determine the restricted endurance are recommended.
6. If error occurs during block erase, attempt to execute the clear status register command, then the block erase command at least three times until the erase error does not occur.
7. Customers desiring Program/Erase failure rate information should contact their Renesas technical support representative.
8. -40 °C for D version.
9. The data hold time includes time that the power supply is off or the clock is not supplied.

**Figure 5.2 Time delay from Suspend Request until Erase Suspend****Table 5.6 Voltage Detection 1 Circuit Electrical Characteristics**

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V <sub>det1</sub>	Voltage Detection Level <sup>(3)</sup>		2.70	2.85	3.00	V
—	Voltage Detection Circuit Self Power Consumption	VCA26 = 1, V <sub>CC</sub> = 5.0V	—	600	—	nA
t <sub>d(E-A)</sub>	Waiting Time until Voltage Detection Circuit Operation Starts <sup>(2)</sup>		—	—	100	μs
V <sub>CCmin</sub>	Microcomputer Operating Voltage Minimum Value		2.7	—	—	V

**NOTES:**

1. The measurement condition is V<sub>CC</sub> = AV<sub>CC</sub> = 2.7V to 5.5V and T<sub>opr</sub> = -40°C to 85 °C.
2. Necessary time until the voltage detection circuit operates when setting to "1" again after setting the VCA26 bit in the VCA2 register to "0".
3. Hold V<sub>det2</sub> > V<sub>det1</sub>.

**Table 5.7 Voltage Detection 2 Circuit Electrical Characteristics**

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V <sub>det2</sub>	Voltage Detection Level <sup>(4)</sup>		3.00	3.30	3.60	V
—	Voltage Monitor 2 Interrupt Request Generation Time <sup>(2)</sup>		—	40	—	μs
—	Voltage Detection Circuit Self Power Consumption	VCA27 = 1, V <sub>CC</sub> = 5.0V	—	600	—	nA
t <sub>d(E-A)</sub>	Waiting Time until Voltage Detection Circuit Operation Starts <sup>(3)</sup>		—	—	100	μs

**NOTES:**

1. The measurement condition is V<sub>CC</sub> = AV<sub>CC</sub> = 2.7V to 5.5V and T<sub>opr</sub> = -40°C to 85 °C.
2. Time until the voltage monitor 2 interrupt request is generated since the voltage passes V<sub>det1</sub>.
3. Necessary time until the voltage detection circuit operates when setting to "1" again after setting the VCA27 bit in the VCA2 register to "0".
4. Hold V<sub>det2</sub> > V<sub>det1</sub>.

**Table 5.8 Reset Circuit Electrical Characteristics (When Using Voltage Monitor 1 Reset)**

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
$V_{por2}$	Power-On Reset Valid Voltage	$-20^{\circ}\text{C} \leq T_{opr} < 85^{\circ}\text{C}$	—	—	$V_{det1}$	V
$t_{w(V_{por2}-V_{det1})}$	Supply Voltage Rising Time When Power-On Reset is Deasserted <sup>(1)</sup>	$-20^{\circ}\text{C} \leq T_{opr} < 85^{\circ}\text{C}$ , $t_{w(por2)} \geq 0\text{s}^{(3)}$	—	—	100	ms

## NOTES:

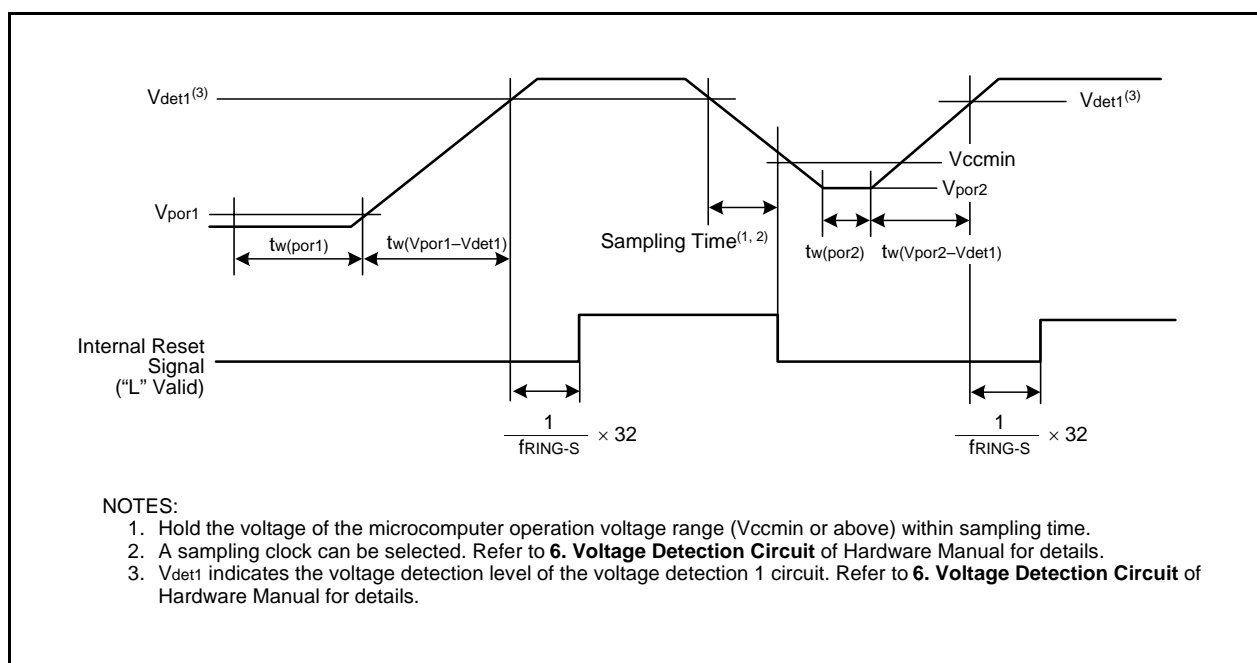
1. This condition is not applicable when using with  $V_{cc} \geq 1.0\text{V}$ .
2. When turning power on after the time to hold the external power below effective voltage ( $V_{por1}$ ) exceeds 10s, refer to **Table 5.9 Reset Circuit Electrical Characteristics (When Not Using Voltage Monitor 1 Reset)**.
3.  $t_{w(por2)}$  is time to hold the external power below effective voltage ( $V_{por2}$ ).

**Table 5.9 Reset Circuit Electrical Characteristics (When Not Using Voltage Monitor 1 Reset)**

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
$V_{por1}$	Power-On Reset Valid Voltage	$-20^{\circ}\text{C} \leq T_{opr} < 85^{\circ}\text{C}$	—	—	0.1	V
$t_{w(V_{por1}-V_{det1})}$	Supply Voltage Rising Time When Power-On Reset is Deasserted	$0^{\circ}\text{C} \leq T_{opr} \leq 85^{\circ}\text{C}$ , $t_{w(por1)} \geq 10\text{s}^{(2)}$	—	—	100	ms
$t_{w(V_{por1}-V_{det1})}$	Supply Voltage Rising Time When Power-On Reset is Deasserted	$-20^{\circ}\text{C} \leq T_{opr} < 0^{\circ}\text{C}$ , $t_{w(por1)} \geq 30\text{s}^{(2)}$	—	—	100	ms
$t_{w(V_{por1}-V_{det1})}$	Supply Voltage Rising Time When Power-On Reset is Deasserted	$-20^{\circ}\text{C} \leq T_{opr} < 0^{\circ}\text{C}$ , $t_{w(por1)} \geq 10\text{s}^{(2)}$	—	—	1	ms
$t_{w(V_{por1}-V_{det1})}$	Supply Voltage Rising Time When Power-On Reset is Deasserted	$0^{\circ}\text{C} \leq T_{opr} \leq 85^{\circ}\text{C}$ , $t_{w(por1)} \geq 1\text{s}^{(2)}$	—	—	0.5	ms

## NOTES:

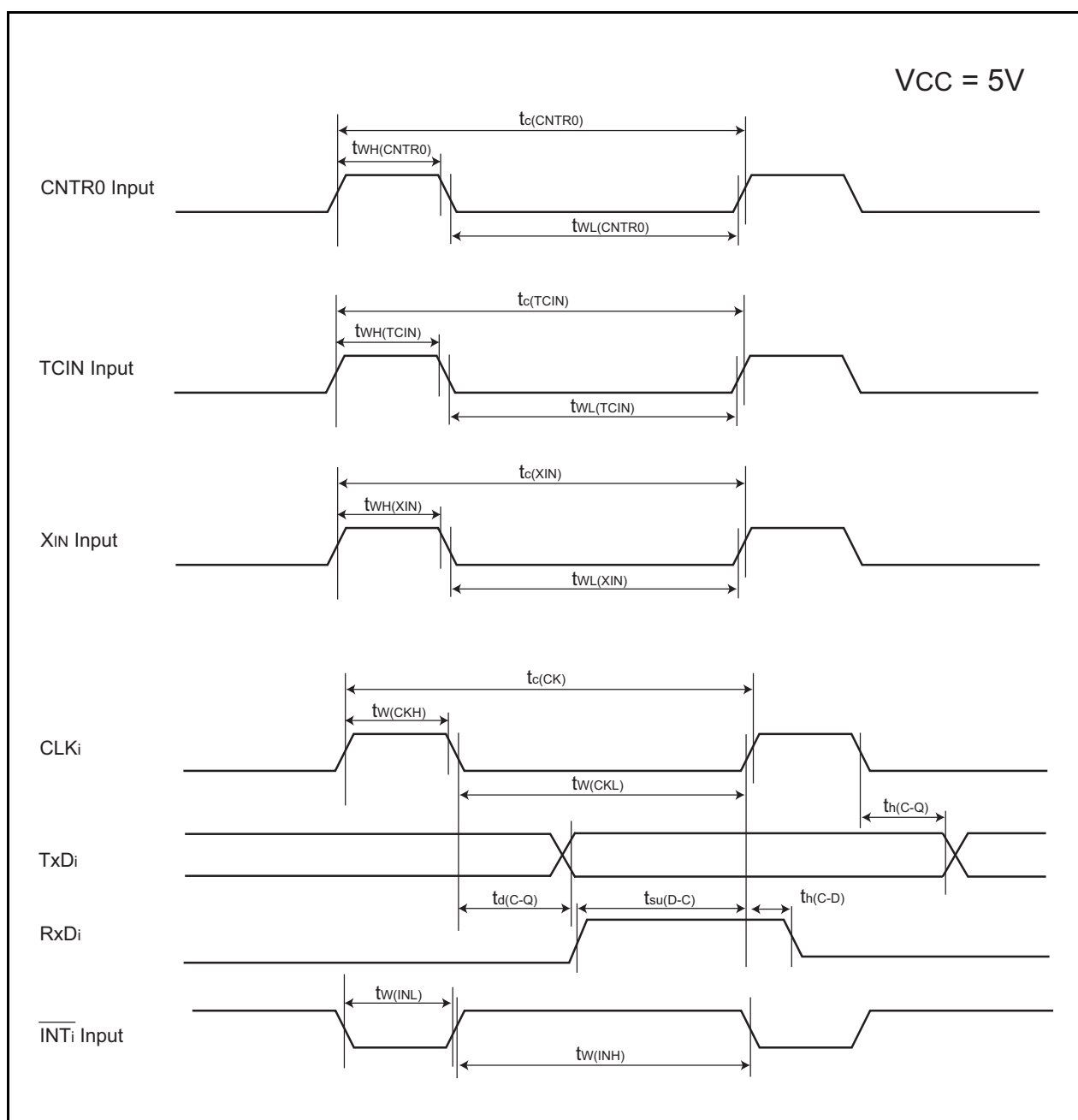
1. When not using the voltage monitor 1 reset, use with  $V_{cc} \geq 2.7\text{V}$ .
2.  $t_{w(por1)}$  is time to hold the external power below effective voltage ( $V_{por1}$ ).

**Figure 5.3 Reset Circuit Electrical Characteristics**



**Table 5.14 Electrical Characteristics (2) [Vcc = 5V] (Topr = -40 to 85 °C, unless otherwise specified.)**

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power Supply Current (Vcc=3.3 to 5.5V) In single-chip mode, the output pins are open and other pins are Vss	High-Speed Mode	XIN = 20MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz No division	–	9	15	mA
			XIN = 16MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz No division	–	8	14	mA
			XIN = 10MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz No division	–	5	–	mA
		Medium-Speed Mode	XIN = 20MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz Divide-by-8	–	4	–	mA
			XIN = 16MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz Divide-by-8	–	3	–	mA
			XIN = 10MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz Divide-by-8	–	2	–	mA
		High-Speed On-Chip Oscillator Mode	Main clock off High-speed on-chip oscillator on=8MHz Low-speed on-chip oscillator on=125kHz No division	–	4	8	mA
			Main clock off High-speed on-chip oscillator on=8MHz Low-speed on-chip oscillator on=125kHz Divide-by-8	–	1.5	–	mA
		Low-Speed On-Chip Oscillator Mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz Divide-by-8	–	470	900	μA
		Wait Mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz While a WAIT instruction is executed Peripheral clock operation VCA26 = VCA27 = 0	–	40	80	μA
		Wait Mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz While a WAIT instruction is executed Peripheral clock off VCA26 = VCA27 = 0	–	38	76	μA
		Stop Mode	Main clock off, Topr = 25 °C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA26 = VCA27 = 0	–	0.8	3.0	μA



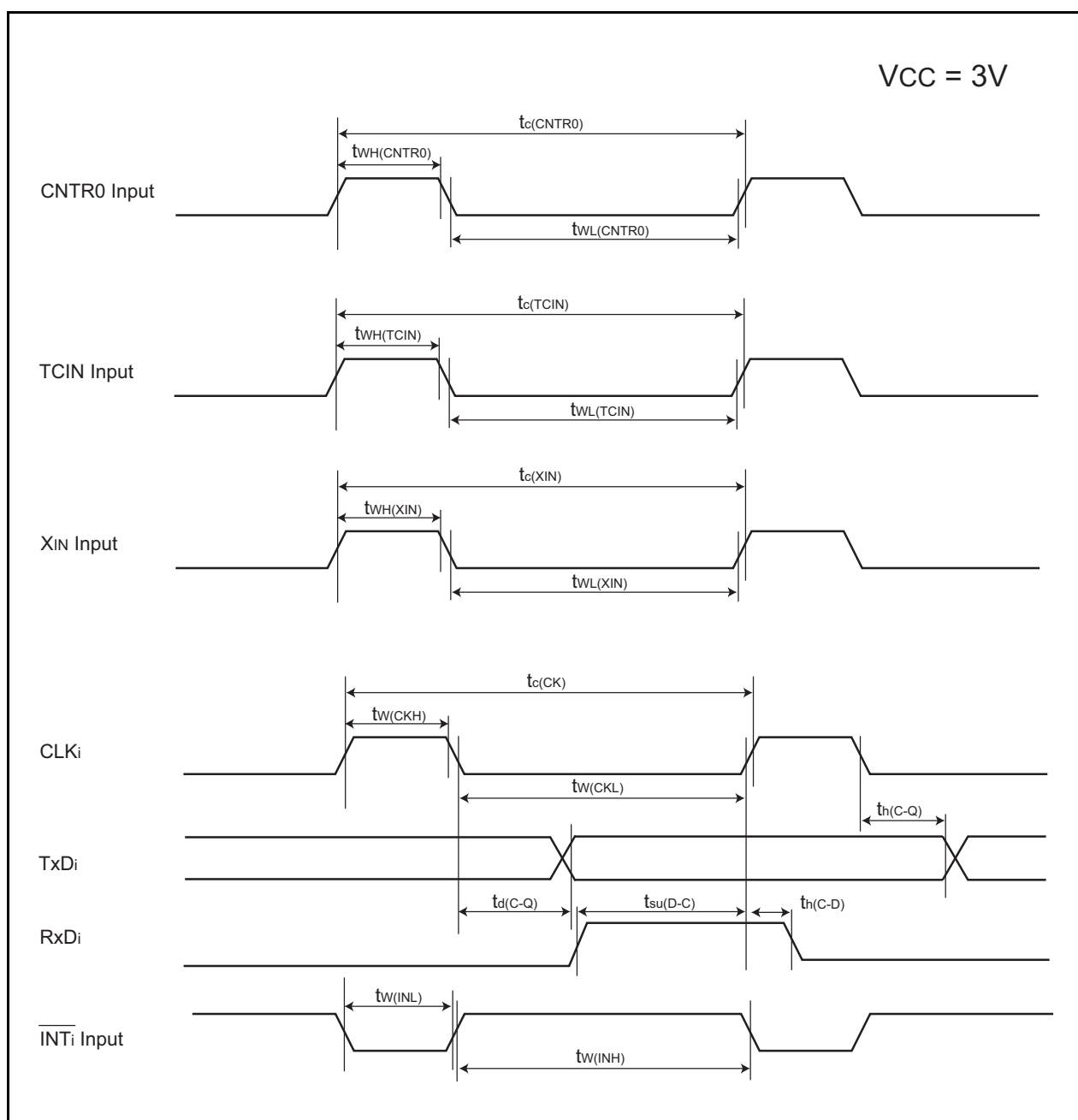
**Figure 5.5** Timing Diagram When  $V_{CC} = 5V$

**Table 5.20 Electrical Characteristics (3) [Vcc = 3V]**

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
VOH	Output "H" Voltage	Except XOUT	IOH = -1mA		Vcc - 0.5	—	Vcc	V
		XOUT	Drive capacity HIGH	IOH = -0.1mA	Vcc - 0.5	—	Vcc	V
			Drive capacity LOW	IOH = -50μA	Vcc - 0.5	—	Vcc	V
VOL	Output "L" Voltage	Except P1_0 to P1_3, XOUT	IOL = 1mA		—	—	0.5	V
		P1_0 to P1_3	Drive capacity HIGH	IOL = 2mA	—	—	0.5	V
			Drive capacity LOW	IOL = 1mA	—	—	0.5	V
		XOUT	Drive capacity HIGH	IOL = 0.1mA	—	—	0.5	V
			Drive capacity LOW	IOL = 50μA	—	—	0.5	V
VT+-VT-	Hysteresis	INT0, INT1, INT3, KI0, KI1, KI2, KI3, CNTR0, CNTR1, TCIN, RXD0			0.2	—	0.8	V
		RESET			0.2	—	1.8	V
IiH	Input "H" Current		VI = 3V		—	—	4.0	μA
IiL	Input "L" Current		VI = 0V		—	—	-4.0	μA
RPULLUP	Pull-Up Resistance		VI = 0V		66	160	500	kΩ
RfXIN	Feedback Resistance	XIN			—	3.0	—	MΩ
fRING-S	Low-Speed On-Chip Oscillator Frequency				40	125	250	kHz
VRAM	RAM Hold Voltage		During stop mode		2.0	—	—	V

## NOTES:

- Vcc = AVcc = 2.7 to 3.3V at Topr = -20 to 85 °C / -40 to 85 °C, f(XIN)=10MHz, unless otherwise specified.



**Figure 5.6** Timing Diagram When  $V_{CC} = 3V$

# REVISION HISTORY

# R8C/16 Group, R8C/17 Group Datasheet

Rev.	Date	Description	
		Page	Summary
2.00	Jan 30, 2006	8	Figure 1.5 PRDP0020BA-A Package Pin Assignment (top view) deleted Table 1.5 Pin Description; Timer C: "CMP0_0 to CMP0_3, CMP1_0 to CMP1_3" → "CMP0_0 to CMP0_2, CMP1_0 to CMP1_2" revised
		10	Figure 2.1 CPU Register; "Reserved Area" → "Reserved Bit" revised
		12	2.8.10 Reserved Area; "Reserved Area" → "Reserved Bit" revised
		13	Figure 3.1 Memory Map of R8C/16 Group revised
		14	3.2 R8C/17 Group; (program area) → (program ROM), (data area) → (data flash) revised Figure 3.2 Memory Map of R8C/17 Group revised
		17	Table 4.3 SFR Information(3); 0085h: "Prescaler Z" → "Prescaler Z Register" 0086h: "Timer Z Secondary" → "Timer Z Secondary Register" 0087h: "Timer Z Primary" → "Timer Z Primary Register" 008Ch: "Prescaler X" → "Prescaler X Register" 008Dh: "Timer X" → "Timer X Register" 0090h, 0091h: "Timer C" → "Timer C Register" revised
		21	Table 5.4 Flash Memory (Program ROM) Electrical Characteristics; • NOTES 1 to 7 added • "Topr" → "Ambient temperature", "(Program area)" → "(Program ROM)" revised
		22	Table 5.5 Flash Memory (Data flash Block A, Block B) Electrical Characteristics; • NOTE1 revised, NOTE9 added • "Topr" → "Ambient temperature", "(Program area)" → "(Program ROM)" revised
		23	Figure 5.2 Time delay from Suspend Request until Erase Suspend revised Table 5.7 Voltage Detection 2 Circuit Electrical Characteristics; NOTE1 revised
		24	Table 5.8 Reset Circuit Electrical Characteristics (When Using Voltage Monitor 1 Reset ); NOTE2 revised Table 5.9 Reset Circuit Electrical Characteristics (When Not Using Voltage Monitor 1 Reset); NOTE1 revised
		25	Table 5.10 High-speed On-Chip Oscillator Circuit Electrical Characteristics revised
		26	Table 5.12 Timing Requirements of I2C bus Interface (IIC); NOTE1 revised
		28	Table 5.14 Electrical Characteristics (2) [Vcc = 5V] revised
		29	"Timing Requirements (Unless ... at Ta = 25°C) [ VCC = 5V ]" → "Timing Requirements (Unless ... at Topr = 25°C) [ VCC = 5V ]" revised
		32	Table 5.18 Serial Interface; "35" → "50", "80" → "50"
		33	Table 5.21 Electrical Characteristics (4) [Vcc = 3V] revised "Timing requirements (Unless ... at Ta = 25°C) [VCC = 3V]" → "Timing requirements (Unless ... at Topr = 25°C) [VCC = 3V]" revised
		35	Table 5.25 Serial Interface; "55" → "70", "160" → "70"
			Package Dimensions; Package "PRDP0020BA-A" deleted