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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800E
Core Size	16-Bit
Speed	60MHz
Connectivity	CANbus, EBI/EMI, SCI, SPI
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	76
Program Memory Size	256KB (128K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	10K x 16
Voltage - Supply (Vcc/Vdd)	2.25V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	160-LQFP
Supplier Device Package	160-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f8357vpye

Document Revision History

Version History	Description of Change
Rev 1.0	Initial Public Release
Rev 2.0	Added Package Pins to GPIO Table in **Part 8 General Purpose Input/Output (GPIO)**. Added "Typical Min" values to **Table 10-17**. Editing grammar, spelling, consistency of language throughout family. Updated values in Regulator Parameters **Table 10-9**; External Clock Operation Timing Requirements **Table 10-13**; SPI Timing **Table 10-18**; ADC Parameters **Table 10-24**; and IO Loading Coefficients at 10MHz **Table 10-25**.
Rev 3.0	Corrected **Table 4-6** Data Memory Map - changed address X:$FF0000 to X:$FFFF00
Rev 4.0	Added **Part 4.8**, added the word "access" to FM Error Interrupt in **Table 4-5**, documenting only Typ. numbers for LVI in **Table 10-6**, updated EMI numbers and write-up in **Part 10.8**.
Rev 5.0	Updated numbers in **Table 10-7** and **Table 10-8** with more recent data. Corrected typo in **Table 10-3** in Pd characteristics.
Rev 6.0	Replace any reference to Flash Interface Unit with Flash Module; removed references to JTAG pin DE; corrected pin number for D14 in **Table 2-2**; added note to V_{CAP} pin in **Table 2-2**; corrected thermal numbers for 160 LQFP in **Table 10-3**; removed unneccessary notes in **Table 10-12**; corrected temperature range in **Table 10-14**; added ADC calibration information to **Table 10-24** and new graphs in **Figure 10-22**.
Rev 7.0	Adding/clarifing notes to **Table 4-4** to help clarify independent program flash blocks and other Program Flash modes, clarification in **Table 10-23**, corrected Digital Input Current Low (pull-up enabled) numbers in **Table 10-5**. Removed text and Table 10-2; replaced with note to **Table 10-1**.
Rev 8.0	Added 56F8157 information; edited to indicate differences in 56F8357 and 56F8157. Reformatted for Freescale look and feel. Updated Temperature Sensor and ADC tables, then updated balance of electrical tables for consistency throughout the family. Clarified I/O power description in **Table 2-2**, added note to **Table 10-7** and clarified **Section 12.3**.
Rev 9.0	Added output voltage maximum value and note to clarify in **Table 10-1**; also removed overall life expectancy note, since life expectancy is dependent on customer usage and must be determined by reliability engineering. Clarified value and unit measure for Maximum allowed P_D in **Table 10-3**. Corrected note about average value for Flash Data Retention in **Table 10-4**. Added new RoHS-compliant orderable part numbers in **Table 13-1**.
Rev 10.0	Added 160MAPBGA information,TA equation updated in **Table 10-4** and additional minor edits throughout data sheet
Rev 11.0	Updated **Table 10-24** to reflect new value for maximum Uncalibrated Gain Error
Rev. 12.0	Deleted formula for Max Ambient Operating Temperature (Automotive) and Max Ambient Operating Temperature (Industrial) in **Table 10-4**. Added RoHS-compliance and "pb-free" language to back cover.
Rev. 13.0	Corrected **Section 6.4** title (from Operation Mode Register to Operating Mode Register). Added information/corrected state during reset in **Table 2-2**. Clarified external reference crystal frequency for PLL in **Table 10-14** by increasing maximum value to 8.4MHz.
Rev. 14.0	Replaced "Tri-stated" with an explanation in State During Reset column in **Table 2-2**.

Table 2-2 Signal and Package Information for the 160-Pin LQFP and MBGA

Signal Name	Pin No.	*Ball No.*	Type	State During Reset	Signal Description
ANB0	116	C13	Input	Analog Input	**ANB0 - 3** — Analog inputs to ADC B, channel 0
ANB1	117	B14			
ANB2	118	C12			
ANB3	119	B13			
ANB4	120	A14	Input	Analog Input	**ANB4 - 7** — Analog inputs to ADC B, channel 1
ANB5	121	A13			
ANB6	122	B12			
ANB7	123	A12			
TEMP_ SENSE	108	E11	Output	Analog Output	**Temperature Sense Diode** — This signal connects to an on-chip diode that can be connected to one of the ADC inputs and used to monitor the temperature of the die. Must be bypassed with a 0.01μF capacitor.
CAN_RX	143	B7	Schmitt Input	Input, pull-up enabled	**FlexCAN Receive Data** — This is the CAN input. This pin has an internal pull-up resistor. To deactivate the internal pull-up resistor, set the CAN bit in the SIM_PUDR register.
CAN_TX	142	D6	Open Drain Output	Open Drain Output	**FlexCAN Transmit Data** — CAN output with internal pull-up enable at reset. * * **Note:** If a pin is configured as open drain output mode, internal pull-up will automatically be disabled when it outputs low. Internal pull-up will be enabled unless it has been manually disabled by clearing the corresponding bit in the PUREN register of the GPIO module, when it outputs high. If a pin is configured as push-pull output mode, internal pull-up will automatically be disabled, whether it outputs low or high.
TC0 **(GPIOE8)**	133	A9	Schmitt Input/ Output Schmitt Input/ Output	Input, pull-up enabled	**TC0** — Timer C, Channel 0 and 1 **Port E GPIO** — These GPIO pins can be individually programmed as input or output pins. At reset, these pins default to Timer functionality. To deactivate the internal pull-up resistor, clear the appropriate bit of the GPIOE_PUR register.
TC1 (GPIOE9)	135	B9			

crystal parameters determine the component values required to provide maximum stability and reliable start-up. The crystal and associated components should be mounted as near as possible to the EXTAL and XTAL pins to minimize output distortion and start-up stabilization time.

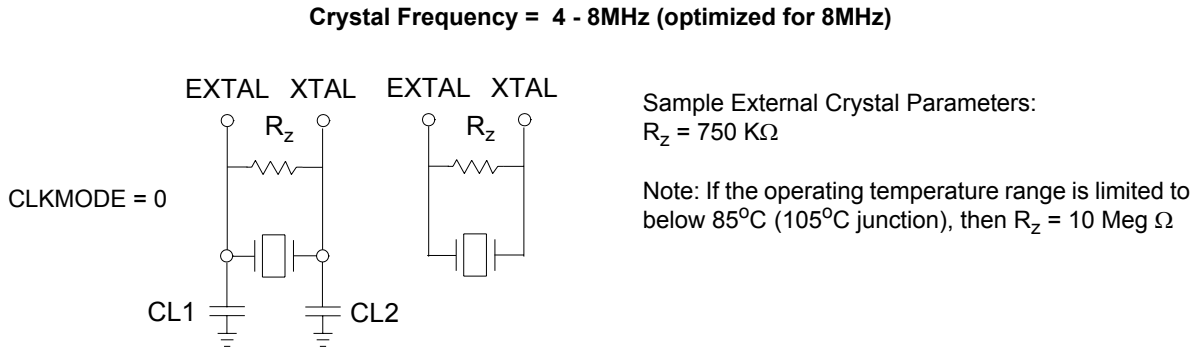


Figure 3-2 Connecting to a Crystal Oscillator

Note: The OCCS_COHL bit must be set to 1 when a crystal oscillator is used. The reset condition on the OCCS_COHL bit is 0. Please see the COHL bit in the Oscillator Control (OSCTL) register, discussed in the **56F8300 Peripheral User Manual**.

3.2.2 Ceramic Resonator (Default)

It is also possible to drive the internal oscillator with a ceramic resonator, assuming the overall system design can tolerate the reduced signal integrity. A typical ceramic resonator circuit is shown in **Figure 3-3**. Refer to the supplier's recommendations when selecting a ceramic resonator and associated components. The resonator and components should be mounted as near as possible to the EXTAL and XTAL pins.

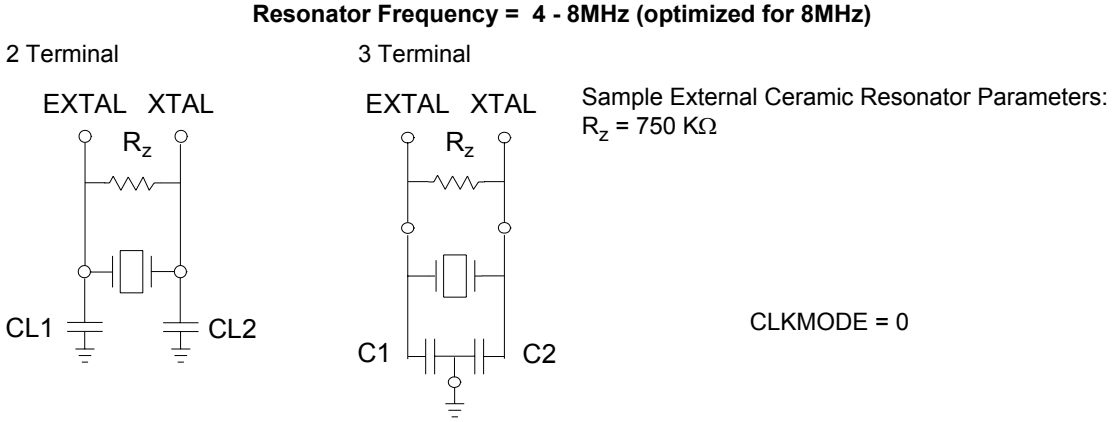


Figure 3-3 Connecting a Ceramic Resonator

Note: The OCCS_COHL bit must be set to 0 when a ceramic resonator is used. The reset condition on the OCCS_COHL bit is 0. Please see the COHL bit in the Oscillator Control (OSCTL) register, discussed in the **56F8300 Peripheral User Manual**.

Table 4-13 Quad Timer C Registers Address Map (Continued) (TMRC_BASE = $00 F0C0)

Register Acronym	Address Offset	Register Description
TMRC0_CTRL	$6	Control Register
TMRC0_SCR	$7	Status and Control Register
TMRC0_CMPLD1	$8	Comparator Load Register 1
TMRC0_CMPLD2	$9	Comparator Load Register 2
TMRC0_COMSCR	$A	Comparator Status and Control Register
		Reserved
TMRC1_CMP1	$10	Compare Register 1
TMRC1_CMP2	$11	Compare Register 2
TMRC1_CAP	$12	Capture Register
TMRC1_LOAD	$13	Load Register
TMRC1_HOLD	$14	Hold Register
TMRC1_CNTR	$15	Counter Register
TMRC1_CTRL	$16	Control Register
TMRC1_SCR	$17	Status and Control Register
TMRC1_CMPLD1	$18	Comparator Load Register 1
TMRC1_CMPLD2	$19	Comparator Load Register 2
TMRC1_COMSCR	$1A	Comparator Status and Control Register
		Reserved
TMRC2_CMP1	$20	Compare Register 1
TMRC2_CMP2	$21	Compare Register 2
TMRC2_CAP	$22	Capture Register
TMRC2_LOAD	$23	Load Register
TMRC2_HOLD	$24	Hold Register
TMRC2_CNTR	$25	Counter Register
TMRC2_CTRL	$26	Control Register
TMRC2_SCR	$27	Status and Control Register
TMRC2_CMPLD1	$28	Comparator Load Register 1
TMRC2_CMPLD2	$29	Comparator Load Register 2
TMRC2_COMSCR	$2A	Comparator Status and Control Register
		Reserved
TMRC3_CMP1	$30	Compare Register 1
TMRC3_CMP2	$31	Compare Register 2
TMRC3_CAP	$32	Capture Register
TMRC3_LOAD	$33	Load Register

Table 4-13 Quad Timer C Registers Address Map (Continued) (TMRC_BASE = $00 F0C0)

Register Acronym	Address Offset	Register Description
TMRC3_HOLD	$34	Hold Register
TMRC3_CNTR	$35	Counter Register
TMRC3_CTRL	$36	Control Register
TMRC3_SCR	$37	Status and Control Register
TMRC3_CMPLD1	$38	Comparator Load Register 1
TMRC3_CMPLD2	$39	Comparator Load Register 2
TMRC3_COMSCR	$3A	Comparator Status and Control Register

Table 4-14 Quad Timer D Registers Address Map (TMRD_BASE = $00 F100)

Quad Timer D is NOT available in the 56F8157 device

Register Acronym	Address Offset	Register Description
TMRD0_CMP1	$0	Compare Register 1
TMRD0_CMP2	$1	Compare Register 2
TMRD0_CAP	$2	Capture Register
TMRD0_LOAD	$3	Load Register
TMRD0_HOLD	$4	Hold Register
TMRD0_CNTR	$5	Counter Register
TMRD0_CTRL	$6	Control Register
TMRD0_SCR	$7	Status and Control Register
TMRD0_CMPLD1	$8	Comparator Load Register 1
TMRD0_CMPLD2	$9	Comparator Load Register 2
TMRD0_COMSCR	$A	Comparator Status and Control Register
		Reserved
TMRD1_CMP1	$10	Compare Register 1
TMRD1_CMP2	$11	Compare Register 2
TMRD1_CAP	$12	Capture Register
TMRD1_LOAD	$13	Load Register
TMRD1_HOLD	$14	Hold Register
TMRD1_CNTR	$15	Counter Register
TMRD1_CTRL	$16	Control Register
TMRD1_SCR	$17	Status and Control Register
TMRD1_CMPLD1	$18	Comparator Load Register 1
TMRD1_CMPLD2	$19	Comparator Load Register 2

5.6.2.1 Reserved—Bits 15–6

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.2.2 EOnCE Receive Register Full Interrupt Priority Level (RX_REG IPL)—Bits 5–4

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 1 through 3. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 1
- 10 = IRQ is priority level 2
- 11 = IRQ is priority level 3

5.6.2.3 EOnCE Transmit Register Empty Interrupt Priority Level (TX_REG IPL)—Bits 3–2

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 1 through 3. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 1
- 10 = IRQ is priority level 2
- 11 = IRQ is priority level 3

5.6.2.4 EOnCE Trace Buffer Interrupt Priority Level (TRBUF IPL)—Bits 1–0

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 1 through 3. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 1
- 10 = IRQ is priority level 2
- 11 = IRQ is priority level 3

5.6.3 Interrupt Priority Register 2 (IPR2)

Base + $2	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	FMCBE IPL		FMCC IPL		FMERR IPL		LOCK IPL		LVI IPL		0	0	IRQB IPL		IRQA IPL	
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-5 Interrupt Priority Register 2 (IPR2)

5.6.6.8 SPI0 Transmitter Empty Interrupt Priority Level (SPI_XMIT IPL)—Bits 1–0

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.7 Interrupt Priority Register 6 (IPR6)

Base + $6	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	TMRC0 IPL		TMRD3 IPL		TMRD2 IPL		TMRD1 IPL		TMRD0 IPL		0	0	DEC0_XIRQ IPL		DEC0_HIRQ IPL	
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-9 Interrupt Priority Register 6 (IPR6)

5.6.7.1 Timer C, Channel 0 Interrupt Priority Level (TMRC0 IPL)—Bits 15–14

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.7.2 Timer D, Channel 3 Interrupt Priority Level (TMRD3 IPL)—Bits 13–12

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.10.8 ADC B Conversion Complete Interrupt Priority Level (ADCB_CC IPL)—Bits 1–0

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.11 Vector Base Address Register (VBA)

Base + $A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	VECTOR BASE ADDRESS												
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-13 Vector Base Address Register (VBA)

5.6.11.1 Reserved—Bits 15–13

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.11.2 Interrupt Vector Base Address (VECTOR BASE ADDRESS)—Bits 12–0

The contents of this register determine the location of the Vector Address Table. The value in this register is used as the upper 13 bits of the interrupt Vector Address Bus (VAB[20:0]). The lower eight bits are determined based upon the highest-priority interrupt. They are then appended onto VBA before presenting the full VAB to the 56800E core; see **Part 5.3.1** for details.

5.6.12 Fast Interrupt 0 Match Register (FIM0)

Base + $B	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 0						
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-14 Fast Interrupt 0 Match Register (FIM0)

5.6.12.1 Reserved—Bits 15–7

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.12.2 Fast Interrupt 0 Vector Number (FAST INTERRUPT 0)—Bits 6–0

This value determines which IRQ will be a Fast Interrupt 0. Fast interrupts vector directly to a service routine based on values in the Fast Interrupt Vector Address registers without having to go to a jump table first; see **Part 5.3.3**. IRQs used as fast interrupts *must* be set to priority level 2. Unexpected results will occur if a fast interrupt vector is set to any other priority. Fast interrupts automatically become the

5.6.18 IRQ Pending 0 Register (IRQP0)

Base + $11	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	PENDING [16:2]															1
Write																
RESET	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Figure 5-20 IRQ Pending 0 Register (IRQP0)

5.6.18.1 IRQ Pending (PENDING)—Bits 16–2

This register combines with the other five to represent the pending IRQs for interrupt vector numbers 2 through 81.

- 0 = IRQ pending for this vector number
- 1 = No IRQ pending for this vector number

5.6.18.2 Reserved—Bit 0

This bit is reserved or not implemented. It is read as 1 and cannot be modified by writing.

5.6.19 IRQ Pending 1 Register (IRQP1)

$Base + $12	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	PENDING [32:17]															
Write																
RESET	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Figure 5-21 IRQ Pending 1 Register (IRQP1)

5.6.19.1 IRQ Pending (PENDING)—Bits 32–17

This register combines with the other five to represent the pending IRQs for interrupt vector numbers 2 through 81.

- 0 = IRQ pending for this vector number
- 1 = No IRQ pending for this vector number

5.6.20 IRQ Pending 2 Register (IRQP2)

Base + $13	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	PENDING [48:33]															
Write																
RESET	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Figure 5-22 IRQ Pending 2 Register (IRQP2)

6.5 Register Descriptions

Table 6-1 SIM Registers (SIM_BASE = $00 F350)

Address Offset	Address Acronym	Register Name	Section Location
Base + $0	SIM_CONTROL	Control Register	6.5.1
Base + $1	SIM_RSTSTS	Reset Status Register	6.5.2
Base + $2	SIM_SCR0	Software Control Register 0	6.5.3
Base + $3	SIM_SCR1	Software Control Register 1	6.5.3
Base + $4	SIM_SCR2	Software Control Register 2	6.5.3
Base + $5	SIM_SCR3	Software Control Register 3	6.5.3
Base + $6	SIM_MSH_ID	Most Significant Half of JTAG ID	6.5.4
Base + $7	SIM_LSH_ID	Least Significant Half of JTAG ID	6.5.5
Base + $8	SIM_PUDR	Pull-up Disable Register	6.5.6
		Reserved	
Base + $A	SIM_CLKOSR	CLKO Select Register	6.5.7
Base + $B	SIM_GPS	GPIO Peripheral Select Register	6.5.8
Base + $C	SIM_PCE	Peripheral Clock Enable Register	6.5.9
Base + $D	SIM_ISALH	I/O Short Address Location High Register	6.5.10
Base + $E	SIM_ISALL	I/O Short Address Location Low Register	6.5.10

6.5.1.2 EMI_MODE (EMI_MODE)—Bit 6

This bit reflects the current (non-clocked) state of the EMI_MODE pin. During reset, this bit, coupled with the EXTBOOT signal, is used to initialize address bits [19:16] either as GPIO or as address. These settings can be explicitly overwritten using the appropriate GPIO peripheral enable register at any time after reset. In addition, this pin can be used as a general purpose input pin after reset.

- 0 = External address bits [19:16] are initially programmed as GPIO
- 1 = When booted with EXTBOOT = 1, A[19:16] are initially programmed as address. If EXTBOOT is 0, they are initialized as GPIO.

6.5.1.3 OnCE Enable (OnCE EBL)—Bit 5

- 0 = OnCE clock to 56800E core enabled when core TAP is enabled
- 1 = OnCE clock to 56800E core is always enabled

6.5.1.4 Software Reset (SW RST)—Bit 4

This bit is always read as 0. Writing a 1 to this bit will cause the part to reset.

6.5.1.5 Stop Disable (STOP_DISABLE)—Bits 3–2

- 00 - Stop mode will be entered when the 56800E core executes a STOP instruction
- 01 - The 56800E STOP instruction will not cause entry into Stop mode; STOP_DISABLE can be reprogrammed in the future
- 10 - The 56800E STOP instruction will not cause entry into Stop mode; STOP_DISABLE can then only be changed by resetting the device
- 11 - Same operation as 10

6.5.1.6 Wait Disable (WAIT_DISABLE)—Bits 1–0

- 00 - Wait mode will be entered when the 56800E core executes a WAIT instruction
- 01 - The 56800E WAIT instruction will not cause entry into Wait mode; WAIT_DISABLE can be reprogrammed in the future
- 10 - The HawkV2 WAIT instruction will not cause entry into Wait mode; WAIT_DISABLE can then only be changed by resetting the device
- 11 - Same operation as 10

6.5.2 SIM Reset Status Register (SIM_RSTSTS)

Bits in this register are set upon any system reset and are initialized only by a Power-On Reset (POR). A reset (other than POR) will only set bits in the register; bits are not cleared. Only software should clear this register.

Base + $1	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	O	0	0	0	0	0	0	0	SWR	COPR	EXTR	POR	0	0
Write																
RESET	0	0	0	0	0	0	0	0	0	0					0	0

Figure 6-4 SIM Reset Status Register (SIM_RSTSTS)

Base + $C	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read Write	EMI	ADCB	ADCA	CAN	DEC1	DEC0	TMRD	TMRC	TMRB	TMRA	SCI 1	SCI 0	SPI 1	SPI 0	PWMB	PWMA
RESET	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Figure 6-12 Peripheral Clock Enable Register (SIM_PCE)

6.5.9.1 External Memory Interface Enable (EMI)—Bit 15

Each bit controls clocks to the indicated peripheral.

- 1 = Clocks are enabled
- 0 = The clock is not provided to the peripheral (the peripheral is disabled)

6.5.9.2 Analog-to-Digital Converter B Enable (ADCB)—Bit 14

Each bit controls clocks to the indicated peripheral.

- 1 = Clocks are enabled
- 0 = The clock is not provided to the peripheral (the peripheral is disabled)

6.5.9.3 Analog-to-Digital Converter A Enable (ADCA)—Bit 13

Each bit controls clocks to the indicated peripheral.

- 1 = Clocks are enabled
- 0 = The clock is not provided to the peripheral (the peripheral is disabled)

6.5.9.4 FlexCAN Enable (CAN)—Bit 12

Each bit controls clocks to the indicated peripheral.

- 1 = Clocks are enabled
- 0 = The clock is not provided to the peripheral (the peripheral is disabled)

6.5.9.5 Decoder 1 Enable (DEC1)—Bit 11

Each bit controls clocks to the indicated peripheral.

- 1 = Clocks are enabled
- 0 = The clock is not provided to the peripheral (the peripheral is disabled)

6.5.9.6 Decoder 0 Enable (DEC0)—Bit 10

Each bit controls clocks to the indicated peripheral.

- 1 = Clocks are enabled
- 0 = The clock is not provided to the peripheral (the peripheral is disabled)

Table 8-1 56F8357 GPIO Ports Configuration

GPIO Port	Port Width	Available Pins in 56F8347	Peripheral Function	Reset Function
A	14	14	14 pins - EMI Address pins	EMI Address
B	8	8	8 pins - EMI Address pins	EMI Address
C	11	11	4 pins -DEC1 / TMRB / SPI1 4 pins -DEC0 / TMRA 3 pins -PWMA current sense	DEC1 / TMRB DEC0 / TMRA PWMA current sense
D	13	13	6 pins - EMI $\overline{CSn}$ 2 pins - SCI1 2 pins - EMI $\overline{CSn}$ 3 pins -PWMB current sense	EMI Chip Selects SCI1 EMI Chip Selects PWMB current sense
E	14	14	2 pins - SCI0 2 pins - EMI Address pins 4 pins - SPI0 2 pins - TMRC 4 pins - TMRD	SCI0 EMI Address SPI0 TMRC TMRD
F	16	16	16 pins - EMI Data	EMI Data

Table 8-2 56F8157 GPIO Ports Configuration

GPIO Port	Port Width	Available Pins in 56F8157	Peripheral Function	Reset Function
A	14	14	14 pins - EMI Address pins	EMI Address
B	8	8	8 pins - EMI Address pins	EMI Address
C	11	11	4 pins - SPI1 4 pins - DEC0 / TMRA 3 pins - Dedicated GPIO	SPI1 DEC0 / TMRA GPIO
D	13	13	6 pins - EMI $\overline{CSn}$ 2 pins - SCI1 2 pins - EMI $\overline{CSn}$ 3 pins -PWMB current sense	EMI Chip Selects SCI1 EMI Chip Selects PWMB current sense
E	14	14	2 pins - SCI0 2 pins - EMI Address pins 4 pins - SPI0 2 pins - TMRC 4 pins - Dedicated GPIO	SCI0 EMI Address SPI0 TMRC GPIO
F	16	16	16 pins - EMI Data	EMI Data

10.2 DC Electrical Characteristics

Note: *The 56F8157 device is specified to meet Industrial requirements only; CAN is NOT available on the 56F8157 device.*

Table 10-5 DC Electrical Characteristics

At Recommended Operating Conditions; see Table 10-4

Characteristic	Symbol	Notes	Min	Typ	Max	Unit	Test Conditions
Output High Voltage	V_{OH}		2.4	—	—	V	$I_{OH} = I_{OHmax}$
Output Low Voltage	V_{OL}		—	—	0.4	V	$I_{OL} = I_{OLmax}$
Digital Input Current High pull-up enabled or disabled	I_{IH}	Pin Groups 1, 2, 5, 6, 9,	—	0	+/- 2.5	µA	V_{IN} = 3.0V to 5.5V
Digital Input Current High with pull-down	I_{IH}	Pin Group 10	40	80	160	µA	V_{IN} = 3.0V to 5.5V
Analog Input Current High	I_{IHA}	Pin Group 13	—	0	+/- 2.5	µA	$V_{IN} = V_{DDA}$
ADC Input Current High	I_{IHADC}	Pin Group 12	—	0	+/- 10	µA	$V_{IN} = V_{DDA}$
Digital Input Current Low pull-up enabled	I_{IL}	Pin Groups 1, 2, 5, 6, 9,	-200	-100	-50	µA	V_{IN} = 0V
Digital Input Current Low pull-up disabled	I_{IL}	Pin Groups 1, 2, 5, 6, 9,	—	0	+/- 2.5	µA	V_{IN} = 0V
Digital Input Current Low with pull-down	I_{IL}	Pin Group 10	—	0	+/- 2.5	µA	V_{IN} = 0V
Analog Input Current Low	I_{ILA}	Pin Group 13	—	0	+/- 2.5	µA	V_{IN} = 0V
ADC Input Current Low	I_{ILADC}	Pin Group 12	—	0	+/- 10	µA	V_{IN} = 0V
EXTAL Input Current Low clock input	I_{EXTAL}		—	0	+/- 2.5	µA	$V_{IN} = V_{DDA}$ or 0V
XTAL Input Current Low clock input	I_{XTAL}	CLKMODE = High	—	0	+/- 2.5	µA	$V_{IN} = V_{DDA}$ or 0V
		CLKMODE = Low	—	—	200	µA	$V_{IN} = V_{DDA}$ or 0V
Output Current High Impedance State	I_{OZ}	Pin Groups 1, 2, 3, 4, 5, 6, 7, 8	—	0	+/- 2.5	µA	V_{OUT} = 3.0V to 5.5V or 0V
Schmitt Trigger Input Hysteresis	V_{HYS}	Pin Groups 2, 6, 9, 10	—	0.3	—	V	—
Input Capacitance (EXTAL/XTAL)	C_{INC}		—	4.5	—	pF	—
Output Capacitance (EXTAL/XTAL)	C_{OUTC}		—	5.5	—	pF	—
Input Capacitance	C_{IN}		—	6	—	pF	—
Output Capacitance	C_{OUT}		—	6	—	pF	—

See Pin Groups in Table 10-1.

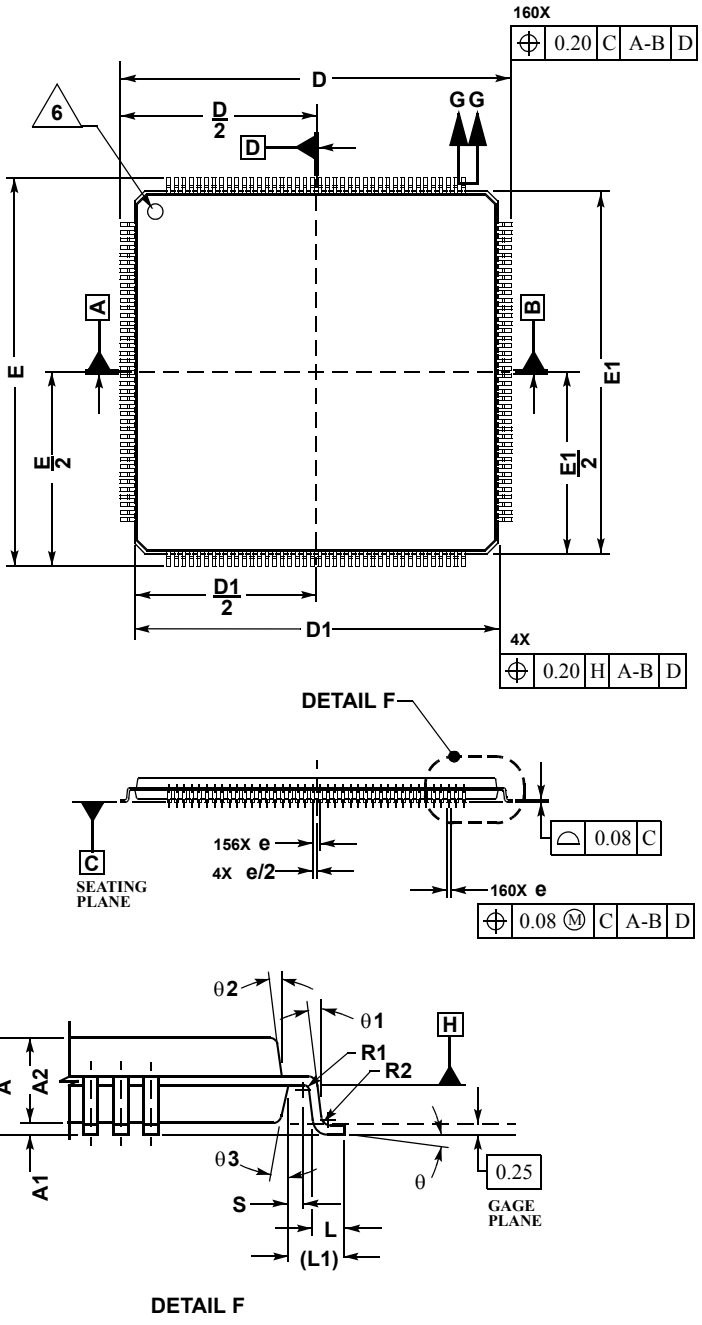
Table 11-2 56F8357 -160 MAPBGA Package Identification by Pin Number

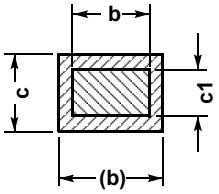
Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name
F4	V_{DD_IO}	K11	V_{SS}	N12	PWMA5	A13	ANB5
C2	$V_{PP}2$	K7	V_{DD_IO}	N13	FAULTA0	B12	ANB6
D3	CLKO	N3	PWMB3	P14	D2	A12	ANB7
B1	TXD0	P2	PWMB4	N14	FAULTA1	B11	EXTBOOT
D2	RXD0	M3	PWMB5	M13	FAULTA2	J11	V_{SS}
C1	PHASEA1	N4	GPIOB5	L13	D3	A11	ISA0
D1	PHASEB1	P3	GPIOB6	M14	FAULTA3	C11	ISA1
E2	INDEX1	M4	GPIOB7	L14	D4	D11	ISA2
E1	HOME1	P4	TXD1	L12	D5	B10	TD0
E3	A1	N5	RXD1	L11	D6	A10	TD1
E4	A2	L4	$\overline{WR}$	K14	OCR_DIS	D10	TD2
F2	A3	P5	$\overline{RD}$	K13	$V_{DDA\_OSC\_PLL}$	E10	TD3
F1	A4	N6	$\overline{PS}$	K12	XTAL	A9	TC0
F3	A5	L5	$\overline{DS}$	J12	EXTAL	F11	V_{DD_IO}
G4	$V_{CAP}4$*	P6	GPIOD0	H11	$V_{CAP}3$*	B9	TC1
K5	V_{DD_IO}	L6	GPIOD1	K10	V_{DD_IO}	D9	$\overline{TRST}$
G1	A6	K6	GPIOD2	J13	$\overline{RSTO}$	D8	TCK
G3	A7	N7	GPIOD3	J14	$\overline{RESET}$	A8	TMS
G2	A8	P7	GPIOD4	H12	CLKMODE	B8	TDI
H1	A9	L7	GPIOD5	G13	ANA0	D7	TDO
H2	A10	N8	ISB0	H13	ANA1	A7	$V_{PP}1$
H4	A11	K8	$V_{CAP}1$*	G12	ANA2	D6	CAN_TX
H3	A12	L8	ISB1	F13	ANA3	B7	CAN_RX
J1	A13	P8	ISB2	F12	ANA4	E8	$V_{CAP}2$*
J2	A14	K9	$\overline{IRQA}$	H14	ANA5	D5	$\overline{SS0}$

* When the on-chip regulator is disabled, these four pins become 2.5V V_{DD_CORE}.

Table 11-3 56F8157 160-Pin LQFP Package Identification by Pin Number (Continued)

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
26	A15	66	$\overline{\text{IRQB}}$	106	ANA6	146	SCLK0
27	V_{SS}	67	FAULTB0	107	ANA7	147	MISO0
28	D7	68	FAULTB1	108	NC	148	MOSI0
29	D8	69	FAULTB2	109	V_{REFLO}	149	D11
30	D9	70	D0	110	V_{REFN}	150	D12
31	V_{DD_IO}	71	D1	111	V_{REFMID}	151	D13
32	D10	72	FAULTB3	112	V_{REFP}	152	D14
33	GPIOB0	73	NC	113	V_{REFH}	153	D15
34	GPIOB1	74	V_{SS}	114	V_{DDA_ADC}	154	A0
35	GPIOB2	75	NC	115	V_{SSA_ADC}	155	PHASEA0
36	GPIOB3	76	NC	116	ANB0	156	PHASEB0
37	GPIOB4	77	V_{DD_IO}	117	ANB1	157	INDEX0
38	PWMB0	78	NC	118	ANB2	158	HOME0
39	PWMB1	79	NC	119	ANB3	159	EMI_MODE
40	PWMB2	80	V_{SS}	120	ANB4	160	V_{SS}





SECTION G-G

NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUMS A, B, AND D TO BE DETERMINED WHERE THE LEADS EXIT THE PLASTIC BODY AT DATUM PLANE H.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. DIMENSIONS D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN A PROTRUSION AND AN ADJACENT LEAD IS 0.07mm.
6. EXACT SHAPE OF CORNERS MAY VARY.

	MILLIMETERS	
DIM	MIN	MAX
A	---	1.60
A1	0.05	0.15
A2	1.35	1.45
b	0.17	0.27
b1	0.17	0.23
c	0.09	0.20
c1	0.09	0.16
D	26.00 BSC	
D1	24.00 BSC	
e	0.50 BSC	
E	26.00 BSC	
E1	24.00 BSC	
L	0.45	0.75
L1	1.00 REF	
R1	0.08	---
R2	0.08	0.20
S	0.20	---
θ	0°	7°
θ1	0°	---
θ2	11°	13°
θ3	11°	13°

Figure 11-5 160-pin LQFP Mechanical Information

Part 12 Design Considerations

12.1 Thermal Design Considerations

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$T_J = T_A + (R_{\theta JA} \times P_D)$

where:

T_A = Ambient temperature for the package (^oC)
$R_{\theta JA}$ = Junction-to-ambient thermal resistance ($^oC/W$)
P_D = Power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry-standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single-layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single-layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low-power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

where:

$R_{\theta JA}$ = Package junction-to-ambient thermal resistance °C/W
$R_{\theta JC}$ = Package junction-to-case thermal resistance °C/W
$R_{\theta CA}$ = Package case-to-ambient thermal resistance °C/W

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$T_J = T_T + (\Psi_{JT} \times P_D)$

where:

T_T = Thermocouple temperature on top of package (^oC)
Ψ_{JT} = Thermal characterization parameter (^oC)/W
P_D = Power dissipation in package (W)

Part 13 Ordering Information

Table 13-1 lists the pertinent information needed to place an order. Consult a Freescale Semiconductor sales office or authorized distributor to determine availability and to order parts.

Table 13-1 Ordering Information

Part	Supply Voltage	Package Type	Pin Count	Frequency (MHz)	Ambient Temperature Range	Order Number
MC56F8357	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	160	60	-40° to + 105° C	MC56F8357VPY60
MC56F8157	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	160	60	-40° to + 105° C	MC56F8157VPY
MC56F8357	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	160	60	-40° to + 105° C	MC56F8357VPYE*
MC56F8357	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	160	60	-40° to + 125° C	MC56F8357MPYE*
MC56F8157	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	160	60	-40° to + 105° C	MC56F8157VPYE*
MC56F8357	3.0–3.6 V	Mold Array Process Ball Grid Array (MAPBGA)	160	60	-40° to + 105° C	MC56F8357VVF*

*This package is RoHS compliant.