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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	56800E
Core Size	16-Bit
Speed	60MHz
Connectivity	CANbus, EBI/EMI, SCI, SPI
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	76
Program Memory Size	256KB (128K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	10K x 16
Voltage - Supply (Vcc/Vdd)	2.25V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	160-BGA
Supplier Device Package	160-MAPBGA (15x15)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc56f8357vvfe

Document Revision History

Version History	Description of Change
Rev 1.0	Initial Public Release
Rev 2.0	Added Package Pins to GPIO Table in **Part 8 General Purpose Input/Output (GPIO)**. Added "Typical Min" values to **Table 10-17**. Editing grammar, spelling, consistency of language throughout family. Updated values in Regulator Parameters **Table 10-9**; External Clock Operation Timing Requirements **Table 10-13**; SPI Timing **Table 10-18**; ADC Parameters **Table 10-24**; and IO Loading Coefficients at 10MHz **Table 10-25**.
Rev 3.0	Corrected **Table 4-6** Data Memory Map - changed address X:$FF0000 to X:$FFFF00
Rev 4.0	Added **Part 4.8**, added the word "access" to FM Error Interrupt in **Table 4-5**, documenting only Typ. numbers for LVI in **Table 10-6**, updated EMI numbers and write-up in **Part 10.8**.
Rev 5.0	Updated numbers in **Table 10-7** and **Table 10-8** with more recent data. Corrected typo in **Table 10-3** in Pd characteristics.
Rev 6.0	Replace any reference to Flash Interface Unit with Flash Module; removed references to JTAG pin DE; corrected pin number for D14 in **Table 2-2**; added note to V_{CAP} pin in **Table 2-2**; corrected thermal numbers for 160 LQFP in **Table 10-3**; removed unneccessary notes in **Table 10-12**; corrected temperature range in **Table 10-14**; added ADC calibration information to **Table 10-24** and new graphs in **Figure 10-22**.
Rev 7.0	Adding/clarifing notes to **Table 4-4** to help clarify independent program flash blocks and other Program Flash modes, clarification in **Table 10-23**, corrected Digital Input Current Low (pull-up enabled) numbers in **Table 10-5**. Removed text and Table 10-2; replaced with note to **Table 10-1**.
Rev 8.0	Added 56F8157 information; edited to indicate differences in 56F8357 and 56F8157. Reformatted for Freescale look and feel. Updated Temperature Sensor and ADC tables, then updated balance of electrical tables for consistency throughout the family. Clarified I/O power description in **Table 2-2**, added note to **Table 10-7** and clarified **Section 12.3**.
Rev 9.0	Added output voltage maximum value and note to clarify in **Table 10-1**; also removed overall life expectancy note, since life expectancy is dependent on customer usage and must be determined by reliability engineering. Clarified value and unit measure for Maximum allowed P_D in **Table 10-3**. Corrected note about average value for Flash Data Retention in **Table 10-4**. Added new RoHS-compliant orderable part numbers in **Table 13-1**.
Rev 10.0	Added 160MAPBGA information,TA equation updated in **Table 10-4** and additional minor edits throughout data sheet
Rev 11.0	Updated **Table 10-24** to reflect new value for maximum Uncalibrated Gain Error
Rev. 12.0	Deleted formula for Max Ambient Operating Temperature (Automotive) and Max Ambient Operating Temperature (Industrial) in **Table 10-4**. Added RoHS-compliance and "pb-free" language to back cover.
Rev. 13.0	Corrected **Section 6.4** title (from Operation Mode Register to Operating Mode Register). Added information/corrected state during reset in **Table 2-2**. Clarified external reference crystal frequency for PLL in **Table 10-14** by increasing maximum value to 8.4MHz.
Rev. 14.0	Replaced "Tri-stated" with an explanation in State During Reset column in **Table 2-2**.

1.2.1 56F8357 Features

The 56F8357 controller includes 256KB of Program Flash and 8KB of Data Flash (each programmable through the JTAG port) with 4KB of Program RAM and 16KB of Data RAM. It also supports program execution from external memory.

A total of 16KB of Boot Flash is incorporated for easy customer inclusion of field-programmable software routines that can be used to program the main Program and Data Flash memory areas. Both Program and Data Flash memories can be independently bulk erased or erased in pages. Program Flash page erase size is 1KB. Boot and Data Flash page erase size is 512 bytes. The Boot Flash memory can also be either bulk or page erased.

A key application-specific feature of the 56F8357 is the inclusion of two Pulse Width Modulator (PWM) modules. These modules each incorporate three complementary, individually programmable PWM signal output pairs (each module is also capable of supporting six independent PWM functions, for a total of 12 PWM outputs) to enhance motor control functionality. Complementary operation permits programmable dead time insertion, distortion correction via current sensing by software, and separate top and bottom output polarity control. The up-counter value is programmable to support a continuously variable PWM frequency. Edge-aligned and center-aligned synchronous pulse width control (0% to 100% modulation) is supported. The device is capable of controlling most motor types: ACIM (AC Induction Motors); both BDC and BLDC (Brush and Brushless DC motors); SRM and VRM (Switched and Variable Reluctance Motors); and stepper motors. The PWMs incorporate fault protection and cycle-by-cycle current limiting with sufficient output drive capability to directly drive standard optoisolators. A “smoke-inhibit”, write-once protection feature for key parameters is also included. A patented PWM waveform distortion correction circuit is also provided. Each PWM is double-buffered and includes interrupt controls to permit integral reload rates to be programmable from 1 to 16. The PWM modules provide a reference output to synchronize the Analog-to-Digital Converters through two channels of Quad Timer C.

The 56F8357 incorporates two Quadrature Decoders capable of capturing all four transitions on the two-phase inputs, permitting generation of a number proportional to actual position. Speed computation capabilities accommodate both fast- and slow-moving shafts. An integrated watchdog timer in the Quadrature Decoder can be programmed with a time-out value to alarm when no shaft motion is detected. Each input is filtered to ensure only true transitions are recorded.

This controller also provides a full set of standard programmable peripherals that include two Serial Communications Interfaces (SCIs); two Serial Peripheral Interfaces (SPIs); and four Quad Timers. Any of these interfaces can be used as General Purpose Input/Outputs (GPIOs) if that function is not required. A Flex Controller Area Network (FlexCAN) interface (CAN Version 2.0 B-compliant) and an internal interrupt controller are a part of the 56F8357.

1.2.2 56F8157 Features

The 56F8157 controller includes 256KB of Program Flash, programmable through the JTAG port, with 16KB of Data RAM. It also supports program execution from external memory.

A total of 16KB of Boot Flash is incorporated for easy customer inclusion of field-programmable software routines that can be used to program the main Program Flash memory area, which can be independently bulk erased or erased in pages. Program Flash page erase size is 1KB. Boot Flash page erase size is 512 bytes and the Boot Flash memory can also be either bulk or page erased.

Table 1-2 Bus Signal Names

Name	Function
Program Memory Interface	
pdb_m[15:0]	Program data bus for instruction word fetches or read operations.
cdbw[15:0]	Primary core data bus used for program memory writes. (Only these 16 bits of the cdbw[31:0] bus are used for writes to program memory.)
pab[20:0]	Program memory address bus. Data is returned on pdb_m bus.
Primary Data Memory Interface Bus	
cdbr_m[31:0]	Primary core data bus for memory reads. Addressed via xab1 bus.
cdbw[31:0]	Primary core data bus for memory writes. Addressed via xab1 bus.
xab1[23:0]	Primary data address bus. Capable of addressing bytes[1], words, and long data types. Data is written on cdbw and returned on cdbr_m. Also used to access memory-mapped I/O.
Secondary Data Memory Interface	
xdb2_m[15:0]	Secondary data bus used for secondary data address bus xab2 in the dual memory reads.
xab2[23:0]	Secondary data address bus used for the second of two simultaneous accesses. Capable of addressing only words. Data is returned on xdb2_m.
Peripheral Interface Bus	
IPBus [15:0]	Peripheral bus accesses all on-chip peripherals registers. This bus operates at the same clock rate as the Primary Data Memory and therefore generates no delays when accessing the processor. Write data is obtained from cdbw. Read data is provided to cdbr_m.

1. Byte accesses can only occur in the bottom half of the memory address space. The MSB of the address will be forced to 0.

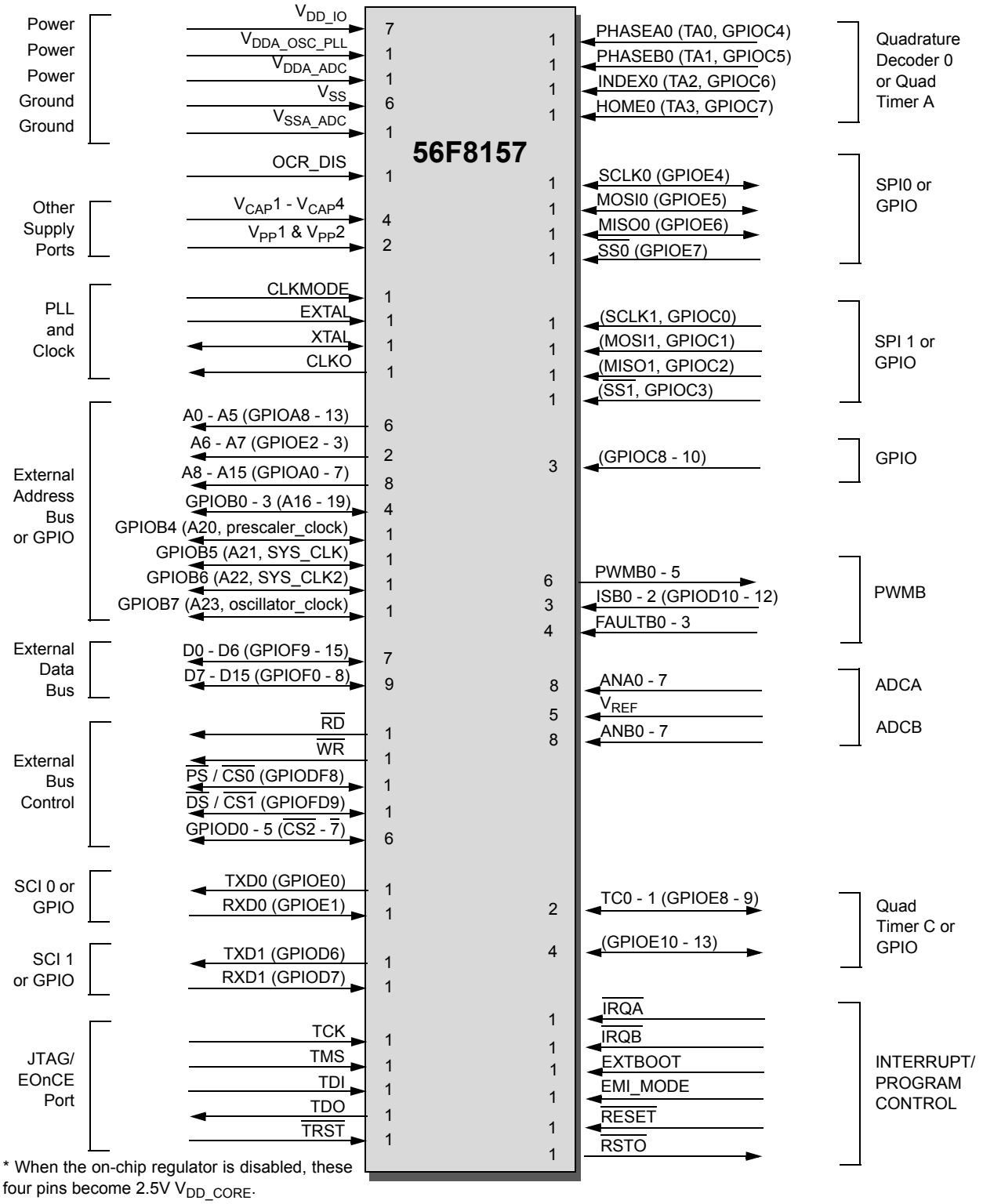


Figure 2-2 56F8157 Signals Identified by Functional Group[1] (160-pin LQFP)

1. Alternate pin functionality is shown in parenthesis; pin direction/type shown is the default functionality.

Table 2-2 Signal and Package Information for the 160-Pin LQFP and MBGA

Signal Name	Pin No.	*Ball No.*	Type	State During Reset	Signal Description
GPIOD0 **($\overline{CS2}$)**	55	P6	Input/ Output Output	Input, pull-up enabled	**Port D GPIO** — These six GPIO pins can be individually programmed as input or output pins. **Chip Select** — $\overline{CS2}$ - $\overline{CS7}$ may be programmed within the EMI module to act as chip selects for specific areas of the external memory map. Depending upon the state of the DRV bit in the EMI Bus Control Register (BCR), $\overline{CS2}$ - $\overline{CS7}$ are tri-stated when the external bus is inactive. Most designs will want to change the DRV state to DRV = 1 instead of using the default setting. At reset, these pins are configured as GPIO. To deactivate the internal pull-up resistor, clear the appropriate GPIO bit in the GPIOD_PUR register. Example: GPIOD0, clear bit 0 in the GPIOD_PUR register.
GPIOD1 ($\overline{CS3}$)	56	L6			
GPIOD2 ($\overline{CS4}$)	57	K6			
GPIOD3 ($\overline{CS5}$)	58	N7			
GPIOD4 ($\overline{CS6}$)	59	P7			
GPIOD5 ($\overline{CS7}$)	60	L7			
TXD0 **(GPIOE0)**	4	B1	Output Input/ Output	In reset, output is disabled, pull-up is enabled	**Transmit Data** — SCI0 transmit data output **Port E GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is SCI output. To deactivate the internal pull-up resistor, clear bit 0 in the GPIOE_PUR register.
RXD0 **(GPIOE1)**	5	D2	Input Input/ Output	Input, pull-up enabled	**Receive Data** — SCI0 receive data input **Port E GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is SCI output. To deactivate the internal pull-up resistor, clear bit 1 in the GPIOE_PUR register.

Table 2-2 Signal and Package Information for the 160-Pin LQFP and MBGA

Signal Name	Pin No.	*Ball No.*	Type	State During Reset	Signal Description
INDEX0 **(TA2)** **(GPIOC6)**	157	A1	Schmitt Input Schmitt Input/ Output Schmitt Input/ Output	Input, pull-up enabled	**Index** — Quadrature Decoder 0, INDEX input **TA2** — Timer A, Channel 2 **Port C GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is INDEX0. To deactivate the internal pull-up resistor, clear bit 6 of the GPIOC_PUR register.
HOME0 **(TA3)** **(GPIOC7)**	158	B3	Schmitt Input Schmitt Input/ Output Schmitt Input/ Output	Input, pull-up enabled	**Home** — Quadrature Decoder 0, HOME input **TA3** — Timer A ,Channel 3 **Port C GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is HOME0. To deactivate the internal pull-up resister, clear bit 7 of the GPIOC_PUR register.
SCLK0 **(GPIOE4)**	146	A6	Schmitt Input/ Output Schmitt Input/ Output	Input, pull-up enabled	**SPI 0 Serial Clock** — In the master mode, this pin serves as an output, clocking slaved listeners. In slave mode, this pin serves as the data clock input. **Port E GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is SCLK0. To deactivate the internal pull-up resistor, clear bit 4 in the GPIOE_PUR register.

Table 2-2 Signal and Package Information for the 160-Pin LQFP and MBGA

Signal Name	Pin No.	*Ball No.*	Type	State During Reset	Signal Description
ANB0	116	C13	Input	Analog Input	**ANB0 - 3** — Analog inputs to ADC B, channel 0
ANB1	117	B14			
ANB2	118	C12			
ANB3	119	B13			
ANB4	120	A14	Input	Analog Input	**ANB4 - 7** — Analog inputs to ADC B, channel 1
ANB5	121	A13			
ANB6	122	B12			
ANB7	123	A12			
TEMP_ SENSE	108	E11	Output	Analog Output	**Temperature Sense Diode** — This signal connects to an on-chip diode that can be connected to one of the ADC inputs and used to monitor the temperature of the die. Must be bypassed with a 0.01μF capacitor.
CAN_RX	143	B7	Schmitt Input	Input, pull-up enabled	**FlexCAN Receive Data** — This is the CAN input. This pin has an internal pull-up resistor. To deactivate the internal pull-up resistor, set the CAN bit in the SIM_PUDR register.
CAN_TX	142	D6	Open Drain Output	Open Drain Output	**FlexCAN Transmit Data** — CAN output with internal pull-up enable at reset. * * **Note:** If a pin is configured as open drain output mode, internal pull-up will automatically be disabled when it outputs low. Internal pull-up will be enabled unless it has been manually disabled by clearing the corresponding bit in the PUREN register of the GPIO module, when it outputs high. If a pin is configured as push-pull output mode, internal pull-up will automatically be disabled, whether it outputs low or high.
TC0 **(GPIOE8)**	133	A9	Schmitt Input/ Output Schmitt Input/ Output	Input, pull-up enabled	**TC0** — Timer C, Channel 0 and 1 **Port E GPIO** — These GPIO pins can be individually programmed as input or output pins. At reset, these pins default to Timer functionality. To deactivate the internal pull-up resistor, clear the appropriate bit of the GPIOE_PUR register.
TC1 (GPIOE9)	135	B9			

Part 3 On-Chip Clock Synthesis (OCCS)

3.1 Introduction

Refer to the OCCS chapter of the **56F8300 Peripheral User Manual** for a full description of the OCCS. The material contained here identifies the specific features of the OCCS design. **Figure 3-1** shows the specific OCCS block diagram to reference from the OCCS chapter of the **56F8300 Peripheral User Manual**.

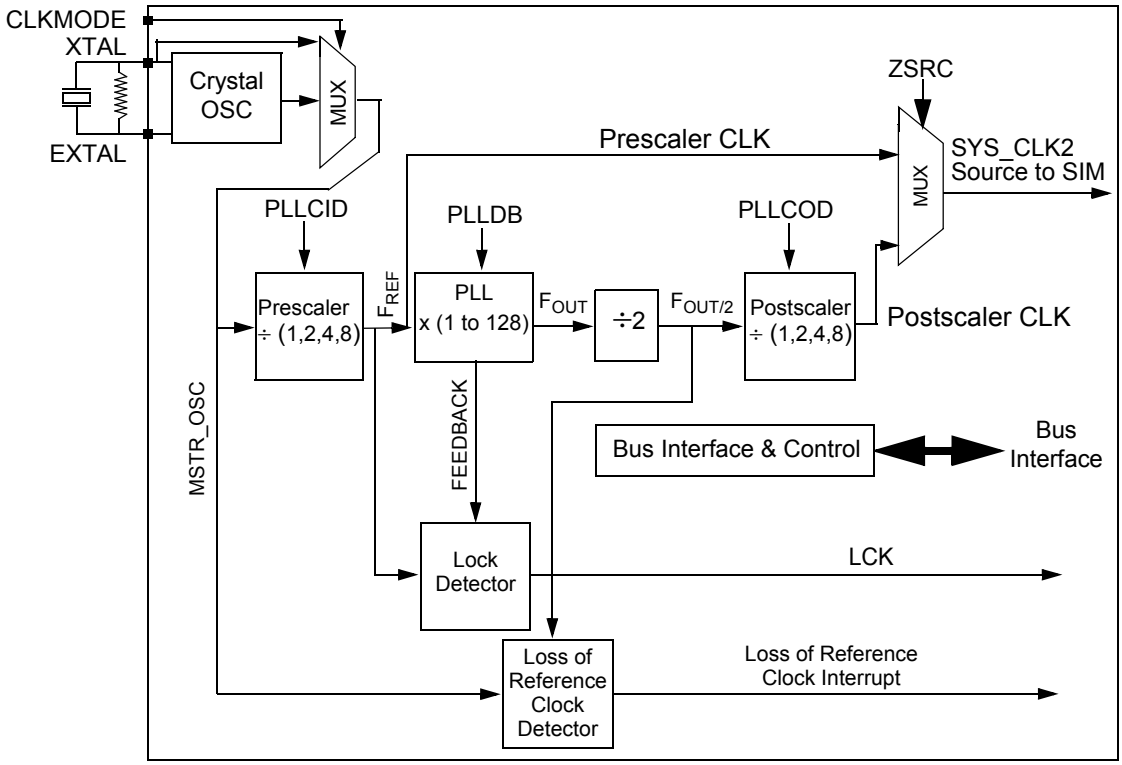


Figure 3-1 OCCS Block Diagram

3.2 External Clock Operation

The system clock can be derived from an external crystal, ceramic resonator, or an external system clock signal. To generate a reference frequency using the internal oscillator, a reference crystal or ceramic resonator must be connected between the EXTAL and XTAL pins.

3.2.1 Crystal Oscillator

The internal oscillator is also designed to interface with a parallel-resonant crystal resonator in the frequency range specified for the external crystal in **Table 10-13**. A recommended crystal oscillator circuit is shown in **Figure 3-2**. Follow the crystal supplier's recommendations when selecting a crystal, since

Table 4-7 Flash Memory Partitions

	Flash Size	Sectors	Sector Size	Page Size
Program Flash	256KB	16	8K x 16 bits	512 x 16 bits
Data Flash	8KB	16	256 x 16 bits	256 x 16 bits
Boot Flash	16KB	4	2K x 16 bits	256 x 16 bits

Please see **56F8300 Peripheral User Manual** for additional Flash information.

4.6 EOnCE Memory Map

Table 4-8 EOnCE Memory Map

Address	Register Acronym	Register Name
		Reserved
X:$FF FF8A	OESCR	External Signal Control Register
		Reserved
X:$FF FF8E	OBCNTR	Breakpoint Unit [0] Counter
		Reserved
X:$FF FF90	OBMSK (32 bits)	Breakpoint 1 Unit [0] Mask Register
X:$FF FF91	—	Breakpoint 1 Unit [0] Mask Register
X:$FF FF92	OBAR2 (32 bits)	Breakpoint 2 Unit [0] Address Register
X:$FF FF93	—	Breakpoint 2 Unit [0] Address Register
X:$FF FF94	OBAR1 (24 bits)	Breakpoint 1 Unit [0] Address Register
X:$FF FF95	—	Breakpoint 1 Unit [0] Address Register
X:$FF FF96	OBCR (24 bits)	Breakpoint Unit [0] Control Register
X:$FF FF97	—	Breakpoint Unit [0] Control Register
X:$FF FF98	OTB (21-24 bits/stage)	Trace Buffer Register Stages
X:$FF FF99	—	Trace Buffer Register Stages
X:$FF FF9A	OTBPR (8 bits)	Trace Buffer Pointer Register
X:$FF FF9B	OTBCR	Trace Buffer Control Register
X:$FF FF9C	OBASE (8 bits)	Peripheral Base Address Register
X:$FF FF9D	OSR	Status Register
X:$FF FF9E	OSCNTR (24 bits)	Instruction Step Counter
X:$FF FF9F	—	Instruction Step Counter
X:$FF FFA0	OCR (bits)	Control Register
		Reserved
X:$FF FFFC	OCLSR (8 bits)	Core Lock / Unlock Status Register

Table 4-15 Pulse Width Modulator A Registers Address Map (PWMA_BASE = $00 F140)
PWMA is NOT available in the 56F8157 device

Register Acronym	Address Offset	Register Description
PWMA_PMCTL	$0	Control Register
PWMA_PMFCTL	$1	Fault Control Register
PWMA_PMFSA	$2	Fault Status Acknowledge Register
PWMA_PMOUT	$3	Output Control Register
PWMA_PMCNT	$4	Counter Register
PWMA_PWMCM	$5	Counter Modulo Register
PWMA_PWMVAL0	$6	Value Register 0
PWMA_PWMVAL1	$7	Value Register 1
PWMA_PWMVAL2	$8	Value Register 2
PWMA_PWMVAL3	$9	Value Register 3
PWMA_PWMVAL4	$A	Value Register 4
PWMA_PWMVAL5	$B	Value Register 5
PWMA_PMDEADTM	$C	Dead Time Register
PWMA_PMDISMAP1	$D	Disable Mapping Register 1
PWMA_PMDISMAP2	$E	Disable Mapping Register 2
PWMA_PMCFG	$F	Configure Register
PWMA_PMCCR	$10	Channel Control Register
PWMA_PMPORT	$11	Port Register
PWMA_PMICCR	$12	PWM Internal Correction Control Register

Table 4-16 Pulse Width Modulator B Registers Address Map (PWMB_BASE = $00 F160)

Register Acronym	Address Offset	Register Description
PWMB_PMCTL	$0	Control Register
PWMB_PMFCTL	$1	Fault Control Register
PWMB_PMFSA	$2	Fault Status Acknowledge Register
PWMB_PMOUT	$3	Output Control Register
PWMB_PMCNT	$4	Counter Register
PWMB_PWMCM	$5	Counter Modulo Register
PWMB_PWMVAL0	$6	Value Register 0

Table 4-21 Analog-to-Digital Converter Registers Address Map (Continued) (ADCB_BASE = $00 F240)

Register Acronym	Address Offset	Register Description
ADCB_HLMT 5	$1E	High Limit Register 5
ADCB_HLMT 6	$1F	High Limit Register 6
ADCB_HLMT 7	$20	High Limit Register 7
ADCB_OFS 0	$21	Offset Register 0
ADCB_OFS 1	$22	Offset Register 1
ADCB_OFS 2	$23	Offset Register 2
ADCB_OFS 3	$24	Offset Register 3
ADCB_OFS 4	$25	Offset Register 4
ADCB_OFS 5	$26	Offset Register 5
ADCB_OFS 6	$27	Offset Register 6
ADCB_OFS 7	$28	Offset Register 7
ADCB_POWER	$29	Power Control Register
ADCB_CAL	$2A	ADC Calibration Register

Table 4-22 Temperature Sensor Register Address Map (TSENSOR_BASE = $00 F270)

Temperature Sensor is NOT available in the 56F8157 device

Register Acronym	Address Offset	Register Description
TSENSOR_CNTL	$0	Control Register

Table 4-23 Serial Communication Interface 0 Registers Address Map (SCI0_BASE = $00 F280)

Register Acronym	Address Offset	Register Description
SCI0_SCIBR	$0	Baud Rate Register
SCI0_SCICR	$1	Control Register
		Reserved
SCI0_SCISR	$3	Status Register
SCI0_SCIDR	$4	Data Register

Add. Offset	Register Name		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$0	IPR0	R	0	0	BKPT_U0 IPL		STPCNT IPL		0	0	0	0	0	0	0	0	0	0
		W																
$1	IPR1	R	0	0	0	0	0	0	0	0	0	0	RX_REG IPL		TX_REG IPL		TRBUF IPL	
		W																
$2	IPR2	R	FMCBE IPL		FMCC IPL		FMERR IPL		LOCK IPL		LVI IPL		0	0	IRQB IPL		IRQA IPL	
		W																
$3	IPR3	R	GPIOD IPL		GPIOE IPL		GPIOF IPL		FCMSGBUF IPL		FCWKUP IPL		FCERR IPL		FCBOFF IPL		0	0
		W																
$4	IPR4	R	SPI0_RCV IPL		SPI1_XMIT IPL		SPI1_RCV IPL		0	0	0	0	GPIOA IPL		GPIOB IPL		GPIOC IPL	
		W																
$5	IPR5	R	DEC1_XIRQ IPL		DEC1_HIRQ IPL		SCI1_RCV IPL		SCI1_RERR IPL		0	0	SCI1_TIDL IPL		SCI1_XMIT IPL		SPI0_XMIT IPL	
		W																
$6	IPR6	R	TMRC0 IPL		TMRD3 IPL		TMRD2 IPL		TMRD1 IPL		TMRD0 IPL		0	0	DEC0_XIRQ IPL		DEC0_HIRQ IPL	
		W																
$7	IPR7	R	TMRA0 IPL		TMRB3 IPL		TMRB2 IPL		TMRB1 IPL		TMRB0 IPL		TMRC3 IPL		TMRC2 IPL		TMRC1 IPL	
		W																
$8	IPR8	R	SCI0_RCV IPL		SCI0_RERR IPL		0	0	SCI0_TIDL IPL		SCI0_XMIT IPL		TMRA3 IPL		TMRA2 IPL		TMRA1 IPL	
		W																
$9	IPR9	R	PWMA F IPL		PWMB F IPL		PWMA_RL IPL		PWMB_RL IPL		ADCA_ZC IPL		ABCB_ZC IPL		ADCA_CC IPL		ADCB_CC IPL	
		W																
$A	VBA	R	0	0	0	VECTOR BASE ADDRESS												
		W																
$B	VBA0	R	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 0						
		W																
$C	FIVAL0	R	FAST INTERRUPT 0 VECTOR ADDRESS LOW															
		W																
$D	FIVAH0	R	0	0	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 0 VECTOR ADDRESS HIGH				
		W																
$E	FIM1	R	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 1						
		W																
$F	FIVAL1	R	FAST INTERRUPT 1 VECTOR ADDRESS LOW															
		W																
$10	FIVAH1	R	0	0	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 1 VECTOR ADDRESS HIGH				
		W																
$11	IRQP0	R	PENDING [16:2]															1
		W																
$12	IRQP1	R	PENDING [32:17]															
		W																
$13	IRQP2	R	PENDING [48:33]															
		W																
$14	IRQP3	R	PENDING [64:49]															
		W																
$15	IRQP4	R	PENDING [80:65]															
		W																
$16	IRQP5	R	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	PEND-ING [81]
		W																
	Reserved																	
$1D	ICTL	R	INT	IPIC			VAB						INT_DIS	1	IRQB STATE	IRQA STATE	IRQB EDG	IRQA EDG
		W																

= Reserved

Figure 5-2 ITCN Register Map Summary

Part 9 Joint Test Action Group (JTAG)

9.1 JTAG Information

Please contact your Freescale marketing representative or authorized distributor for device/package-specific BSDL information.

Part 10 Specifications

10.1 General Characteristics

The 56F8357/56F8157 are fabricated in high-density CMOS with 5V-tolerant TTL-compatible digital inputs. The term “5V-tolerant” refers to the capability of an I/O pin, built on a 3.3V-compatible process technology, to withstand a voltage up to 5.5V without damaging the device. Many systems have a mixture of devices designed for 3.3V and 5V power supplies. In such sytems, a bus may carry both 3.3V- and 5V-compatible I/O voltage levels (a standard 3.3V I/O is designed to receive a maximum voltage of 3.3V ± 10% during normal operation without causing damage). This 5V-tolerant capability therefore offers the power savings of 3.3V I/O levels combined with the ability to receive 5V levels without damage.

Absolute maximum ratings in **Table 10-1** are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond these ratings may affect device reliability or cause permanent damage to the device.

Note: All specifications meet both Automotive and Industrial requirements unless individual specifications are listed.

Note: *The 56F8157 device is guaranteed to 40MHz and specified to meet Industrial requirements only.*

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Table 10-16 External Memory Interface Timing

Characteristic	Symbol	Wait States Configuration	D	M	Wait States Controls	Unit
Address Valid to $\overline{WR}$ Asserted	t_{AWR}	WWS=0	-1.477	0.50	WWSS	ns
		WWS>0	-1.564	0.75 + DCAOE		
$\overline{WR}$ Width Asserted to $\overline{WR}$ Deasserted	t_{WR}	WWS=0	-0.186	0.25 + DCAOE	WWS	ns
		WWS>0	-0.256	0		
Data Out Valid to $\overline{WR}$ Asserted	t_{DWR}	WWS=0	-9.568	0.25 + DCAEO	WWSS	ns
		WWS=0	-1.721	0.00		
		WWS>0	-9.227	0.50		
		WWS>0	-1.808	0.25 + DCAOE		
Valid Data Out Hold Time after $\overline{WR}$ Deasserted	t_{DOH}		-2.287	0.25 + DCAEO	WWSH	ns
Valid Data Out Set-Up Time to $\overline{WR}$ Deasserted	t_{DOS}		-1.622	0.25 + DCAOE	WWS,WWSS	ns
			-9.041	0.50		
Valid Address after $\overline{WR}$ Deasserted	t_{WAC}		-3.918	0.25 + DCAEO	WWSH	ns
$\overline{RD}$ Deasserted to Address Invalid	t_{RDA}		-2.229	0.00	RWSH	ns
Address Valid to $\overline{RD}$ Deasserted	t_{ARDD}		-1.887	1.00	RWSS,RWS	ns
Valid Input Data Hold after $\overline{RD}$ Deasserted	t_{DRD}		0.00	N/A[1]	—	ns
$\overline{RD}$ Assertion Width	t_{RD}		0.212	1.00	RWS	ns
Address Valid to Input Data Valid	t_{AD}		-14.427	1.00	RWSS,RWS	ns
			-19.751	1.25 + DCAOE		
Address Valid to $\overline{RD}$ Asserted	t_{ARDA}		-2.121	0.00	RWSS	ns
$\overline{RD}$ Asserted to Input Data Valid	t_{RDD}		-12.306	1.00	RWSS,RWS	ns
			-17.630	1.25 + DCAOE		
$\overline{WR}$ Deasserted to $\overline{RD}$ Asserted	t_{WRRD}		-1.923	0.25 + DCAEO	WWSH,RWSS	ns
$\overline{RD}$ Deasserted to $\overline{RD}$ Asserted	t_{RDRD}		-0.234[2]	0.00	RWSS,RWSH MDAR[3], [4]	ns
$\overline{WR}$ Deasserted to $\overline{WR}$ Asserted	t_{WRWR}	WWS=0	-1.279	0.75 + DCAEO	WWSS, WWSH	ns
		WWS>0	-0.938	1.00		
$\overline{RD}$ Deasserted to $\overline{WR}$ Asserted	t_{RDWR}	WWS=0	-0.046	0.50	RWSH, WWSS, MDAR[3]	ns
		WWS>0	0.052	0.75 + DCAOE		

1. N/A, since device captures data before it deasserts RD
2. If RWSS = RWSH = 0, and the chip select does not change, then $\overline{RD}$ does not deassert during back-to-back reads.
3. Substitute BMDAR for MDAR if there is no chip select
4. MDAR is active in this calculation only when the chip select changes.

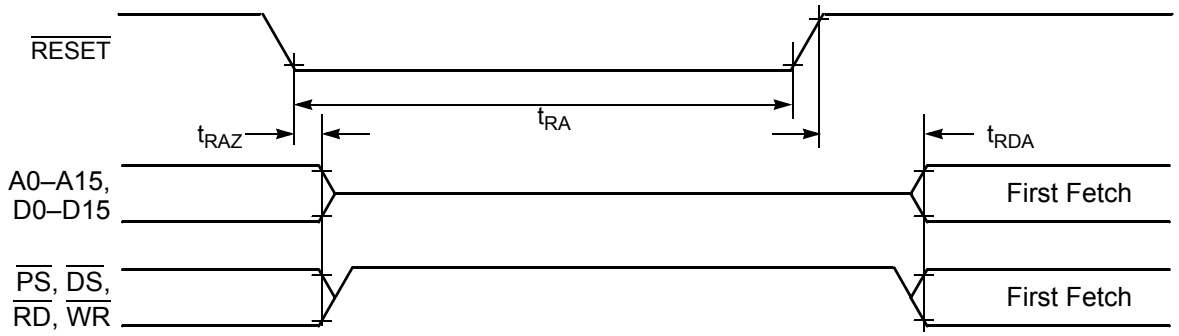


Figure 10-5 Asynchronous Reset Timing

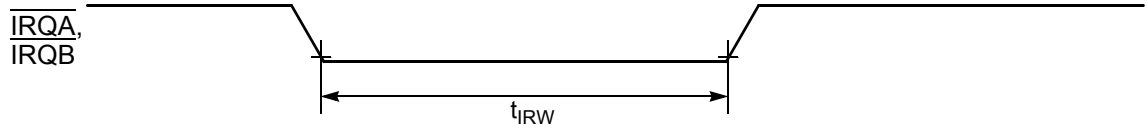
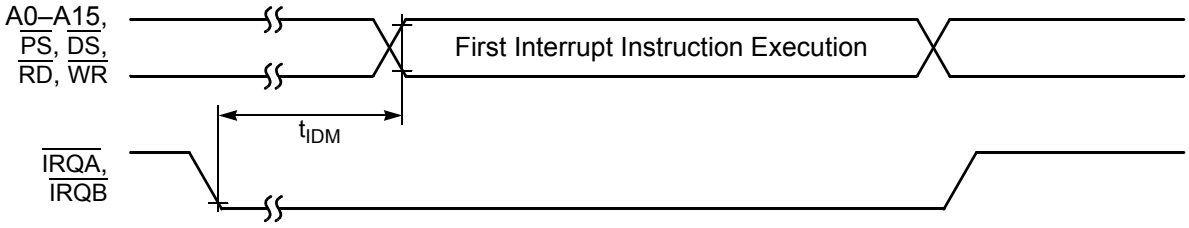
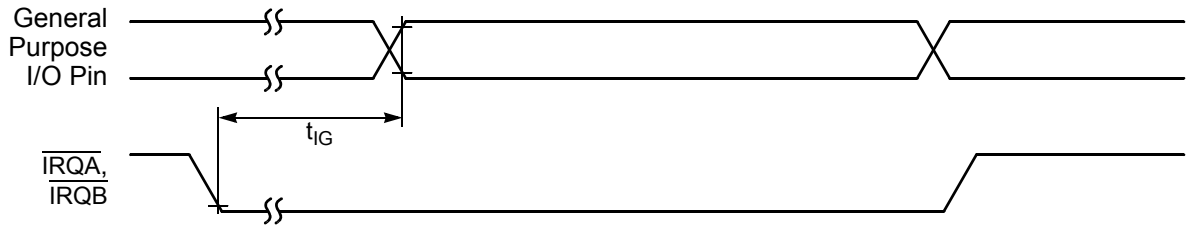


Figure 10-6 External Interrupt Timing (Negative-Edge Sensitive)



a) First Interrupt Instruction Execution



b) General Purpose I/O

Figure 10-7 External Level-Sensitive Interrupt Timing

Part 11 Packaging

Note: *The 160 Map Ball Grid Array is not available in the 56F8157 device.*

11.1 56F8357 Package and Pin-Out Information

This section contains package and pin-out information for the 56F8357. This device comes in a 160-pin Low-profile Quad Flat Pack (LQFP) and *160 Map Ball Grid Array*. **Figure 11-1** shows the package lay-out for the 160-pin LQFP, and **Figure 11-2** for the160 Map Ball Grid Array. **Figure 11-5** shows the mechanical parameters for the LQFP package and **Figure 11-3** for the MBGA, **Table 11-1** lists the pin-out for the 160-pin LQFP and **Table 11-2** lists the pin-out for the 160 MBGA.

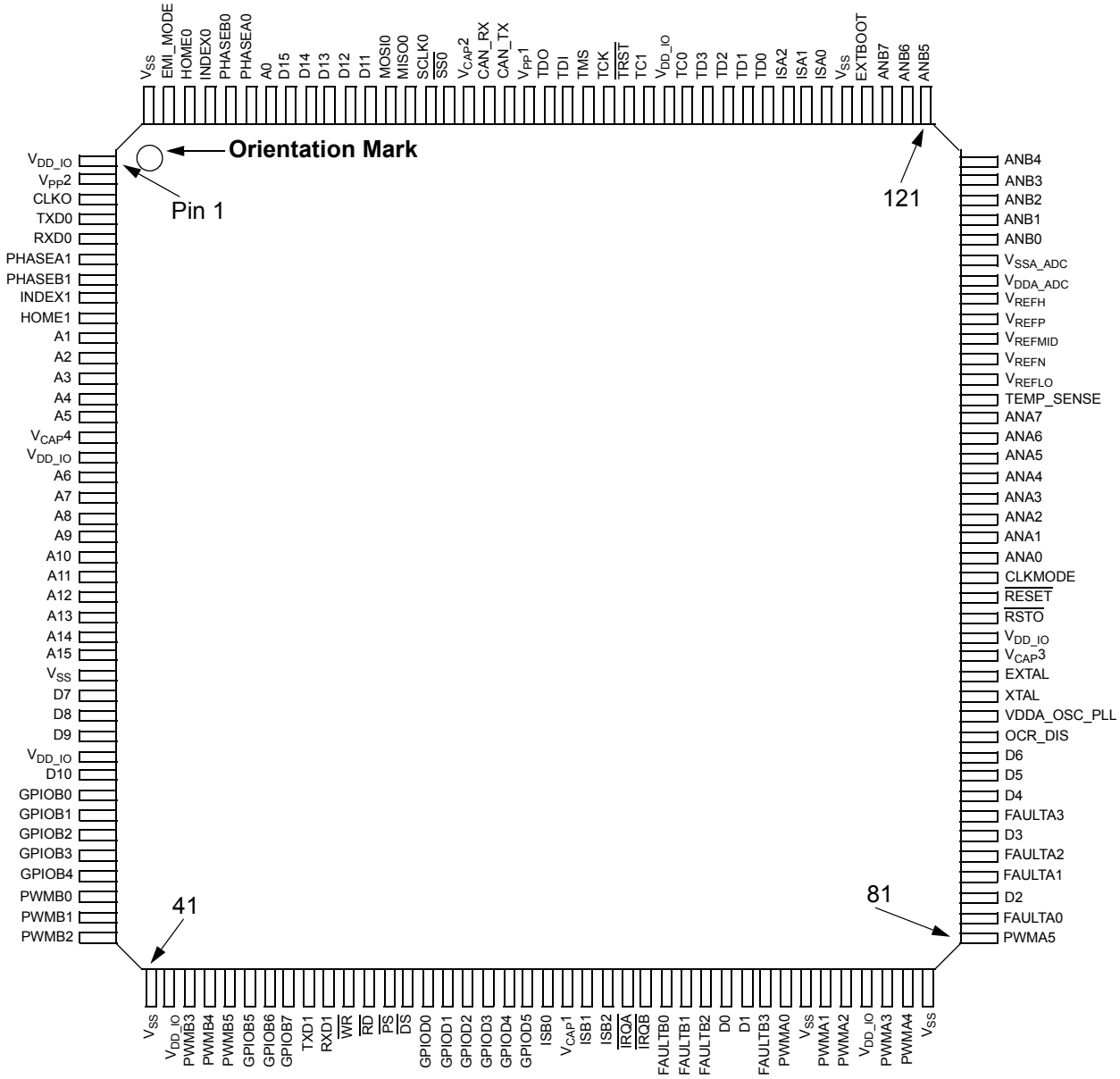


Figure 11-1 Top View, 56F8357 160-Pin LQFP Package

Table 11-1 56F8357 160-Pin LQFP Package Identification by Pin Number (Continued)

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
26	A15	66	$\overline{\text{IRQB}}$	106	ANA6	146	SCLK0
27	V_{SS}	67	FAULTB0	107	ANA7	147	MISO0
28	D7	68	FAULTB1	108	TEMP_SENSE	148	MOSI0
29	D8	69	FAULTB2	109	V_{REFLO}	149	D11
30	D9	70	D0	110	V_{REFN}	150	D12
31	V_{DD_IO}	71	D1	111	V_{REFMID}	151	D13
32	D10	72	FAULTB3	112	V_{REFP}	152	D14
33	GPIOB0	73	PWMA0	113	V_{REFH}	153	D15
34	GPIOB1	74	V_{SS}	114	V_{DDA_ADC}	154	A0
35	GPIOB2	75	PWMA1	115	V_{SSA_ADC}	155	PHASEA0
36	GPIOB3	76	PWMA2	116	ANB0	156	PHASEB0
37	GPIOB4	77	V_{DD_IO}	117	ANB1	157	INDEX0
38	PWMB0	78	PWMA3	118	ANB2	158	HOME0
39	PWMB1	79	PWMA4	119	ANB3	159	EMI_MODE
40	PWMB2	80	V_{SS}	120	ANB4	160	V_{SS}

Part 12 Design Considerations

12.1 Thermal Design Considerations

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$T_J = T_A + (R_{\theta JA} \times P_D)$

where:

T_A = Ambient temperature for the package (^oC)
$R_{\theta JA}$ = Junction-to-ambient thermal resistance ($^oC/W$)
P_D = Power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry-standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single-layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single-layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low-power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

where:

$R_{\theta JA}$ = Package junction-to-ambient thermal resistance °C/W
$R_{\theta JC}$ = Package junction-to-case thermal resistance °C/W
$R_{\theta CA}$ = Package case-to-ambient thermal resistance °C/W

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$T_J = T_T + (\Psi_{JT} \times P_D)$

where:

T_T = Thermocouple temperature on top of package (^oC)
Ψ_{JT} = Thermal characterization parameter (^oC)/W
P_D = Power dissipation in package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

When heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back-calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

12.2 Electrical Design Considerations

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Use the following list of considerations to assure correct operation:

- Provide a low-impedance path from the board power supply to each V_{DD} pin on the hybrid controller, and from the board ground to each V_{SS} (GND) pin
- The minimum bypass requirement is to place six 0.01–0.1µF capacitors positioned as close as possible to the package supply pins. The recommended bypass configuration is to place one bypass capacitor on each of the V_{DD}/V_{SS} pairs, including V_{DDA}/V_{SSA}. Ceramic and tantalum capacitors tend to provide better performance tolerances.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip V_{DD} and V_{SS} (GND) pins are less than 0.5 inch per capacitor lead
- Use at least a four-layer Printed Circuit Board (PCB) with two inner layers for V_{DD} and V_{SS}
- Bypass the V_{DD} and V_{SS} layers of the PCB with approximately 100µF, preferably with a high-grade capacitor such as a tantalum capacitor
- Because the device's output signals have fast rise and fall times, PCB trace lengths should be minimal

Part 13 Ordering Information

Table 13-1 lists the pertinent information needed to place an order. Consult a Freescale Semiconductor sales office or authorized distributor to determine availability and to order parts.

Table 13-1 Ordering Information

Part	Supply Voltage	Package Type	Pin Count	Frequency (MHz)	Ambient Temperature Range	Order Number
MC56F8357	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	160	60	-40° to + 105° C	MC56F8357VPY60
MC56F8157	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	160	60	-40° to + 105° C	MC56F8157VPY
MC56F8357	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	160	60	-40° to + 105° C	MC56F8357VPYE*
MC56F8357	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	160	60	-40° to + 125° C	MC56F8357MPYE*
MC56F8157	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	160	60	-40° to + 105° C	MC56F8157VPYE*
MC56F8357	3.0–3.6 V	Mold Array Process Ball Grid Array (MAPBGA)	160	60	-40° to + 105° C	MC56F8357VVF*

*This package is RoHS compliant.