Intel - EP4S40G5H40C2ES1 Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	21248
Number of Logic Elements/Cells	531200
Total RAM Bits	28033024
Number of I/O	654
Number of Gates	-
Voltage - Supply	0.92V ~ 0.98V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1517-BBGA, FCBGA
Supplier Device Package	1517-HBGA (42.5x42.5)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep4s40g5h40c2es1

Feature Summary

The following list summarizes the Stratix IV device family features:

- Up to 48 full-duplex CDR-based transceivers in Stratix IV GX and GT devices supporting data rates up to 8.5 Gbps and 11.3 Gbps, respectively
- Dedicated circuitry to support physical layer functionality for popular serial protocols, such as PCI Express (PCIe) (PIPE) Gen1 and Gen2, Gbps Ethernet (GbE), Serial RapidIO, SONET / SDH, XAUI / HiGig, (OIF) CEI-6G, SD / HD / 3G-SDI, Fibre Channel, SFI-5, and Interlaken
- Complete PCIe protocol solution with embedded PCIe hard IP blocks that implement PHY-MAC layer, Data Link layer, and Transaction layer functionality

f For more information, refer to the IP Compiler for PCI Express User Guide

- Programmable transmitter pre-emphasis and receiver equalization circuitry to compensate for frequency-dependent losses in the physical medium
- Typical physical medium attachment (PMA) power consumption of 100 mW at 3.125 Gbps and 135 mW at 6.375 Gbps per channel
- 72,600 to 813,050 equivalent LEs per device
- 7,370 to 33,294 Kb of enhanced TriMatrix memory consisting of three RAM block sizes to implement true dual-port memory and FIFO buffers
- High-speed digital signal processing (DSP) blocks configurable as 9 x 9-bit, 12 x 12-bit, 18 x 18-bit, and 36 x 36-bit full-precision multipliers at up to 600 MHz
- Up to 16 global clocks (GCLK), 88 regional clocks (RCLK), and 132 periphery clocks (PCLK) per device
- Programmable power technology that minimizes power while maximizing device performance
- Up to 1,120 user I / O pins arranged in 24 modular I / O banks that support a wide range of single-ended and differential I / O standards
- Support for high-speed external memory interfaces including DDR, DDR2, DDR3 SDRAM, RLDRAM II, QDR II, and QDR II+ SRAM on up to 24 modular I / O banks
- High-speed LVDS I / O support with serializer / deserializer (SERDES), dynamic phase alignment (DPA), and soft-CDR circuitry at data rates up to 1.6 Gbps
- Support for source-synchronous bus standards, including SGMII, GbE, SPI-4 Phase 2 (POS-PHY Level 4), SFI-4.1, XSBI, UTOPIA IV, NPSI, and CSIX-L1
- Pinouts for Stratix IV E devices designed to allow migration of designs from Stratix III to Stratix IV E with minimal PCB impact

Stratix IV GX Devices

Stratix IV GX devices provide up to 48 full-duplex CDR-based transceiver channels per device:

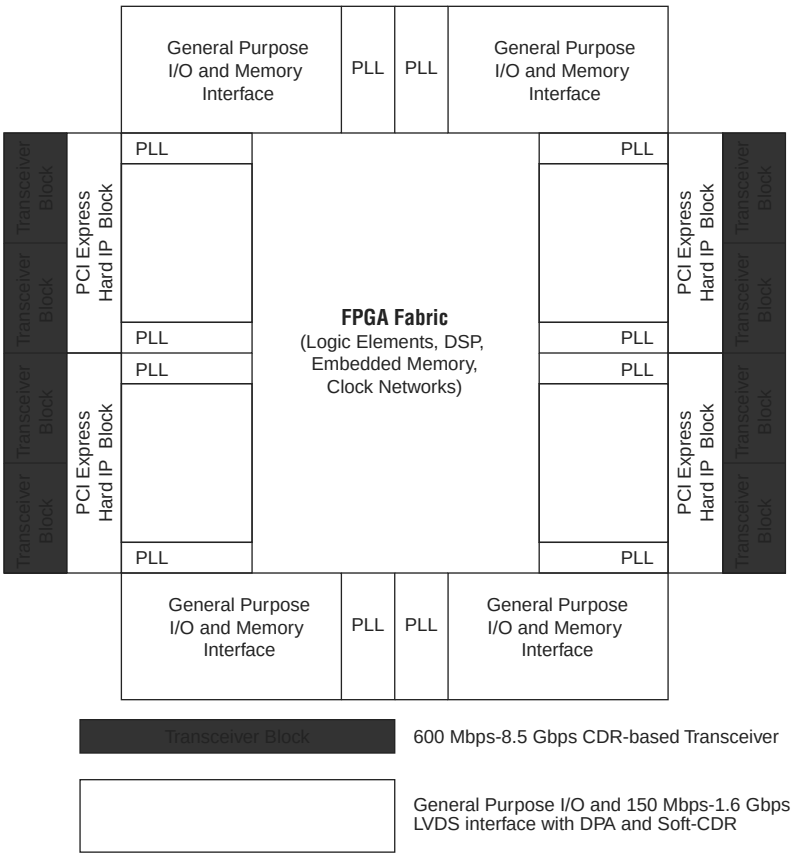
- Thirty-two out of the 48 transceiver channels have dedicated physical coding sublayer (PCS) and physical medium attachment (PMA) circuitry and support data rates between 600 Mbps and 8.5 Gbps
- The remaining 16 transceiver channels have dedicated PMA-only circuitry and support data rates between 600 Mbps and 6.5 Gbps

1 The actual number of transceiver channels per device varies with device selection. For more information about the exact transceiver count in each device, refer to Table 1–1 on page 1–11.

1 For more information about transceiver architecture, refer to the Transceiver Architecture in Stratix IV Devices chapter.

Figure 1–1 shows a high-level Stratix IV GX chip view.

Figure 1–1. Stratix IV GX Chip View (1)



Note to Figure 1–1:

(1) Resource counts vary with device selection, package selection, or both.

Stratix IV GT Devices

Stratix IV GT devices provide up to 48 CDR-based transceiverchannels per device:

Thirty-two out of the 48 transceiver channels have dedicated PCS and PMA

Architecture Features

The Stratix IV device family features are divided into high-speed transceiver features and FPGA fabric and I/O features.

1 The high-speed transceiver features apply only to Stratix IV GX and Stratix IV GT devices.

High-Speed Transceiver Features

The following sections describe high-speed transceiver features for Stratix IV GX and GT devices.

Highest Aggregate Data Bandwidth

Up to 48 full-duplex transceiver channels supporting data rates up to 8.5 Gbps in Stratix IV GX devices and up to 11.3 Gbps in Stratix IV GT devices.

Wide Range of Protocol Support

Physical layer support for the following serial protocols:

Stratix IV GX—PCIe Gen1 and Gen2, GbE, Serial RapidIO, SONET/SDH, XAUI/HiGig, (OIF) CEI-6G, SD/HD/3G-SDI, Fibre Channel, SFI-5, GPON, SAS/SATA, HyperTransport 1.0 and 3.0, and Interlaken

Stratix IV GT—40G/100G Ethernet, SFI-S, Interlaken, SFI-5.1, Serial RapidIO, SONET/SDH, XAUI/HiGig, (OIF) CEI-6G, 3G-SDI, and Fibre Channel

Extremely flexible and easy-to-configure transceiver data path to implement proprietary protocols

PCIe Support

Complete PCIe Gen1 and Gen2 protocol stack solution compliant to PCI Express base specification 2.0 that includes PHY-MAC, Data Link, and transaction layer circuitry embedded in PCI Express hard IP blocks

f For more information, refer to the PCI Express Compiler User Guide

Root complex and end-point applications

x1, x4, and x8 lane configurations

PIPE 2.0-compliant interface

Embedded circuitry to switch between Gen1 and Gen2 data rates

Built-in circuitry for electrical idle generation and detection, receiver detect, power state transitions, lane reversal, and polarity inversion

8B/10B encoder and decoder, receiver synchronization state machine, and ± 300 parts per million (ppm) clock compensation circuitry

Transaction layer support for up to two virtual channels (VCs)

System Integration

All Stratix IV devices support hot socketing

Four configuration modes:

- Passive Serial (PS)
- Fast Passive Parallel (FPP)
- Fast Active Serial (FAS)
- JTAG configuration

Ability to perform remote system upgrades

256-bit advanced encryption standard (AES) encryption of configuration bits protects your design against copying, reverse engineering, and tampering

Built-in soft error detection for configuration RAM cells

f For more information about how to connect the PLL, external memory interfaces, I/O, high-speed differential I/O, power, and the JTAG pins to PCB, refer to the Stratix IV GX and Stratix IV E Device Family Pin Connection Guidelines and the Stratix IV GT Device Family Pin Connection Guidelines

Table 1–2 lists the Stratix IV GX device package options.

Table 1–2. Stratix IV GX Device Package Options (1), (2)

Device	F780 (29 mm x 29 mm) (6)		F1152 (35 mm x 35 mm) (6)	F1152 (35 mm x 35 mm) (5), (7)		F1517 (40 mm x 40 mm) (5), (7)	F1760 (42.5 mm x 42.5 mm) (7)	F1932 (45 mm x 45 mm) (7)
EP4SGX70	DF29	—	—	HF35	—	—	—	—
EP4SGX110	DF29	—	FF35	HF35	—	—	—	—
EP4SGX180	DF29	—	FF35	—	HF35	KF40	—	—
EP4SGX230	DF29	—	FF35	—	HF35	KF40	—	—
EP4SGX290	—	FH29 (3)	FF35	—	HF35	KF40	KF43	NF45
EP4SGX360	—	FH29 (3)	FF35	—	HF35	KF40	KF43	NF45
EP4SGX530	—	—	—	—	HH35 (4)	KH40 (4)	KF43	NF45

Notes to Table 1–2:

(1) Device packages in the same column and marked under the same arrow sign have vertical migration capability.
(2) Use the Pin Migration Viewer in the Pin Planner to verify the pin migration compatibility when migrating devices. For more information, refer to I/O Management in the Quartus II Handbook, Volume 2
(3) The 780-pin EP4SGX290 and EP4SGX360 devices are available only in 33 mm x 33 mm Hybrid flip chip package.
(4) The 1152-pin and 1517-pin EP4SGX530 devices are available only in 42.5 mm x 42.5 mm Hybrid flip chip packages.
(5) When migrating between hybrid and flip chip packages, there is an additional keep-out area. For more information, refer to the Package Information Datasheet for Altera Devices
(6) Devices listed in this column are available in –2x, –3, and –4 speed grades. These devices do not have on-package decoupling capacitors.
(7) Devices listed in this column are available in –2, –3, and –4 speed grades. These devices have

1 On-package decoupling reduces the need for on-board or PCB decoupling capacitors by satisfying the transient current requirements at higher frequencies. The Power Delivery Network design tool for Stratix IV devices accounts for the on-package decoupling and reflects the reduced requirements for PCB decoupling capacitors.

Table 1–3 lists the Stratix IV GX device on-package decoupling information.

Table 1–3. Stratix IV GX Device On-Package Decoupling Information (1)

Ordering Information		V_{CC}	V_{CCIO}	V_{CCL_GXB}	$V_{CCA\_L/R}$	V_{CCT} and V_{CCR} (Shared)
EP4SGX70	HF35	2 u1uF + 2 u470nF	10nF per bank (2)	100nF per transceiver block	100nF	1 u470nF + 1 u47nF per side
EP4SGX110	HF35	2 u1uF + 2 u470nF	10nF per bank (2)	100nF per transceiver block	100nF	1 u470nF + 1 u47nF per side
EP4SGX180	HF35 KF40	2 u1uF + 2 u470nF	10nF per bank (2)	100nF per transceiver block	100nF	1 u470nF + 1 u47nF per side
EP4SGX230	HF35 KF40	2 u1 uF + 2 u470 nF	10 nF per bank (2)	100 nF per transceiver block	100 nF	1 u470 nF + 1 u47 nF per side
EP4SGX290	HF35 KF40 KF43 NF45	4 u1 uF + 4 u470 nF	10 nF per bank (2)	100 nF per transceiver block	100nF	1 u470 nF + 1 u47 nF per side
EP4SGX360	HF35 KF40 KF43 NF45	4 u1 uF + 4 u470 nF	10 nF per bank (2)	100 nF per transceiver block	100 nF	1 u470 nF + 1 u47 nF per side
EP4SGX530	HH35 KH40 KF43 NF45	4 u1 uF + 4 u470 nF	10 nF per bank (2)	100 nF per transceiver block	100 nF	1 u470 nF + 1 u47 nF per side

Notes to Table 1–3:

(1) Table 1–3 refers to production devices on-package decoupling. For more information about decoupling design of engineering sample (ES) devices, contact Altera Technical Support.

(2) For I/O banks 3(*), 4(*), 7(*), and 8(*) only. There is no OPD for I/O bank 1(*), 2(*), 5(*), and 6(*).

Table 1–4 lists the Stratix IV E device features.

Table 1–4. Stratix IV E Device Features

Feature	EP4SE230	EP4SE360		EP4SE530			EP4SE820		
Package Pin Count	780	780	1152	1152	1517	1760	1152	1517	1760
ALMs	91,200	141,440		212,480			325,220		
LEs	228,000	353,600		531,200			813,050		
High-Speed LVDS SERDES (up to 1.6 Gbps) (1)	56	56	88	88	112	112	88	112	132
SPI-4.2 Links	3	3	4	4	6		4	6	6
M9K Blocks (256 x 36 bits)	1,235	1,248		1,280			1610		
M144K Blocks (2048 x 72 bits)	22	48		64			60		
Total Memory (MLAB+M9K+ M144K) Kb	17,133	22,564		27,376			33,294		
Embedded Multipliers (18 x 18) (2)	1,288	1,040		1,024			960		
PLLs	4	4	8	8	12	12	8	12	12
User I/Os (3)	488	488	744	744	976	976	744 (4)	976 (4)	1120 (4)
Speed Grade (fastest to slowest)	–2, –3, –4	–2, –3, –4	–2, –3, –4	–2, –3, –4	–2, –3, –4	–2, –3, –4	–3, –4	–3, –4	–3, –4

Notes to Table 1–4:

(1) The user I/O count from the pin-out files include all general purpose I/Os, dedicated clock pins, and dual purpose configuration pins. Transceiver pins and dedicated configuration pins are not included in the pin count.

(2) Four multiplier adder mode.

(3) Total pairs of high-speed LVDS SERDES take the lowest channel count of R_X/T_X.

(4) This data is preliminary.

Table 1–5 summarizes the Stratix IV E device package options.

Table 1–5. Stratix IV E Device Package Options (1), (2)

Device	F780 (29 mm x 29 mm) (5), (6)	F1152 (35 mm x 35 mm) (5), (7)	F1517 (40 mm x 40 mm) (7)	F1760 (42.5 mm x 42.5 mm) (7)
EP4SE230	F29	—	—	—
EP4SE360	H29 (3)	F35	—	—
EP4SE530	—	H35 (4)	H40 (4)	F43
EP4SE820	—	H35 (4)	H40 (4)	F43

Notes to Table 1–5:

(1) Device packages in the same column and marked under the same arrow sign have vertical migration capability.

(2) Use the Pin Migration Viewer in the Pin Planner to verify the pin migration compatibility when migrating devices. For more information, refer to I/O Management in the Quartus II Handbook, Volume 2

(3) The 780-pin EP4SE360 device

Table 1–6 lists the Stratix IV E on-package decoupling information.

Table 1–7 lists the Stratix IV GT device features.

10G Transceiver Channels (600 Mbps - 11.3 Gbps with PMA + PCS)	12	12	24	24	24	24	32
8G Transceiver Channels (600 Mbps - 8.5 Gbps with PMA + PCS)(1)	12	12	0	8	8	0	0
PMA-only CMU Channels (600 Mbps- 6.5 Gbps)	12	12	12	16	16	12	16
PCIe hard IP Blocks	2	2	2	4	4	2	4
High-Speed LVDS SERDES (up to 1.6 Gbps)(2)	46	46	46	47	47	46	47
SP1-4.2 Links	2	2	2	2	2	2	2
M9K Blocks (256 x 36 bits)	1,235	1,280	1,235	936	1,248	1,280	
M144K Blocks (2048 x 72 bits)	22	64	22	36	48	64	
Total Memory (MLAB + M9K + M144K) Kb	17,133	27,376	17,133	17,248	22,564	27,376	
Embedded Multipliers 18 x 18(3)	1,288	1,024	1,288	832	1,024	1,024	
PLLs	8	8	8	12	12	8	12
User I/Os(4), (5)	654	654	654	781	781	654	781
Speed Grade (fastest to slowest)	–1, –2, –3	–1, –2, –3	–1, –2, –3	–1, –2, –3	–1, –2, –3	–1, –2, –3	–1, –2, –3

Notes to Table 1–7

(1) You can configure all 10G transceiver channels as 8G transceiver channels. For example, the EP4S40G2F40 device has twenty-four 8G transceiver channels and the EP4S100G5F45 device has thirty-two 8G transceiver channels.

(2) Total pairs of high-speed LVDS SERDES. Take the lowest channel count of TX or RX.

(3) Four multiplier adder mode.

(4) The user I/O count from the pin-out files include all general purpose I/Os, dedicated clock pins, and dual purpose configuration pins. Transceiver

Table 1–8 lists the resource counts for the Stratix IV GT devices.

Table 1–8. Stratix IV GT Device Package Options (1), (2)

Device	1517 Pin (40 mm x 40 mm) (3)	1932 Pin (45 mm x 45 mm)
Stratix IV GT 40 G Devices		
EP4S40G2	F40	—
EP4S40G5	H40 (4), (5)	—
Stratix IV GT 100 G Devices		
EP4S100G2	F40	—
EP4S100G3	—	F45
EP4S100G4	—	F45
EP4S100G5	H40 (4), (5)	F45

Notes to Table 1–8:

(1) This table represents pin compatability; however, it does not include hard IP block placement compatability.

(2) Devices under the same arrow shown have vertical migration capability.

(3) When migrating between hybrid and flip chip packages, there is additional keep-out area. For more information, refer to the Altera Device Package Information Data Sheet.

(4) EP4S40G5 and EP4S100G5 devices with 1517 pin count are only available in 42.5 x 42.5-mm Hybrid flip chip packages.

(5) If you are using the hard IP block, migration is not possible.

Table 1–9 lists the Stratix IV GT on-package decoupling information.

Table 1–9. Stratix IV GT Device On-Package Decoupling Information (1)

Ordering Information	V_{CC}	V_{CCIO}	V_{CCL_GXB}	$V_{CCA\_L/R}$	$V_{CCT\_L/R}$	V

		Updated the “Stratix IV Device Family Overview”, “Feature Summary”, “Stratix IV GT Devices”, “High-Speed Transceiver Features”, “FPGA Fabric and I/O Features”, “Highest Aggregate Data Bandwidth”, “System Integration”, and “Integrated Software Platform” sections.
November 2009	3.0	Added Table 1–3, Table 1–6, and Table 1–9. Updated Table 1–1, Table 1–2, Table 1–4, Table 1–5, Table 1–7, and Table 1–8. Updated Figure 1–3, Figure 1–4, and Figure 1–5. Minor text edits.