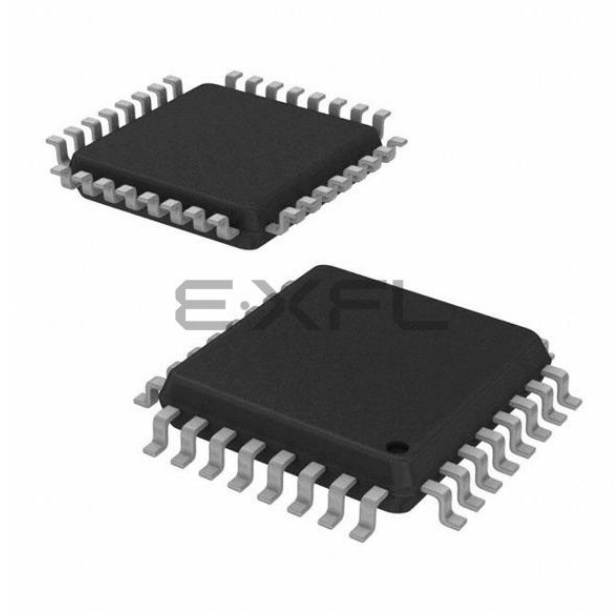

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Details	
Product Status	Obsolete
Core Processor	ST7
Core Size	8-Bit
Speed	8MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st72f344k2t6

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Figure 3. LQFP44 package pinout

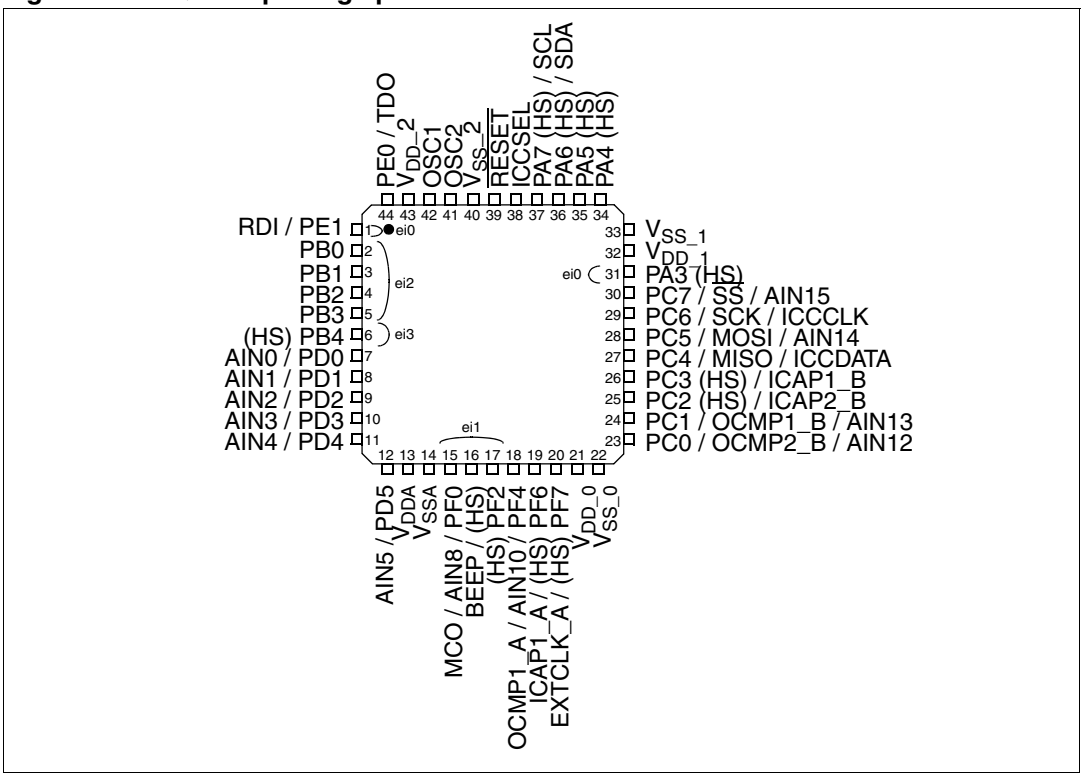
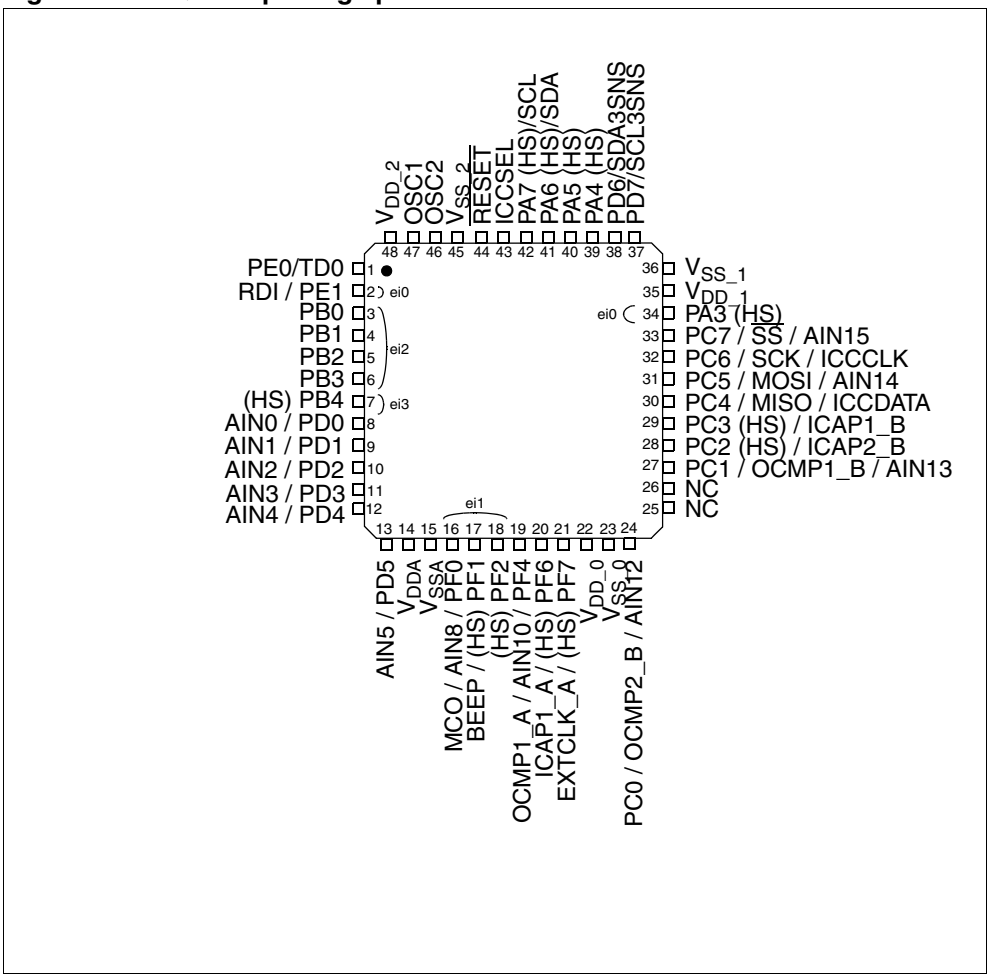


Figure 4. LQFP48 package pinout



Note: For external pin connection guidelines, refer to Section 13: Electrical characteristics.

Table 3. Device pin description (continued)

Pin n°			Pin name	Type	Level		Port						Main function (after reset)	Alternate function	
							Input (1)				Output				
LQFP32	LQFP44	LQFP48			Input	Output	float	wpu	int	ana	OD	PP			
10	25	28	PC2 (HS)/ICAP2_B	I/O	C_T	HS	X	X			X	X	Port C2	Timer B input capture 2	
11	26	29	PC3 (HS)/ICAP1_B	I/O	C_T	HS	X	X			X	X	Port C3	Timer B input capture 1	
12	27	30	PC4/MISO/ICCDATA	I/O	C_T		X	X			X	X	Port C4	SPI Master In / Slave Out data	ICC data input
13	28	31	PC5/MOSI/AIN14	I/O	C_T		X	X		X	X	X	Port C5	SPI Master Out / Slave In data	ADC analog input 14
14	29	32	PC6/SCK/ICCCLK	I/O	C_T		X	X			X	X	Port C6	SPI serial clock	ICC clock output
15	30	33	PC7/$\overline{SS}$/AIN15	I/O	C_T		X	X		X	X	X	Port C7	SPI slave select (active low)	ADC analog input 15
16	31	34	PA3 (HS)	I/O	C_T	HS	X		ei0		X	X	Port A3		
-	32	35	V_{DD_1} (2)	S									Digital main supply voltage		
-	33	36	V_{SS_1} (2)	S									Digital ground voltage		
-	-	37	PD7 (3)/ SCL3SNS	I/O	C_T	HS	X				T (4)		Port D7	I2C3SNS serial clock	
-	-	38	PD6 (3)/ SDA3SNS	I/O	C_T	HS	X				T		Port D6	I2C3SNS serial data	
17	34	39	PA4 (HS)	I/O	C_T	HS	X	X			X	X	Port A4		
-	35	40	PA5 (HS) (3)	I/O	C_T	HS	X	X			X	X	Port A5		
18	36	41	PA6 (HS)/SDA	I/O	C_T	HS	X				T		Port A6	I2C serial data	
19	37	42	PA7 (HS)/SCL	I/O	C_T	HS	X				T		Port A7	I2C serial clock	
20	38	43	ICCSEL (5)	I									ICC mode selection		
21	39	44	$\overline{RESET}$	I/O	C_T								Top priority non maskable interrupt.		
22	40	45	V_{SS_2} (2)	S									Digital ground voltage		
23	41	46	OSC2	O									Resonator oscillator inverter output		
24	42	47	OSC1	I									External clock input or resonator oscillator inverter input		
25	43	48	V_{DD_2} (2)	S									Digital main supply voltage		
26	44	1	PE0/TDO	I/O	C_T		X	X			X	X	Port E0	SCI transmit data out	

8.6 External interrupts

8.6.1 I/O port interrupt sensitivity

The external interrupt sensitivity is controlled by the IPA, IPB and ISxx bits of the EICR register (*Figure 24*). This control allows to have up to 4 fully independent external interrupt source sensitivities.

Each external interrupt source can be generated on four (or five) different events on the pin:

- Falling edge
- Rising edge
- Falling and rising edge
- Falling edge and low level
- Rising edge and high level (only for ei0 and ei2)

To guarantee correct functionality, the sensitivity bits in the EICR register can be modified only when the I1 and I0 bits of the CC register are both set to 1 (level 3). This means that interrupts must be disabled before changing sensitivity.

The pending interrupts are cleared by writing a different value in the ISx[1:0], IPA or IPB bits of the EICR.

Figure 24. External interrupt control bits

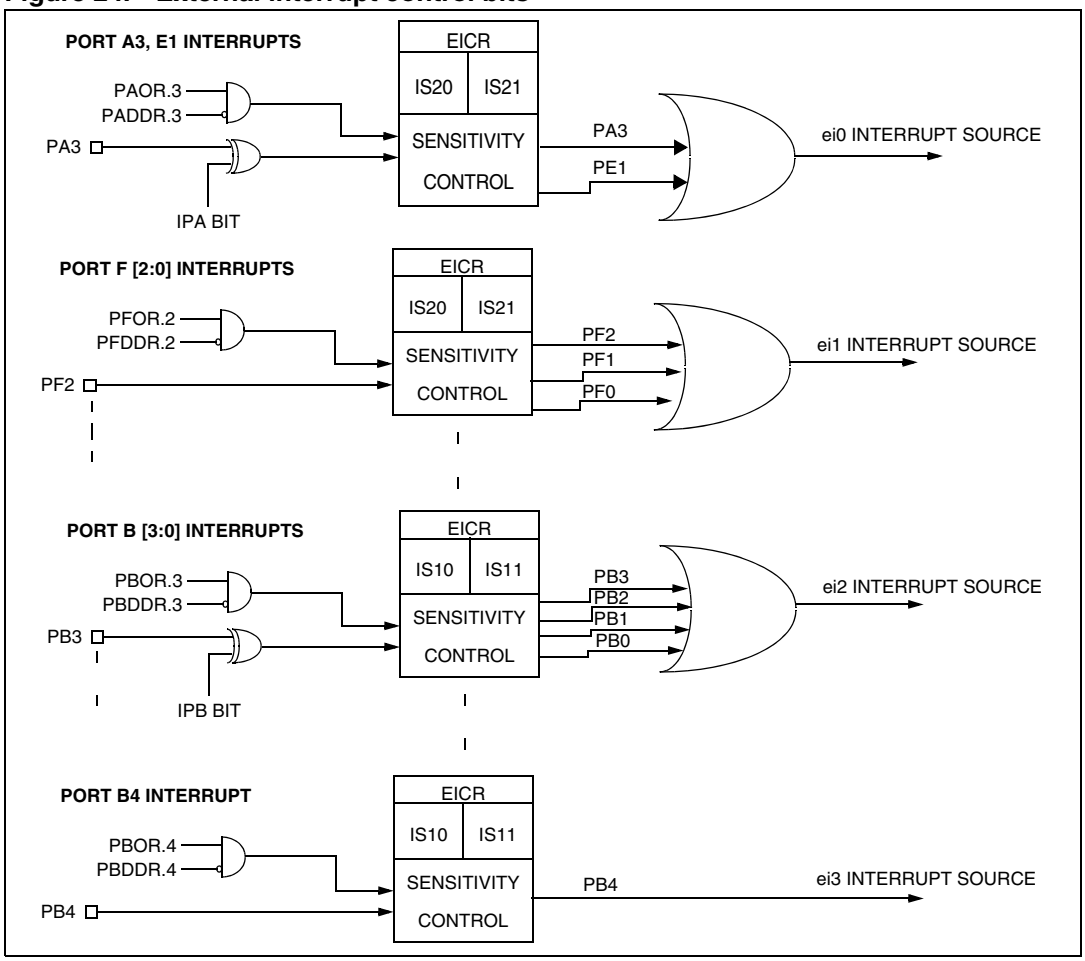
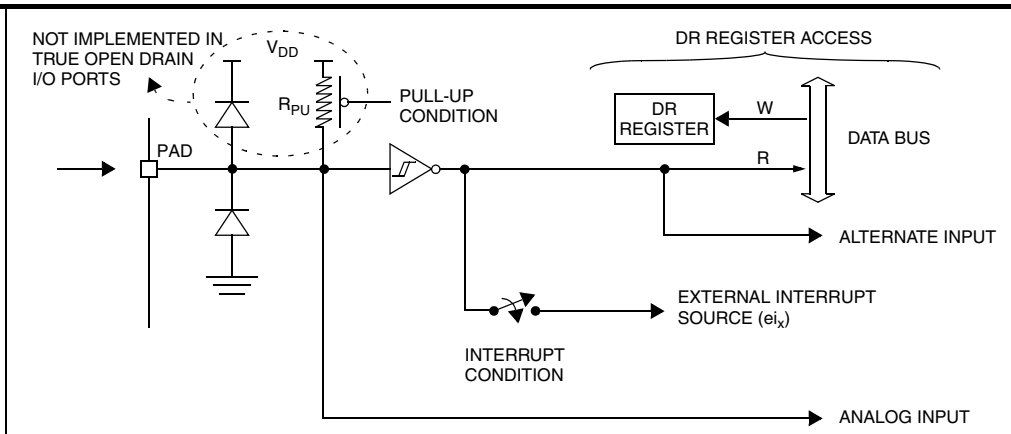
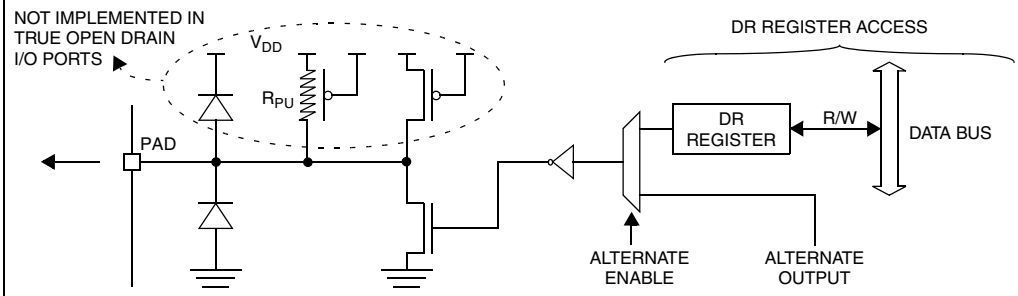
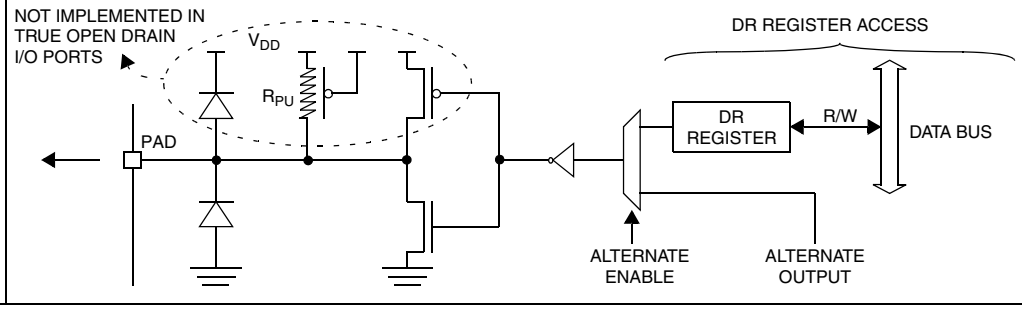


Table 28. I/O port configurations

Hardware configuration	
Input (1)	
Open-drain output (2)	
Push-pull output (2)	

1. When the I/O port is in input configuration and the associated alternate function is enabled as an output, reading the DR register will read the alternate function output status.
2. When the I/O port is in output configuration and the associated alternate function is enabled as an input, the alternate function reads the pin status given by the DR register content.

Caution: The alternate function must not be activated as long as the pin is configured as input with interrupt, in order to avoid generating spurious interrupts.

Analog alternate function

When the pin is used as an ADC input, the I/O must be configured as floating input. The analog multiplexer (controlled by the ADC registers) switches the analog voltage present on the selected pin to the common analog rail which is connected to the ADC input.

11 On-chip peripherals

11.1 Window watchdog (WWDG)

11.1.1 Introduction

The window watchdog is used to detect the occurrence of a software fault, usually generated by external interference or by unforeseen logical conditions, which causes the application program to abandon its normal sequence. The Watchdog circuit generates an MCU reset on expiry of a programmed time period, unless the program refreshes the contents of the downcounter before the T6 bit becomes cleared. An MCU reset is also generated if the 7-bit downcounter value (in the control register) is refreshed before the downcounter has reached the window register value. This implies that the counter must be refreshed in a limited window.

11.1.2 Main features

- Programmable free-running downcounter
- Conditional reset
  - Reset (if watchdog activated) when the downcounter value becomes less than 40h
  - Reset (if watchdog activated) if the downcounter is reloaded outside the window (see *Figure 40*)
- Hardware/Software Watchdog activation (selectable by option byte)
- Optional reset on HALT instruction (configurable by option byte)

11.1.3 Functional description

The counter value stored in the WDGCR register (bits T[6:0]), is decremented every 16384 f_{OSC2} cycles (approx.), and the length of the timeout period can be programmed by the user in 64 increments.

If the watchdog is activated (the WDGA bit is set) and when the 7-bit downcounter (T[6:0] bits) rolls over from 40h to 3Fh (T6 becomes cleared), it initiates a reset cycle pulling low the reset pin for typically 30 µs. If the software reloads the counter while the counter is greater than the value stored in the window register, then a reset is generated.

A minimum of four falling edges of the CPU clock must occur between two consecutive active edges of the external clock; thus, the external clock frequency must be less than a quarter of the CPU clock frequency.

Figure 44. Counter timing diagram, internal clock divided by 2

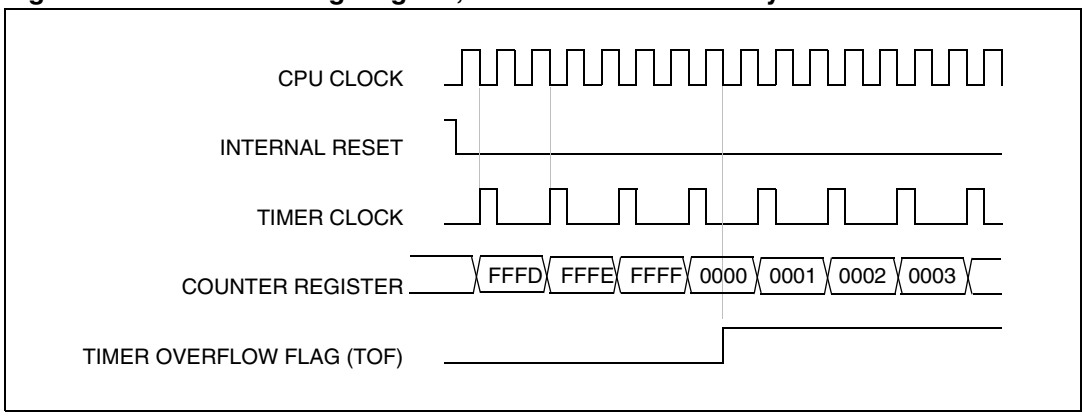


Figure 45. Counter timing diagram, internal clock divided by 4

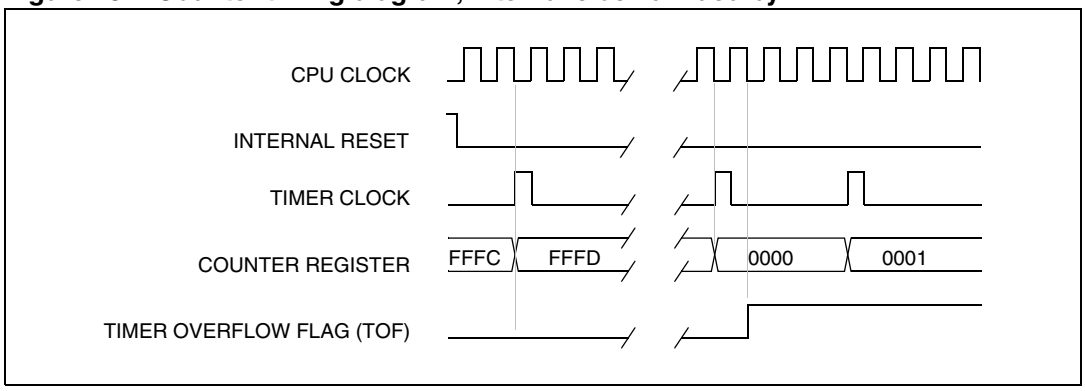
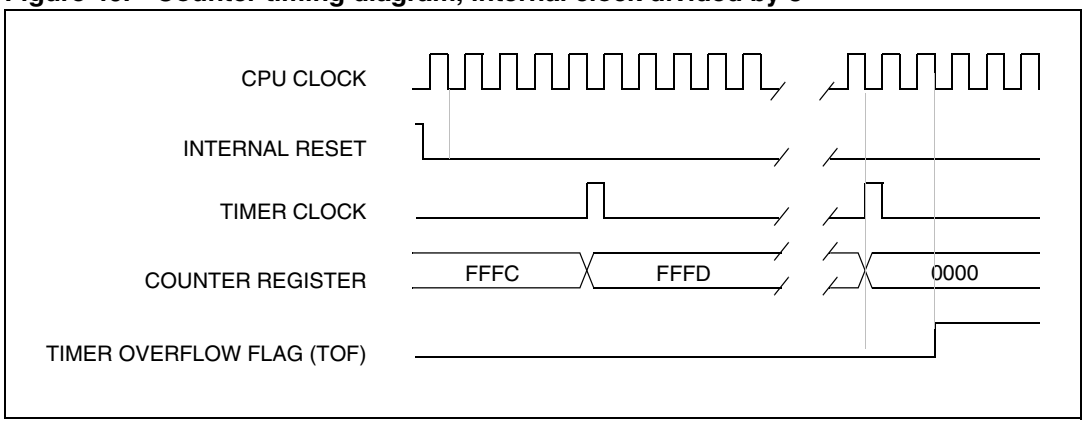


Figure 46. Counter timing diagram, internal clock divided by 8



Note: The device is in reset state when the internal reset signal is high. When it is low, the Device is running.

the ICIE bit is set. This can be avoided if the input capture function i is disabled by reading the ICiHR (see note 1).

6 *The TOF bit can be used with interrupt in order to measure events that go beyond the timer range (FFFFh).*

Figure 47. Input capture block diagram

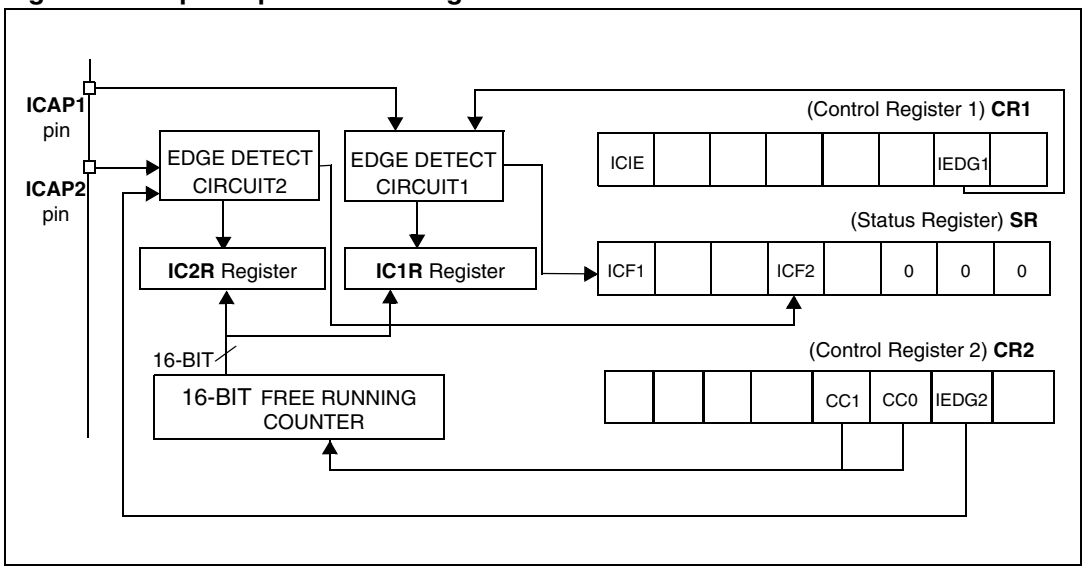
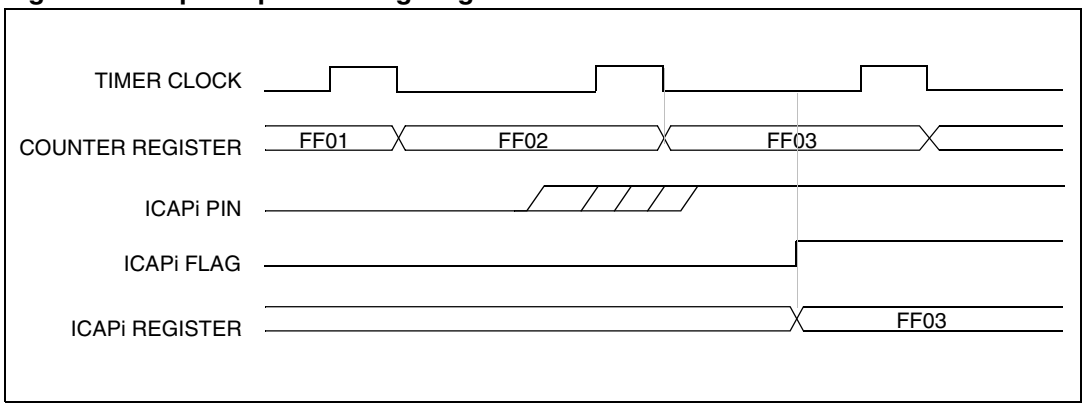


Figure 48. Input capture timing diagram



1. The active edge is the rising edge.
2. The time between an event on the ICAPi pin and the appearance of the corresponding flag is from 2 to 3 CPU clock cycles. This depends on the moment when the ICAP event happens relative to the timer clock.

Output compare

In this section, the index, *i*, may be 1 or 2 because there are 2 output compare functions in the 16-bit timer.

This function can be used to control an output waveform or indicate when a period of time has elapsed.

Table 51. 16-bit timer register map and reset values

Address (Hex.)	Register label	7	6	5	4	3	2	1	0
Timer A: 32 Timer B: 42	CR1 Reset value	ICIE 0	OCIE 0	TOIE 0	FOLV2 0	FOLV1 0	OLVL2 0	IEDG1 0	OLVL1 0
Timer A: 31 Timer B: 41	CR2 Reset value	OC1E 0	OC2E 0	OPM 0	PWM 0	CC1 0	CC0 0	IEDG2 0	EXEDG 0
Timer A: 33 Timer B: 43	CSR Reset value	ICF1 x	OCF1 x	TOF x	ICF2 x	OCF2 x	TIMD 0	- x	- x
Timer A: 34 Timer B: 44	IC1HR Reset value	MSB x	x	x	x	x	x	x	LSB x
Timer A: 35 Timer B: 45	IC1LR Reset value	MSB x	x	x	x	x	x	x	LSB x
Timer A: 36 Timer B: 46	OC1HR Reset value	MSB 1	0	0	0	0	0	0	LSB 0
Timer A: 37 Timer B: 47	OC1LR Reset value	MSB 0	0	0	0	0	0	0	LSB 0
Timer A: 3E Timer B: 4E	OC2HR Reset value	MSB 1	0	0	0	0	0	0	LSB 0
Timer A: 3F Timer B: 4F	OC2LR Reset value	MSB 0	0	0	0	0	0	0	LSB 0
Timer A: 38 Timer B: 48	CHR Reset value	MSB 1	1	1	1	1	1	1	LSB 1
Timer A: 39 Timer B: 49	CLR Reset value	MSB 1	1	1	1	1	1	0	LSB 0
Timer A: 3A Timer B: 4A	ACHR Reset value	MSB 1	1	1	1	1	1	1	LSB 1
Timer A: 3B Timer B: 4B	ACLR Reset value	MSB 1	1	1	1	1	1	0	LSB 0
Timer A: 3C Timer B: 4C	IC2HR Reset value	MSB x	x	x	x	x	x	x	LSB x
Timer A: 3D Timer B: 4D	IC2LR Reset value	MSB x	x	x	x	x	x	x	LSB x

11.5 SCI serial communication interface

11.5.1 Introduction

The serial communications interface (SCI) offers a flexible means of full-duplex data exchange with external equipment requiring an industry standard NRZ asynchronous serial data format. The SCI offers a very wide range of baud rates using two baud rate generator systems.

11.5.2 Main features

- Full-duplex, asynchronous communications
- NRZ standard format (Mark/Space)
- Dual baud rate generator systems
- Independently programmable transmit and receive baud rates up to 500,000 baud
- Programmable data word length (8 or 9 bits)
- Receive buffer full, Transmit buffer empty and End of Transmission flags
- 2 receiver wake-up modes:
  - Address bit (MSB)
  - Idle line
- Muting function for multiprocessor configurations
- Separate enable bits for Transmitter and Receiver
- 4 error detection flags:
  - Overrun error
  - Noise error
  - Frame error
  - Parity error
- 5 interrupt sources with flags:
  - Transmit data register empty
  - Transmission complete
  - Receive data register full
  - Idle line received
  - Overrun error detected
- Parity control:
  - Transmits parity bit
  - Checks parity of received data byte
- Reduced power consumption mode

11.5.3 General description

The interface is externally connected to another device by three pins (see *Figure 63*). Any SCI bidirectional communication requires a minimum of two pins: Receive Data In (RDI) and Transmit Data Out (TDO):

- SCLK: Transmitter clock output. This pin outputs the transmitter data clock for synchronous transmission (no clock pulses on start bit and stop bit, and a software option to send a clock pulse on the last data bit). This can be used to control

11.5.6 Interrupts

Table 58. Interrupt events

Interrupt event	Event flag	Enable control bit	Exit from Wait	Exit from Halt
Transmit data register empty	TDRE	TIE	Yes	No
Transmission complete	TC	TCIE		
Received data ready to be read	RDRF	RIE		
Overrun error detected	OR			
Idle line detected	IDLE	ILIE		
Parity error	PE	PIE		

The SCI interrupt events are connected to the same interrupt vector.

These events generate an interrupt if the corresponding Enable Control Bit is set and the interrupt mask in the CC register is reset (RIM instruction).

11.5.7 Register description

Status register (SCISR)

Reset value: 1100 0000 (C0h)

7							0
TDRE	TC	RDRF	IDLE	OR	NF	FE	PE
Read-only							

Bit 7 = **TDRE** *Transmit data register empty.*

This bit is set by hardware when the content of the TDR register has been transferred into the shift register. An interrupt is generated if the TIE bit = 1 in the SCICR2 register. It is cleared by a software sequence (an access to the SCISR register followed by a write to the SCIDR register).

0: Data is not transferred to the shift register
1: Data is transferred to the shift register

Note: Data is not transferred to the shift register until the TDRE bit is cleared.

Bit 6 = **TC** *Transmission complete.*

This bit is set by hardware when transmission of a frame containing Data is complete. An interrupt is generated if TCIE = 1 in the SCICR2 register. It is cleared by a software sequence (an access to the SCISR register followed by a write to the SCIDR register).

0: Transmission is not complete
1: Transmission is complete

Note: TC is not set after the transmission of a Preamble or a Break.

Bit 5 = **RDRF** *Received data ready flag.*

This bit is set by hardware when the content of the RDR register has been transferred to the SCIDR register. An interrupt is generated if RIE = 1 in the SCICR2 register. It is

Table 59. SCP[1:0] configuration

PR prescaling factor	SCP1	SCP0
1	0	0
3		1
4	1	0
13		1

Bits 5:3 = **SCT[2:0]** *SCI Transmitter rate divisor*

These 3 bits, in conjunction with the SCP1 and SCP0 bits, define the total division applied to the bus clock to yield the transmit rate clock in conventional baud rate Generator mode.

Table 60. SCT[2:0] configuration

TR dividing factor	SCT2	SCT1	SCT0
1	0	0	0
2			1
4		1	0
8			1
16	1	0	0
32			1
64		1	0
128			1

*Note: This TR factor is used only when the ETPR fine tuning factor is equal to 00h; otherwise, TR is replaced by the (TR*ETPR) dividing factor.*

Bits 2:0 = **SCR[2:0]** *SCI Receiver rate divisor.*

These 3 bits, in conjunction with the SCP1 and SCP0 bits, define the total division applied to the bus clock to yield the receive rate clock in conventional Baud Rate Generator mode.

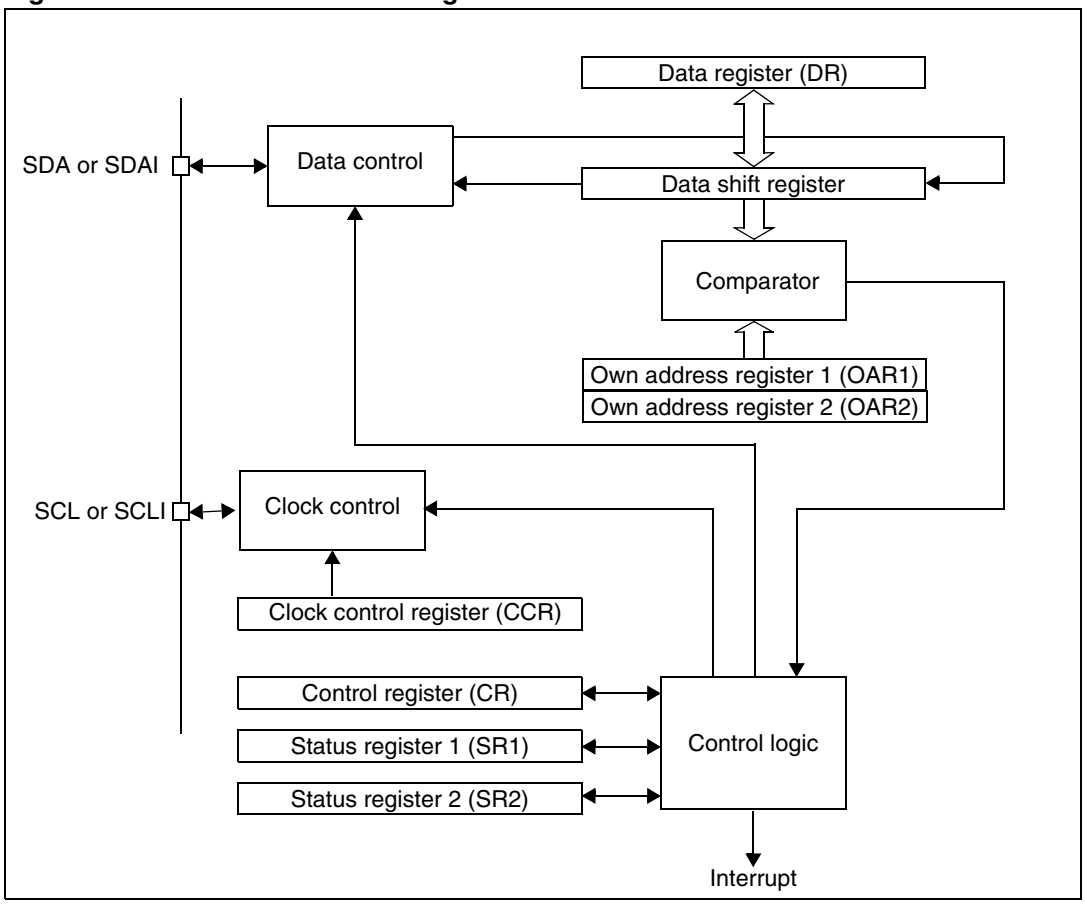
Table 61. SCR[2:0] configuration

RR dividing factor	SCR2	SCR1	SCR0
1	0	0	0
2			1
4		1	0
8			1
16	1	0	0
32			1
64		1	0
128			1

When the I²C cell is enabled, the SDA and SCL ports must be configured as floating inputs. In this case, the value of the external pull-up resistor used depends on the application.

When the I²C cell is disabled, the SDA and SCL ports revert to being standard I/O port pins.

Figure 68. I²C interface block diagram



11.6.4 Functional description

Refer to the CR, SR1 and SR2 registers in *Section 11.6.7*. for the bit definitions.

By default the I²C interface operates in Slave mode (M/SL bit is cleared) except when it initiates a transmit or receive sequence.

First the interface frequency must be configured using the FRi bits in the OAR2 register.

Slave mode

As soon as a start condition is detected, the address is received from the SDA line and sent to the shift register; then it is compared with the address of the interface or the General Call address (if selected by software).

Note: In 10-bit addressing mode, the comparison includes the header sequence (11110xx0) and the two most significant bits of the address.

Header matched (10-bit mode only): the interface generates an acknowledge pulse if the ACK bit is set.

11.8.3 Functional description

The conversion is monotonic, meaning that the result never decreases if the analog input does not, and never increases if the analog input does not.

If the input voltage (V_{AIN}) is greater than V_{AREF} (high-level voltage reference), then the conversion result is FFh in the ADCDRH register and 03h in the ADCDRL register (without overflow indication).

If the input voltage (V_{AIN}) is lower than V_{SSA} (low-level voltage reference), then the conversion result in the ADCDRH and ADCDRL registers is 00 00h.

The A/D converter is linear and the digital result of the conversion is stored in the ADCDRH and ADCDRL registers. The accuracy of the conversion is described in *Section 13: Electrical characteristics*.

R_{AIN} is the maximum recommended impedance for an analog input signal. If the impedance is too high, this will result in a loss of accuracy due to leakage and sampling not being completed in the allotted time.

A/D converter configuration

The analog input ports must be configured as input, no pull-up, no interrupt. Refer to the «I/O ports» chapter. Using these pins as analog inputs does not affect the ability of the port to be read as a logic input.

In the ADCCSR register:

– Select the CS[3:0] bits to assign the analog channel to convert.

Starting the conversion

In the ADCCSR register:

- Set the ADON bit to enable the A/D converter and to start the conversion. From this time on, the ADC performs a continuous conversion of the selected channel.

When a conversion is complete:

- The EOC bit is set by hardware.
- The result is in the ADCDR registers.

A read to the ADCDRH resets the EOC bit.

To read the 10 bits, perform the following steps:

1. Poll the EOC bit
2. Read the ADCDRL register
3. Read the ADCDRH register. This clears EOC automatically.

Note: The data is not latched, so both the low and the high data register must be read before the next conversion is complete, so it is recommended to disable interrupts while reading the conversion result.

To read only 8 bits, perform the following steps:

1. Poll the EOC bit
2. Read the ADCDRH register. This clears EOC automatically.

13.8.2 EMI (electromagnetic interference)

Based on a simple application running on the product (toggling 2 LEDs through the I/O ports), the product is monitored in terms of emission. This emission test is in line with the norm SAE J 1752/3 which specifies the board and the loading of each pin.

Table 104. EMI emissions(1)

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{OSC}/f_{CPU}]		Unit
				8/4 MHz	16/8 MHz	
S_{EMI}	Peak level	V_{DD}=5V, T_A=+25°C, SO20 package, conforming to SAE J 1752/3	0.1 MHz to 30 MHz	TBD	TBD	dBµV
			30 MHz to 130 MHz	TBD	TBD	
			130 MHz to 1 GHz	TBD	TBD	
			SAE EMI Level	TBD	TBD	-

1. Data based on characterization results, not tested in production.

13.8.3 Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). Human body model can be simulated. This test conforms to the JESD22-A114A/A115A standard.

Table 105. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C	>2000	V

1. Data based on characterization results, not tested in production.

Static latch-up (LU)

Two complementary static tests are required on 6 parts to assess the latch-up performance.

- A supply overvoltage (applied to each power supply pin)
- A current injection (applied to each input, output and configurable I/O pin) performed on each sample.

This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.

Table 120. Size of sector 0

Sector 0 size	SEC1	SEC0
2k	1	0
4k	1	1

OPT1 = **FMP_R** *Read-out protection*

Readout protection, when selected provides a protection against program memory content extraction and against write access to Flash memory. Erasing the option bytes when the FMP_R option is selected will cause the whole memory to be erased first and the device can be reprogrammed. Refer to the ST7 Flash Programming Reference Manual and *Section 4.5* for more details.
0: Read-out protection off
1: Read-out protection on

OPT0 = **FMP_W** *Flash write protection*

This option indicates if the Flash program memory is write protected.
Warning: When this option is selected, the program memory (and the option bit itself) can never be erased or programmed again.
0: Write protection off
1: Write protection on

	Option byte 0								Option byte 1							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
	WDG HALT	WDG SW	LVD1	LVD0	SEC1	SEC0	FMPR	FMPW	RSTC	OSCRANGE 2:0			OSC	DIV2EN	PLL x4x8	PLL OFF
Default value	1	1	1	1	1	1	0	0	1	1	1	1	0	1	1	1

15.1.2 Option byte 1

OPT7 = **RSTC** *reset clock cycle selection*

This option bit selects the number of CPU cycles inserted during the reset phase and when exiting Halt mode. For resonator oscillators, it is advised to select 4096 due to the long crystal stabilization time.
0: Reset phase with 4096 CPU cycles
1: Reset phase with 256 CPU cycles

OPT6:4 = **OSCRANGE[2:0]** *Oscillator range*

When the internal RC oscillator is not selected (Option OSC=1), these option bits select the range of the resonator oscillator current source or the external clock source.

15.1.4 Option byte 3

OPT7:6 = **PKG1:0** *Package selection*

These option bits select the package.

Table 123. Package selection

Version	Selected package	PKG 1	PKG 0
K	LQFP32	0	0
S	LQFP44	0	1
C	LQFP48	1	x

OPT5 = **I2C3S** *I2C3SNS selection*

0: I2C3SNS selected
1: I2C3SNS not selected

OPT4:0 = Reserved. Must be kept at 1.

Table 124. Option byte default values

	Option byte 2								Option byte 3							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
	Reserved								PKG1	PKG0	I2C3S	Reserved				
Default value	1	1	1	1	1	1	1	1	x	x	x	1	1	1	1	1