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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	48 MIPS
Connectivity	EBI/EMI, I²C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	40
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.25V
Data Converters	A/D 32x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f382-gqr

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2. C8051F34x Compatibility

The C8051F38x family is designed to be a pin and code compatible replacement for the C8051F34x device family, with an enhanced feature set. The C8051F38x device should function as a drop-in replacement for the C8051F34x devices in most applications. Table 2.1 lists recommended replacement part numbers for C8051F34x devices. See “2.1. Hardware Incompatibilities” to determine if any changes are necessary when upgrading an existing C8051F34x design to the C8051F38x.

Table 2.1. C8051F38x Replacement Part Numbers

C8051F34x Part Number	C8051F38x Part Number
C8051F340-GQ	C8051F380-GQ
C8051F341-GQ	C8051F382-GQ
C8051F342-GQ	C8051F381-GQ
C8051F342-GM	C8051F381-GM
C8051F343-GQ	C8051F383-GQ
C8051F343-GM	C8051F383-GM
C8051F344-GQ	C8051F380-GQ
C8051F345-GQ	C8051F382-GQ
C8051F346-GQ	C8051F381-GQ
C8051F346-GM	C8051F381-GM
C8051F347-GQ	C8051F383-GQ
C8051F347-GM	C8051F383-GM
C8051F348-GQ	C8051F386-GQ
C8051F349-GQ	C8051F387-GQ
C8051F349-GM	C8051F387-GM
C8051F34A-GQ	C8051F381-GQ
C8051F34A-GM	C8051F381-GM
C8051F34B-GQ	C8051F383-GQ
C8051F34B-GM	C8051F383-GM
C8051F34C-GQ	C8051F384-GQ
C8051F34D-GQ	C8051F385-GQ

3. Pinout and Package Definitions

Table 3.1. Pin Definitions for the C8051F380/1/2/3/4/5/6/7/C

Name	Pin Numbers		Type	Description
	48-pin	32-pin		
V_{DD}	10	6	Power In Power Out	2.7–3.6 V Power Supply Voltage Input. 3.3 V Voltage Regulator Output.
GND	7	3		Ground.
$\overline{RST}$/ C2CK	13	9	D I/O D I/O	Device Reset. Open-drain output of internal POR or V_{DD} monitor. An external source can initiate a system reset by driving this pin low for at least 15 µs. Clock signal for the C2 Debug Interface.
C2D	14	—	D I/O	Bi-directional data signal for the C2 Debug Interface.
P3.0 / C2D	—	10	D I/O D I/O	Port 3.0. See Section 20 for a complete description of Port 3. Bi-directional data signal for the C2 Debug Interface.
REGIN	11	7	Power In	5 V Regulator Input. This pin is the input to the on-chip voltage regulator.
VBUS	12	8	D In	VBUS Sense Input. This pin should be connected to the VBUS signal of a USB network. A 5 V signal on this pin indicates a USB network connection.
D+	8	4	D I/O	USB D+.
D–	9	5	D I/O	USB D–.
P0.0	6	2	D I/O or A In	Port 0.0. See Section 20 for a complete description of Port 0.
P0.1	5	1	D I/O or A In	Port 0.1.
P0.2	4	32	D I/O or A In	Port 0.2.
P0.3	3	31	D I/O or A In	Port 0.3.
P0.4	2	30	D I/O or A In	Port 0.4.
P0.5	1	29	D I/O or A In	Port 0.5.
P0.6	48	28	D I/O or A In	Port 0.6.

5.2. Electrical Characteristics

Table 5.2. Global Electrical Characteristics

–40 to +85 °C, 25 MHz system clock unless otherwise specified.

Parameter	Test Condition	Min	Typ	Max	Unit
Digital Supply Voltage[1]		V_{RST}[1]	3.3	3.6	V
Digital Supply RAM Data Retention Voltage		—	1.5	—	V
SYSCLK (System Clock)[2]		0	—	48	MHz
Specified Operating Temperature Range		–40	—	+85	°C
Digital Supply Current—CPU Active (Normal Mode, fetching instructions from Flash)					
I_{DD}[3]	SYSCLK = 48 MHz, V_{DD} = 3.3 V	—	12	14	mA
	SYSCLK = 24 MHz, V_{DD} = 3.3 V	—	7	8	mA
	SYSCLK = 1 MHz, V_{DD} = 3.3 V	—	0.45	0.85	mA
	SYSCLK = 80 kHz, V_{DD} = 3.3 V	—	280	—	µA
Digital Supply Current—CPU Inactive (Idle Mode, not fetching instructions from Flash)					
Idle I_{DD}[3]	SYSCLK = 48 MHz, V_{DD} = 3.3 V	—	6.5	8	mA
	SYSCLK = 24 MHz, V_{DD} = 3.3 V	—	3.5	5	mA
	SYSCLK = 1 MHz, V_{DD} = 3.3 V	—	0.35	—	mA
	SYSCLK = 80 kHz, V_{DD} = 3.3 V	—	220	—	µA
Digital Supply Current (Stop or Suspend Mode, shut-down)	Oscillator not running (STOP mode), Internal Regulators OFF, V_{DD} = 3.3 V	—	1	—	µA
	Oscillator not running (STOP or SUS-PEND mode), REG0 and REG1 both in low power mode, V_{DD} = 3.3 V.	—	100	—	µA
	Oscillator not running (STOP or SUS-PEND mode), REG0 OFF, V_{DD} = 3.3 V.	—	150	—	µA
Digital Supply Current for USB Module (USB Active Mode[4])	USB Clock = 48 MHz, V_{DD} = 3.3 V	—	8	—	mA

Notes:

1. USB Requires 3.0 V Minimum Supply Voltage.
2. SYSCLK must be at least 32 kHz to enable debugging.
3. Includes normal mode bias current for REG0 and REG1. Does not include current from internal oscillators, USB, or other analog peripherals.
4. An additional 220uA is sourced by the D+ or D- pull-up to the USB bus when the USB pull-up is active.

6.5. ADC0 Analog Multiplexer (C8051F380/1/2/3/C only)

AMUX0 selects the positive and negative inputs to the ADC. The positive input (AIN+) can be connected to individual Port pins, the on-chip temperature sensor, or the positive power supply (V_{DD}). The negative input (AIN-) can be connected to individual Port pins, VREF, or GND. When GND is selected as the negative input, ADC0 operates in Single-ended Mode; at all other times, ADC0 operates in Differential Mode. The ADC0 input channels are selected in the AMX0P and AMX0N registers as described in SFR Definition 6.9 and SFR Definition 6.10.

Important Note About ADC0 Input Configuration: Port pins selected as ADC0 inputs should be configured as analog inputs, and should be skipped by the Digital Crossbar. To configure a Port pin for analog input, set to 0 the corresponding bit in register PnMDIN. To force the Crossbar to skip a Port pin, set to 1 the corresponding bit in register PnSKIP. See Section “20. Port Input/Output” on page 153 for more Port I/O configuration details.

7. Voltage Reference Options

The Voltage reference multiplexer for the ADC is configurable to use an externally connected voltage reference, the on-chip reference voltage generator routed to the VREF pin, the unregulated power supply voltage (V_{DD}), or the regulated 1.8 V internal supply (see Figure 7.1). The REFSL bit in the Reference Control register (REF0CN, SFR Definition 7.1) selects the reference source for the ADC. For an external source or the on-chip reference, REFSL should be set to 0 to select the VREF pin. To use V_{DD} as the reference source, REFSL should be set to 1. To override this selection and use the internal regulator as the reference source, the REGOVR bit can be set to 1.

The BIASE bit enables the internal voltage bias generator, which is used by many of the analog peripherals on the device. This bias is automatically enabled when any peripheral which requires it is enabled, and it does not need to be enabled manually. The bias generator may be enabled manually by writing a 1 to the BIASE bit in register REF0CN. The electrical specifications for the voltage reference circuit are given in Table 5.12.

The C8051F380/1/2/3/C devices also include an on-chip voltage reference circuit which consists of a 1.2 V, temperature stable bandgap voltage reference generator and a selectable-gain output buffer amplifier. The buffer is configured for 1x or 2x gain using the REFBGS bit in register REF0CN. On the 1x gain setting the output voltage is nominally 1.2 V, and on the 2x gain setting the output voltage is nominally 2.4 V. The on-chip voltage reference can be driven on the VREF pin by setting the REFBE bit in register REF0CN to a 1. The maximum load seen by the VREF pin must be less than 200 µA to GND. Bypass capacitors of 0.1 µF and 4.7 µF are recommended from the VREF pin to GND, and a minimum of 0.1uF is required. If the on-chip reference is not used, the REFBE bit should be cleared to 0. Electrical specifications for the on-chip voltage reference are given in Table 5.12.

Important Note about the VREF Pin: When using either an external voltage reference or the on-chip reference circuitry, the VREF pin should be configured as an analog pin and skipped by the Digital Crossbar. Refer to Section “20. Port Input/Output” on page 153 for the location of the VREF pin, as well as details of how to configure the pin in analog mode and to be skipped by the crossbar.

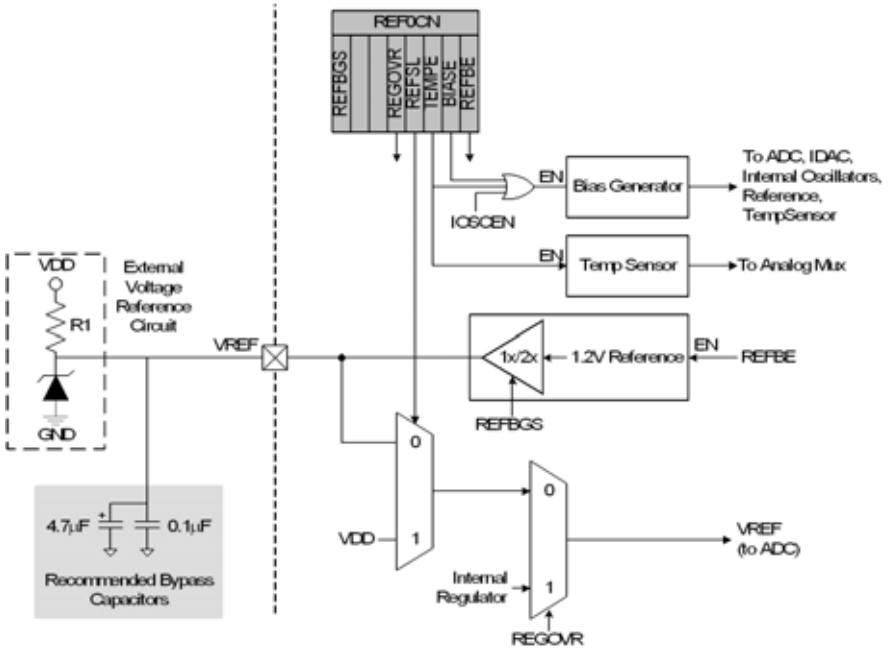


Figure 7.1. Voltage Reference Functional Block Diagram

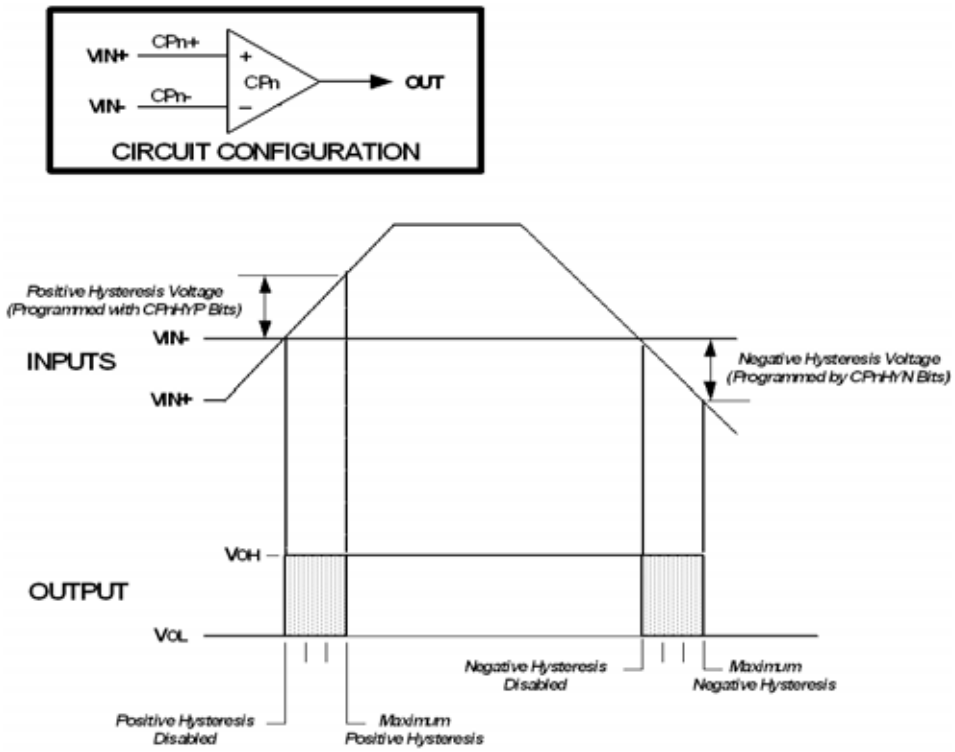


Figure 8.3. Comparator Hysteresis Plot

The Comparator hysteresis is software-programmable via its Comparator Control register CPTnCN (for n = 0 or 1). The user can program both the amount of hysteresis voltage (referred to the input voltage) and the positive and negative-going symmetry of this hysteresis around the threshold voltage.

The Comparator hysteresis is programmed using Bits 3–0 in the Comparator Control Register CPTnCN (shown in SFR Definition 8.1). The amount of negative hysteresis voltage is determined by the settings of the CPnHYN bits. Settings of 20, 10 or 5 mV of nominal negative hysteresis can be programmed, or negative hysteresis can be disabled. In a similar way, the amount of positive hysteresis is determined by the setting the CPnHYP bits.

Comparator interrupts can be generated on both rising-edge and falling-edge output transitions. (For Interrupt enable and priority control, see Section “16.1. MCU Interrupt Sources and Vectors” on page 119). The CPnFIF flag is set to logic 1 upon a Comparator falling-edge occurrence, and the CPnRIF flag is set to logic 1 upon the Comparator rising-edge occurrence. Once set, these bits remain set until cleared by software. The Comparator rising-edge interrupt mask is enabled by setting CPnRIE to a logic 1. The Comparator falling-edge interrupt mask is enabled by setting CPnFIE to a logic 1.

The output state of the Comparator can be obtained at any time by reading the CPnOUT bit. The Comparator is enabled by setting the CPnEN bit to logic 1, and is disabled by clearing this bit to logic 0.

Note that false rising edges and falling edges can be detected when the comparator is first powered on or if changes are made to the hysteresis or response time control bits. Therefore, it is recommended that the rising-edge and falling-edge flags be explicitly cleared to logic 0 a short time after the comparator is enabled or its mode bits have been changed.

Notes on Registers, Operands and Addressing Modes:
Rn - Register R0–R7 of the currently selected register bank. **@Ri** - Data RAM location addressed indirectly through R0 or R1. **rel** - 8-bit, signed (two's complement) offset relative to the first byte of the following instruction. Used by SJMP and all conditional jumps. **direct** - 8-bit internal data location's address. This could be a direct-access Data RAM location (0x00–0x7F) or an SFR (0x80–0xFF). **#data** - 8-bit constant **#data16** - 16-bit constant **bit** - Direct-accessed bit in Data RAM or SFR **addr11** - 11-bit destination address used by ACALL and AJMP. The destination must be within the same 2 kB page of program memory as the first byte of the following instruction. **addr16** - 16-bit destination address used by LCALL and LJMP. The destination may be anywhere within the 8 kB program memory space. There is one unused opcode (0xA5) that performs the same function as NOP. All mnemonics copyrighted © Intel Corporation 1980.

Table 15.2. Special Function Registers (Continued)

SFRs are listed in alphabetical order. All undefined SFR locations are reserved

Register	Address	Page	Description	Page
TMR5RLL	0xCA	F	Timer/Counter 5 Reload Low	296
USB0ADR	0x96	All Pages	USB0 Indirect Address Register	176
USB0DAT	0x97	All Pages	USB0 Data Register	177
USB0XCN	0xD7	All Pages	USB0 Transceiver Control	174
VDM0CN	0xFF	All Pages	V_{DD} Monitor Control	132
XBR0	0xE1	All Pages	Port I/O Crossbar Control 0	159
XBR1	0xE2	All Pages	Port I/O Crossbar Control 1	160
XBR2	0xE3	All Pages	Port I/O Crossbar Control 2	161

17.6. PCA Watchdog Timer Reset

The programmable Watchdog Timer (WDT) function of the Programmable Counter Array (PCA) can be used to prevent software from running out of control during a system malfunction. The PCA WDT function can be enabled or disabled by software as described in Section “27.4. Watchdog Timer Mode” on page 308; the WDT is enabled and clocked by SYSCLK / 12 following any reset. If a system malfunction prevents user software from updating the WDT, a reset is generated and the WDTRSF bit (RSTSRC.5) is set to 1. The state of the $\overline{\text{RST}}$ pin is unaffected by this reset.

17.7. Flash Error Reset

If a Flash program read, write, or erase operation targets an illegal address, a system reset is generated. This may occur due to any of the following:

- Programming hardware attempts to write or erase a Flash location which is above the user code space address limit.
- A Flash read from firmware is attempted above user code space. This occurs when a MOVC operation is attempted above the user code space address limit.
- A Program read is attempted above user code space. This occurs when user code attempts to branch to an address above the user code space address limit.
- A Flash read, write, or erase attempt is restricted due to a Flash security setting.
- A Flash write or erase is attempted when the V_{DD} monitor is not enabled.

The FERROR bit (RSTSRC.6) is set following a Flash error reset. The state of the $\overline{\text{RST}}$ pin is unaffected by this reset.

17.8. Software Reset

Software may force a reset by writing a 1 to the SWRSF bit (RSTSRC.4). The SWRSF bit will read 1 following a software forced reset. The state of the $\overline{\text{RST}}$ pin is unaffected by this reset.

17.9. USB Reset

Writing 1 to the USBRSF bit in register RSTSRC selects USB0 as a reset source. With USB0 selected as a reset source, a system reset will be generated when either of the following occur:

1. RESET signaling is detected on the USB network. The USB Function Controller (USB0) must be enabled for RESET signaling to be detected. See Section “21. Universal Serial Bus Controller (USB0)” on page 172 for information on the USB Function Controller.
2. A falling or rising voltage on the VBUS pin.

The USBRSF bit will read 1 following a USB reset. The state of the $\overline{\text{RST}}$ pin is unaffected by this reset.

18. Flash Memory

On-chip, re-programmable Flash memory is included for program code and non-volatile data storage. The Flash memory can be programmed in-system through the C2 interface or by software using the MOVX instruction. Once cleared to logic 0, a Flash bit must be erased to set it back to logic 1. Flash bytes would typically be erased (set to 0xFF) before being reprogrammed. The write and erase operations are automatically timed by hardware for proper execution; data polling to determine the end of the write/erase operation is not required. Code execution is stalled during a Flash write/erase operation.

18.1. Programming The Flash Memory

The simplest means of programming the Flash memory is through the C2 interface using programming tools provided by Silicon Labs or a third party vendor. This is the only means for programming a non-initialized device. For details on the C2 commands to program Flash memory, see Section “28. C2 Interface” on page 316.

To ensure the integrity of Flash contents, it is strongly recommended that the V_{DD} monitor be left enabled in any system which writes or erases Flash memory from code. It is also crucial to ensure that the FLRT bit in register FLSCL be set to '1' if a clock speed higher than 25 MHz is being used for the device.

18.1.1. Flash Lock and Key Functions

Flash writes and erases by user software are protected with a lock and key function. The Flash Lock and Key Register (FLKEY) must be written with the correct key codes, in sequence, before Flash operations may be performed. The key codes are: 0xA5, 0xF1. The timing does not matter, but the codes must be written in order. If the key codes are written out of order, or the wrong codes are written, Flash writes and erases will be disabled until the next system reset. Flash writes and erases will also be disabled if a Flash write or erase is attempted before the key codes have been written properly. The Flash lock resets after each write or erase; the key codes must be written again before a following Flash operation can be performed. The FLKEY register is detailed in SFR Definition 18.2.

18.1.2. Flash Erase Procedure

The Flash memory can be programmed by software using the MOVX write instruction with the address and data byte to be programmed provided as normal operands. Before writing to Flash memory using MOVX, Flash write operations must be enabled by: (1) Writing the Flash key codes in sequence to the Flash Lock register (FLKEY); and (2) Setting the PSWE Program Store Write Enable bit (PSCTL.0) to logic 1 (this directs the MOVX writes to target Flash memory). The PSWE bit remains set until cleared by software.

A write to Flash memory can clear bits to logic 0 but cannot set them; only an erase operation can set bits to logic 1 in Flash. **A byte location to be programmed must be erased before a new value is written.** The Flash memory is organized in 512-byte pages. The erase operation applies to an entire page (setting all bytes in the page to 0xFF). To erase an entire 512-byte page, perform the following steps:

1. Disable interrupts (recommended).
2. Write the first key code to FLKEY: 0xA5.
3. Write the second key code to FLKEY: 0xF1.
4. Set the PSEE bit (register PSCTL).
5. Set the PSWE bit (register PSCTL).
6. Using the MOVX instruction, write a data byte to any location within the 512-byte page to be erased.
7. Clear the PSWE bit (register PSCTL).
8. Clear the PSEE bit (register PSCTI).

19.4. Clock Multiplier

The C8051F380/1/2/3/4/5/6/7/C device includes a 48 MHz high-frequency oscillator instead of a 12 MHz oscillator and a 4x Clock Multiplier, so the USB0 module can be run directly from the internal high-frequency oscillator. For compatibility with C8051F34x and C8051F32x devices however, the CLKMUL register (SFR Definition 19.4) behaves as if the Clock Multiplier is present and working.

SFR Definition 19.4. CLKMUL: Clock Multiplier Control

Bit	7	6	5	4	3	2	1	0
Name	MULEN	MULINIT	MULRDY				MULSEL[1:0]	
Type	R	R	R	R	R	R	R	
Reset	1	1	1	0	0	0	0	0

SFR Address = 0xB9; SFR Page = 0

Bit	Name	Description
7	MULEN	**Clock Multiplier Enable Bit.** This bit always reads 1.
6	MULINIT	**Clock Multiplier Initialize Bit.** This bit always reads 1.
5	MULRDY	**Clock Multiplier Ready Bit.** This bit always reads 1.
4:2	Unused	Read = 000b; Write = don't care
1:0	MULSEL[1:0]	**Clock Multiplier Input Select Bits.** These bits always read 00.

19.6. External Oscillator Drive Circuit

The external oscillator circuit may drive an external crystal, ceramic resonator, capacitor, or RC network. A CMOS clock may also provide a clock input. Figure 19.1 shows a block diagram of the four external oscillator options. The external oscillator is enabled and configured using the OSCXCN register (see SFR Definition 19.6).

Important Note on External Oscillator Usage: Port pins must be configured when using the external oscillator circuit. When the external oscillator drive circuit is enabled in crystal/resonator mode, Port pins P0.2 and P0.3 are used as XTAL1 and XTAL2, respectively. When the external oscillator drive circuit is enabled in capacitor, RC, or CMOS clock mode, Port pin P0.3 is used as XTAL2. The Port I/O Crossbar should be configured to skip the Port pin used by the oscillator circuit; see Section “20.1. Priority Crossbar Decoder” on page 154 for Crossbar configuration. Additionally, when using the external oscillator circuit in crystal/resonator, capacitor, or RC mode, the associated Port pins should be configured as **analog inputs**. In CMOS clock mode, the associated pin should be configured as a **digital input**. See Section “20.2. Port I/O Initialization” on page 158 for details on Port input mode selection.

The external oscillator output may be selected as the system clock or used to clock some of the digital peripherals (e.g. Timers, PCA, etc.). See the data sheet chapters for each digital peripheral for details. See Section “5. Electrical Characteristics” on page 37 for complete oscillator specifications.

19.6.1. External Crystal Mode

If a crystal or ceramic resonator is used as the external oscillator, the crystal/resonator and a 10 MΩ resistor must be wired across the XTAL1 and XTAL2 pins as shown in Figure 19.1, “Crystal Mode”. Appropriate loading capacitors should be added to XTAL1 and XTAL2, and both pins should be configured for analog I/O with the digital output drivers disabled.

The capacitors shown in the external crystal configuration provide the load capacitance required by the crystal for correct oscillation. These capacitors are “in series” as seen by the crystal and “in parallel” with the stray capacitance of the XTAL1 and XTAL2 pins.

Note: The recommended load capacitance depends upon the crystal and the manufacturer. Refer to the crystal data sheet when completing these calculations.

The equation for determining the load capacitance for two capacitors is

$$C_L = \frac{C_A \times C_B}{C_A + C_B} + C_S$$

Where:
C_A and C_B are the capacitors connected to the crystal leads.
C_S is the total stray capacitance of the PCB.
The stray capacitance for a typical layout where the crystal is as close as possible to the pins is 2-5 pF per pin.

If C_A and C_B are the same (C), then the equation becomes

$$C_L = \frac{C}{2} + C_S$$

For example, a tuning-fork crystal of 32 kHz with a recommended load capacitance of 12.5 pF should use the configuration shown in Figure 19.1, Option 1. With a stray capacitance of 3 pF per pin (6 pF total), the 13 pF capacitors yield an equivalent capacitance of 12.5 pF across the crystal, as shown in Figure 19.2.

SFR Definition 20.16. P3: Port 3

Bit	7	6	5	4	3	2	1	0
Name	P3[7:0]							
Type	R/W							
Reset	1	1	1	1	1	1	1	1

SFR Address = 0xB0; SFR Page = All Pages; Bit Addressable

Bit	Name	Description	Write	Read
7:0	P3[7:0]	**Port 3 Data.** Sets the Port latch logic value or reads the Port pin logic state in Port cells configured for digital I/O.	0: Set output latch to logic LOW. 1: Set output latch to logic HIGH.	0: P3.n Port pin is logic LOW. 1: P3.n Port pin is logic HIGH.

SFR Definition 20.17. P3MDIN: Port 3 Input Mode

Bit	7	6	5	4	3	2	1	0
Name	P3MDIN[7:0]							
Type	R/W							
Reset	1	1	1	1	1	1	1	1

SFR Address = 0xF4; SFR Page = All Pages

Bit	Name	Function
7:0	P3MDIN[7:0]	**Analog Configuration Bits for P3.7–P3.0 (respectively).** Port pins configured for analog mode have their weak pullup, digital driver, and digital receiver disabled. 0: Corresponding P3.n pin is configured for analog mode. 1: Corresponding P3.n pin is not configured for analog mode.

Table 22.3. Sources for Hardware Changes to SMBnCN

Bit	Set by Hardware When:	Cleared by Hardware When:
MASTERn	■ A START is generated.	■ A STOP is generated. ■ Arbitration is lost.
TXMODEn	■ START is generated. ■ SMBnDAT is written before the start of an SMBus frame.	■ A START is detected. ■ Arbitration is lost. ■ SMBnDAT is not written before the start of an SMBus frame.
STAn	■ A START followed by an address byte is received.	■ Must be cleared by software.
STOn	■ A STOP is detected while addressed as a slave. ■ Arbitration is lost due to a detected STOP.	■ A pending STOP is generated.
ACKRQn	■ A byte has been received and an ACK response value is needed (only when hardware ACK is not enabled).	■ After each ACK cycle.
ARBLOSTn	■ A repeated START is detected as a MASTER when STAn is low (unwanted repeated START). ■ SCLn is sensed low while attempting to generate a STOP or repeated START condition. ■ SDAn is sensed low while transmitting a 1 (excluding ACK bits).	■ Each time SIn is cleared.
ACKn	■ The incoming ACK value is low (ACKNOWLEDGE).	■ The incoming ACK value is high (NOT ACKNOWLEDGE).
SIn	■ A START has been generated. ■ Lost arbitration. ■ A byte has been transmitted and an ACK/NACK received. ■ A byte has been received. ■ A START or repeated START followed by a slave address + R/W has been received. ■ A STOP has been received.	■ Must be cleared by software.

22.4.4. Hardware Slave Address Recognition

The SMBus hardware has the capability to automatically recognize incoming slave addresses and send an ACK without software intervention. Automatic slave address recognition is enabled by setting the EHACK bit in register SMB0ADM to 1. This will enable both automatic slave address recognition and automatic hardware ACK generation for received bytes (as a master or slave). More detail on automatic hardware ACK generation can be found in Section 22.4.3.2.

The registers used to define which address(es) are recognized by the hardware are the SMBus Slave Address register and the SMBus Slave Address Mask register. A single address or range of addresses (including the General Call Address 0x00) can be specified using these two registers. The most-significant seven bits of the two registers are used to define which addresses will be ACKed. A 1 in bit positions of the slave address mask SLVM[6:0] enable a comparison between the received slave address and the hardware's slave address SLV[6:0] for those bits. A 0 in a bit of the slave address mask means that bit will be treated as a "don't care" for comparison purposes. In this case, either a 1 or a 0 value are acceptable on

Table 22.5. SMBus Status Decoding: Hardware ACK Disabled (EHACK = 0) (Continued)

Mode	Values Read				Current SMbus State	Typical Response Options	Values to Write			Next Status Vector Expected
	Status Vector	ACKRQ	ARBLOST	ACK			STA	STO	ACK	
Slave Transmitter	0100	0	0	0	A slave byte was transmitted; NACK received.	No action required (expecting STOP condition).	0	0	X	0001
		0	0	1	A slave byte was transmitted; ACK received.	Load SMB0DAT with next data byte to transmit.	0	0	X	0100
		0	1	X	A Slave byte was transmitted; error detected.	No action required (expecting Master to end transfer).	0	0	X	0001
	0101	0	X	X	An illegal STOP or bus error was detected while a Slave Transmission was in progress.	Clear STO.	0	0	X	—
Slave Receiver	0010	1	0	X	A slave address + R/W was received; ACK requested.	If Write, Acknowledge received address	0	0	1	0000
						If Read, Load SMB0DAT with data byte; ACK received address	0	0	1	0100
						NACK received address.	0	0	0	—
		1	1	X	Lost arbitration as master; slave address + R/W received; ACK requested.	If Write, Acknowledge received address	0	0	1	0000
						If Read, Load SMB0DAT with data byte; ACK received address	0	0	1	0100
						NACK received address.	0	0	0	—
						Reschedule failed transfer; NACK received address.	1	0	0	1110
	0001	0	0	X	A STOP was detected while addressed as a Slave Transmitter or Slave Receiver.	Clear STO.	0	0	X	—
		1	1	X	Lost arbitration while attempting a STOP.	No action required (transfer complete/aborted).	0	0	0	—
	0000	1	0	X	A slave byte was received; ACK requested.	Acknowledge received byte; Read SMB0DAT.	0	0	1	0000
						NACK received byte.	0	0	0	—

SFR Definition 26.3. TCON: Timer Control

Bit	7	6	5	4	3	2	1	0
Name	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x88; SFR Page = All Pages; Bit-Addressable

Bit	Name	Function
7	TF1	**Timer 1 Overflow Flag.** Set to 1 by hardware when Timer 1 overflows. This flag can be cleared by software but is automatically cleared when the CPU vectors to the Timer 1 interrupt service routine.
6	TR1	**Timer 1 Run Control.** Timer 1 is enabled by setting this bit to 1.
5	TF0	**Timer 0 Overflow Flag.** Set to 1 by hardware when Timer 0 overflows. This flag can be cleared by software but is automatically cleared when the CPU vectors to the Timer 0 interrupt service routine.
4	TR0	**Timer 0 Run Control.** Timer 0 is enabled by setting this bit to 1.
3	IE1	**External Interrupt 1.** This flag is set by hardware when an edge/level of type defined by IT1 is detected. It can be cleared by software but is automatically cleared when the CPU vectors to the External Interrupt 1 service routine in edge-triggered mode.
2	IT1	**Interrupt 1 Type Select.** This bit selects whether the configured $\overline{\text{INT1}}$ interrupt will be edge or level sensitive. $\overline{\text{INT1}}$ is configured active low or high by the IN1PL bit in the IT01CF register (see SFR Definition 16.7). 0: $\overline{\text{INT1}}$ is level triggered. 1: $\overline{\text{INT1}}$ is edge triggered.
1	IE0	**External Interrupt 0.** This flag is set by hardware when an edge/level of type defined by IT1 is detected. It can be cleared by software but is automatically cleared when the CPU vectors to the External Interrupt 0 service routine in edge-triggered mode.
0	IT0	**Interrupt 0 Type Select.** This bit selects whether the configured $\overline{\text{INT0}}$ interrupt will be edge or level sensitive. $\overline{\text{INT0}}$ is configured active low or high by the IN0PL bit in register IT01CF (see SFR Definition 16.7). 0: $\overline{\text{INT0}}$ is level triggered. 1: $\overline{\text{INT0}}$ is edge triggered.

C2 Register Definition 28.4. FPCTL: C2 Flash Programming Control

Bit	7	6	5	4	3	2	1	0
Name	FPCTL[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

C2 Address: 0x02

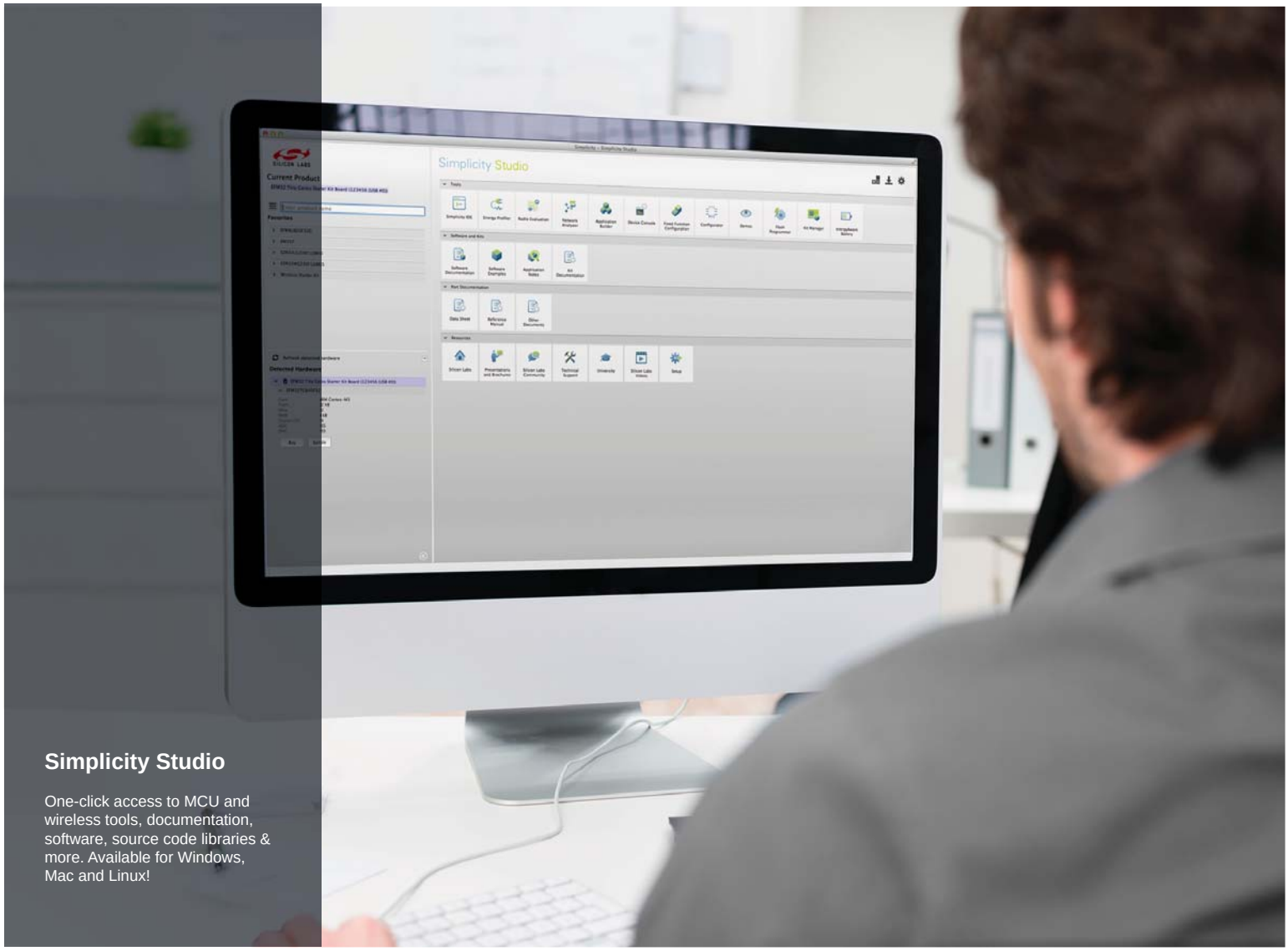
Bit	Name	Function
7:0	FPCTL[7:0]	**Flash Programming Control Register.** This register is used to enable Flash programming via the C2 interface. To enable C2 Flash programming, the following codes must be written in order: 0x02, 0x01. Note that once C2 Flash programming is enabled, a system reset must be issued to resume normal operation.

C2 Register Definition 28.5. FPDAT: C2 Flash Programming Data

Bit	7	6	5	4	3	2	1	0
Name	FPDAT[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

C2 Address: 0xAD

Bit	Name	Function	
7:0	FPDAT[7:0]	**C2 Flash Programming Data Register.** This register is used to pass Flash commands, addresses, and data during C2 Flash accesses. Valid commands are listed below.	
		Code	**Command**
		0x06	Flash Block Read
		0x07	Flash Block Write
		0x08	Flash Page Erase
		0x03	Device Erase



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