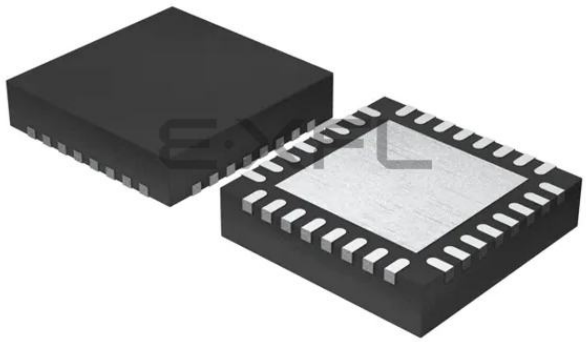

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	48 MIPS
Connectivity	I²C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.25V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f385-gmr

List of Figures

Table 1.1. Product Selection Guide

Ordering Part Number	MIPS (Peak)	Flash Memory (Bytes)	RAM	Calibrated Internal Oscillator	Low Frequency Oscillator	USB with 1k Endpoint RAM	Supply Voltage Regulator	SMBus/I2C	Enhanced SPI	UARTs	Timers (16-bit)	Programmable Counter Array	Digital Port I/O	External Memory Interface (EMIF)	10-bit 500ksps ADC	Temperature Sensor	Voltage Reference	Analog Comparators	Package
C8051F380-GQ	48	64k	4352	✓	✓	✓	✓	2	✓	2	6	✓	40	✓	✓	✓	✓	2	TQFP48
C8051F381-GQ	48	64k	4352	✓	✓	✓	✓	2	✓	2	6	✓	25	—	✓	✓	✓	2	LQFP32
C8051F381-GM	48	64k	4352	✓	✓	✓	✓	2	✓	2	6	✓	25	—	✓	✓	✓	2	QFN32
C8051F382-GQ	48	32k	2304	✓	✓	✓	✓	2	✓	2	6	✓	40	✓	✓	✓	✓	2	TQFP48
C8051F383-GQ	48	32k	2304	✓	✓	✓	✓	2	✓	2	6	✓	25	—	✓	✓	✓	2	LQFP32
C8051F383-GM	48	32k	2304	✓	✓	✓	✓	2	✓	2	6	✓	25	—	✓	✓	✓	2	QFN32
C8051F384-GQ	48	64k	4352	✓	✓	✓	✓	2	✓	2	6	✓	40	✓	—	—	—	2	TQFP48
C8051F385-GQ	48	64k	4352	✓	✓	✓	✓	2	✓	2	6	✓	25	—	—	—	—	2	LQFP32
C8051F385-GM	48	64k	4352	✓	✓	✓	✓	2	✓	2	6	✓	25	—	—	—	—	2	QFN32
C8051F386-GQ	48	32k	2304	✓	✓	✓	✓	2	✓	2	6	✓	40	✓	—	—	—	2	TQFP48
C8051F387-GQ	48	32k	2304	✓	✓	✓	✓	2	✓	2	6	✓	25	—	—	—	—	2	LQFP32
C8051F387-GM	48	32k	2304	✓	✓	✓	✓	2	✓	2	6	✓	25	—	—	—	—	2	QFN32
C8051F38C-GQ	48	16k	2304	✓	✓	✓	✓	2	✓	2	6	✓	25	—	✓	✓	✓	2	LQFP32
C8051F38C-GM	48	16k	2304	✓	✓	✓	✓	2	✓	2	6	✓	25	—	✓	✓	✓	2	QFN32

2.1. Hardware Incompatibilities

While the C8051F38x family includes a number of new features not found on the C8051F34x family, there are some differences that should be considered for any design port.

- **Clock Multiplier**: The C8051F38x does not include the 4x clock multiplier from the C8051F34x device families. This change only impacts systems which use the clock multiplier in conjunction with an external oscillator source.
- **External Oscillator C and RC Modes**: The C and RC modes of the oscillator have a divide-by-2 stage on the C8051F38x to aid in noise immunity. This was not present on the C8051F34x device family, and any clock generated with C or RC mode will change accordingly.
- **Fab Technology**: The C8051F38x is manufactured using a different technology process than the C8051F34x. As a result, many of the electrical performance parameters will have subtle differences. These differences should not affect most systems but it is nonetheless important to review the electrical parameters for any blocks that are used in the design, and ensure they are compatible with the existing hardware.

Table 3.1. Pin Definitions for the C8051F380/1/2/3/4/5/6/7/C (Continued)

Name	Pin Numbers		Type	Description
	48-pin	32-pin		
P3.1	29	—	D I/O or A In	Port 3.1.
P3.2	28	—	D I/O or A In	Port 3.2.
P3.3	27	—	D I/O or A In	Port 3.3.
P3.4	26	—	D I/O or A In	Port 3.4.
P3.5	25	—	D I/O or A In	Port 3.5.
P3.6	24	—	D I/O or A In	Port 3.6.
P3.7	23	—	D I/O or A In	Port 3.7.
P4.0	22	—	D I/O or A In	Port 4.0. See Section 20 for a complete description of Port 4.
P4.1	21	—	D I/O or A In	Port 4.1.
P4.2	20	—	D I/O or A In	Port 4.2.
P4.3	19	—	D I/O or A In	Port 4.3.
P4.4	18	—	D I/O or A In	Port 4.4.
P4.5	17	—	D I/O or A In	Port 4.5.
P4.6	16	—	D I/O or A In	Port 4.6.
P4.7	15	—	D I/O or A In	Port 4.7.

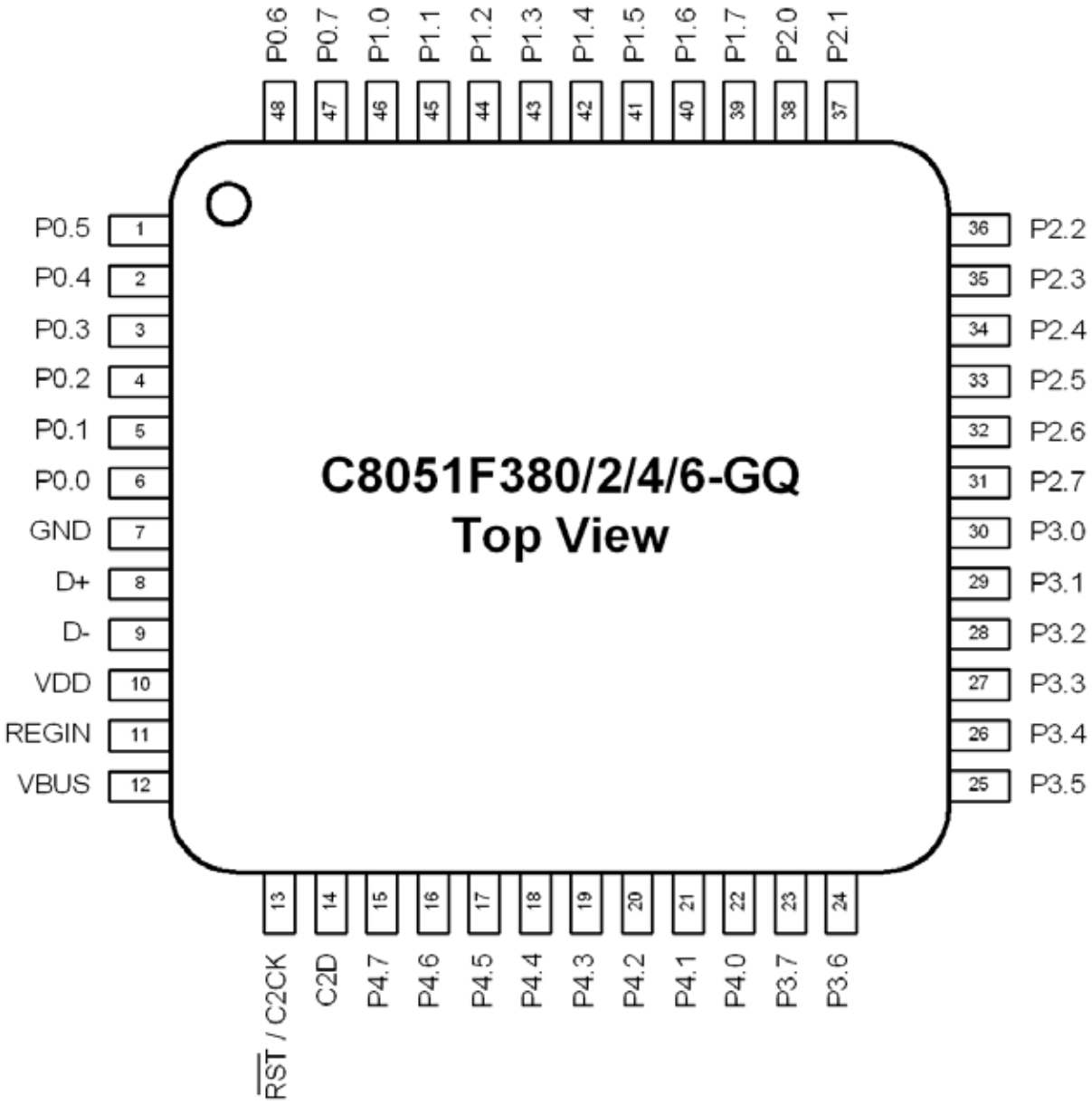

Figure 3.1. TQFP-48 Pinout Diagram (Top View)

Table 5.13. Comparator Electrical Characteristics

V_{DD} = 3.0 V, –40 to +85 °C unless otherwise noted.

Parameter	Test Condition	Min	Typ	Max	Unit
Response Time: Mode 0, Vcm* = 1.5 V	CP0+ – CP0– = 100 mV	—	100	—	ns
	CP0+ – CP0– = –100 mV	—	250	—	ns
Response Time: Mode 1, Vcm* = 1.5 V	CP0+ – CP0– = 100 mV	—	175	—	ns
	CP0+ – CP0– = –100 mV	—	500	—	ns
Response Time: Mode 2, Vcm* = 1.5 V	CP0+ – CP0– = 100 mV	—	320	—	ns
	CP0+ – CP0– = –100 mV	—	1100	—	ns
Response Time: Mode 3, Vcm* = 1.5 V	CP0+ – CP0– = 100 mV	—	1050	—	ns
	CP0+ – CP0– = –100 mV	—	5200	—	ns
Common-Mode Rejection Ratio		—	1.5	4	mV/V
Positive Hysteresis 1	CP0HYP1–0 = 00	—	0	1	mV
Positive Hysteresis 2	CP0HYP1–0 = 01	2	5	10	mV
Positive Hysteresis 3	CP0HYP1–0 = 10	7	10	20	mV
Positive Hysteresis 4	CP0HYP1–0 = 11	15	20	30	mV
Negative Hysteresis 1	CP0HYN1–0 = 00	—	0	1	mV
Negative Hysteresis 2	CP0HYN1–0 = 01	2	5	10	mV
Negative Hysteresis 3	CP0HYN1–0 = 10	7	10	20	mV
Negative Hysteresis 4	CP0HYN1–0 = 11	15	20	30	mV
Inverting or Non-Inverting Input Voltage Range		–0.25	—	V_{DD} + 0.25	V
Input Capacitance		—	4	—	pF
Input Bias Current		—	0.001	—	nA
Input Offset Voltage		–10	—	+10	mV
Power Supply					
Power Supply Rejection		—	0.1	—	mV/V
Power-up Time		—	10	—	µs
Supply Current at DC	Mode 0	—	20	—	µA
	Mode 1	—	10	—	µA
	Mode 2	—	4	—	µA
	Mode 3	—	1	—	µA

Note: Vcm is the common-mode voltage on CP0+ and CP0–.

SFR Definition 8.1. CPT0CN: Comparator0 Control

Bit	7	6	5	4	3	2	1	0
Name	CP0EN	CP0OUT	CP0RIF	CP0FIF	CP0HYP[1:0]		CP0HYN[1:0]	
Type	R/W	R	R/W	R/W	R/W		R/W	
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x9B; SFR Page = All Pages

Bit	Name	Function
7	CP0EN	**Comparator0 Enable Bit.** 0: Comparator0 Disabled. 1: Comparator0 Enabled.
6	CP0OUT	**Comparator0 Output State Flag.** 0: Voltage on CP0+ < CP0–. 1: Voltage on CP0+ > CP0–.
5	CP0RIF	**Comparator0 Rising-Edge Flag. Must be cleared by software.** 0: No Comparator0 Rising Edge has occurred since this flag was last cleared. 1: Comparator0 Rising Edge has occurred.
4	CP0FIF	**Comparator0 Falling-Edge Flag. Must be cleared by software.** 0: No Comparator0 Falling-Edge has occurred since this flag was last cleared. 1: Comparator0 Falling-Edge has occurred.
3:2	CP0HYP[1:0]	**Comparator0 Positive Hysteresis Control Bits.** 00: Positive Hysteresis Disabled. 01: Positive Hysteresis = 5 mV. 10: Positive Hysteresis = 10 mV. 11: Positive Hysteresis = 20 mV.
1:0	CP0HYN[1:0]	**Comparator0 Negative Hysteresis Control Bits.** 00: Negative Hysteresis Disabled. 01: Negative Hysteresis = 5 mV. 10: Negative Hysteresis = 10 mV. 11: Negative Hysteresis = 20 mV.

8.1. Comparator Multiplexers

C8051F380/1/2/3/4/5/6/7/C devices include an analog input multiplexer to connect Port I/O pins to the comparator inputs. The Comparator inputs are selected in the CPTnMX registers (SFR Definition 8.5 and SFR Definition 8.6). The CMXnP2–CMXnP0 bits select the Comparator positive input; the CMXnN2–CMXnN0 bits select the Comparator negative input.

Important Note About Comparator Inputs: The Port pins selected as comparator inputs should be configured as analog inputs in their associated Port configuration register, and configured to be skipped by the Crossbar (for details on Port configuration, see Section “20.3. General Purpose Port I/O” on page 161).

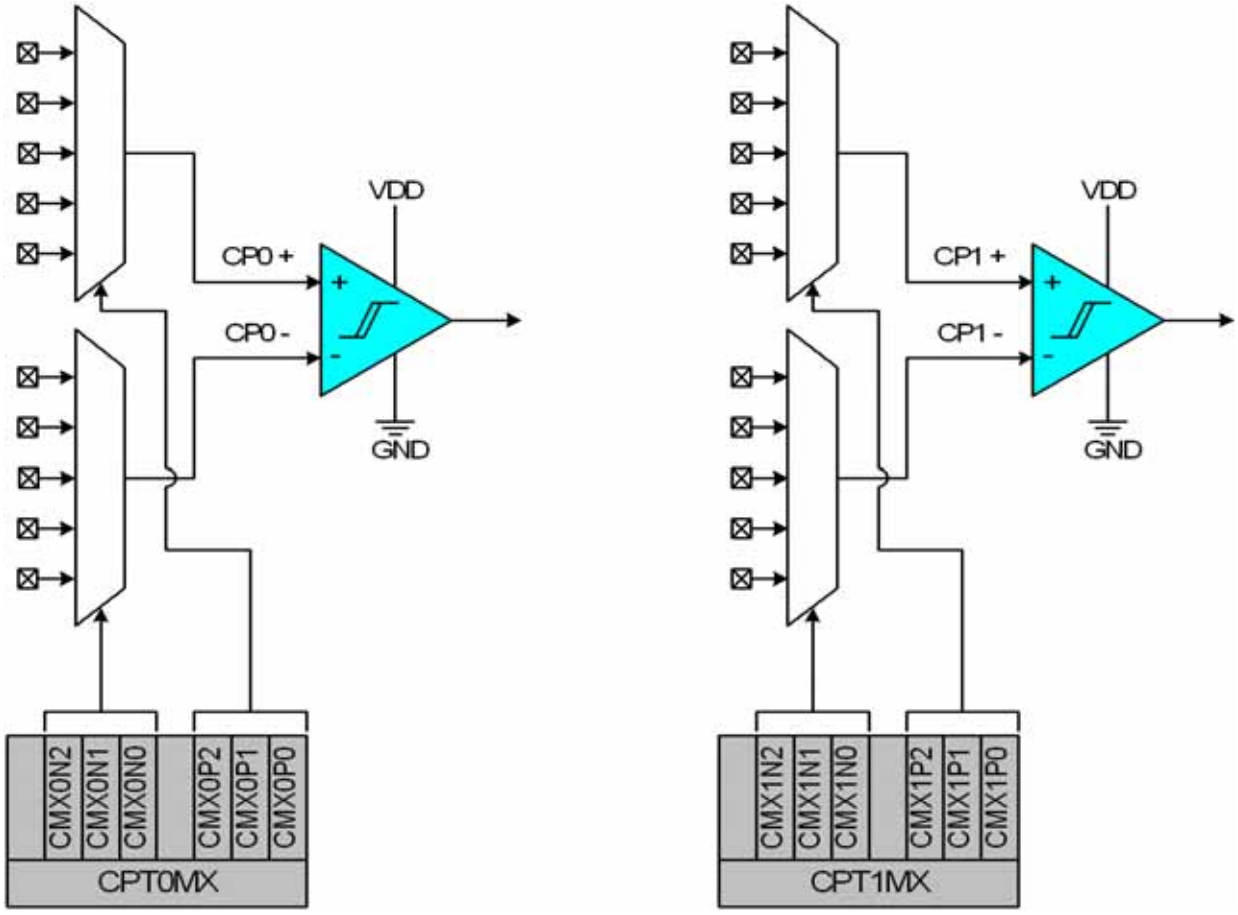

Figure 8.4. Comparator Input Multiplexer Block Diagram

14.6. Memory Mode Selection

The external data memory space can be configured in one of four modes, shown in Figure 14.4, based on the EMIF Mode bits in the EMI0CF register (SFR Definition 14.5). These modes are summarized below. More information about the different modes can be found in Section “14.7. Timing” on page 102.

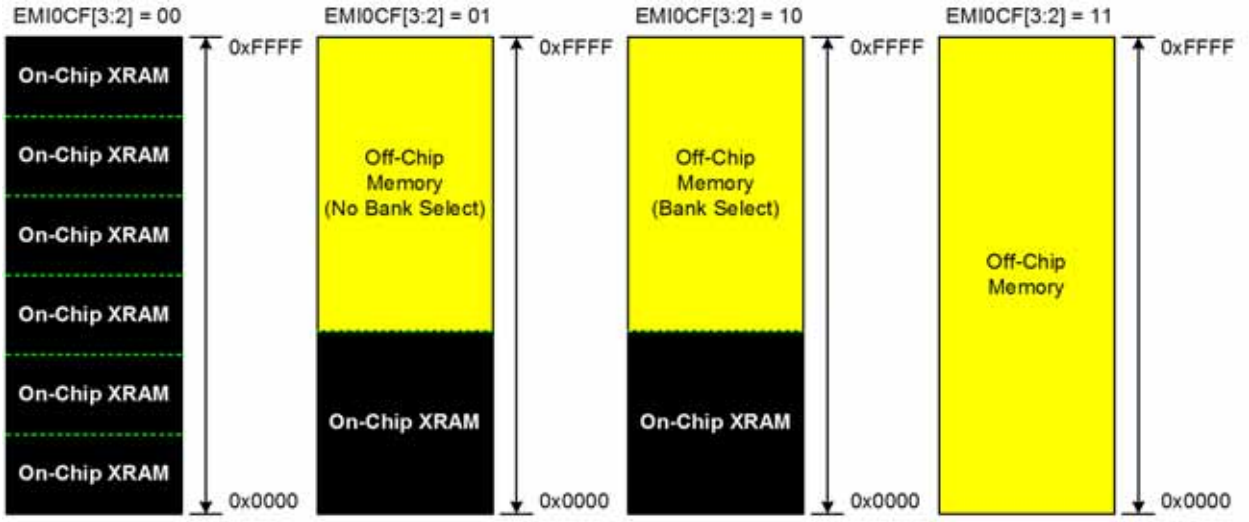

Figure 14.4. EMIF Operating Modes

14.6.1. Internal XRAM Only

When EMI0CF.[3:2] are set to 00, all MOVX instructions will target the internal XRAM space on the device. Memory accesses to addresses beyond the populated space will wrap on 2k or 4k boundaries (depending on the RAM available on the device). As an example, the addresses 0x1000 and 0x2000 both evaluate to address 0x0000 in on-chip XRAM space.

- 8-bit MOVX operations use the contents of EMI0CN to determine the high-byte of the effective address and R0 or R1 to determine the low-byte of the effective address.
- 16-bit MOVX operations use the contents of the 16-bit DPTR to determine the effective address.

14.6.2. Split Mode without Bank Select

When EMI0CF.[3:2] are set to 01, the XRAM memory map is split into two areas, on-chip space and off-chip space.

- Effective addresses below the internal XRAM size boundary will access on-chip XRAM space.
- Effective addresses above the internal XRAM size boundary will access off-chip space.
- 8-bit MOVX operations use the contents of EMI0CN to determine whether the memory access is on-chip or off-chip. However, in the “No Bank Select” mode, an 8-bit MOVX operation will not drive the upper 8-bits A[15:8] of the Address Bus during an off-chip access. This allows the user to manipulate the upper address bits at will by setting the Port state directly via the port latches. This behavior is in contrast with “Split Mode with Bank Select” described below. The lower 8-bits of the Address Bus A[7:0] are driven, determined by R0 or R1.
- 16-bit MOVX operations use the contents of DPTR to determine whether the memory access is on-chip or off-chip, and unlike 8-bit MOVX operations, the full 16-bits of the Address Bus A[15:0] are driven during the off-chip transaction.

Table 15.2. Special Function Registers (Continued)

SFRs are listed in alphabetical order. All undefined SFR locations are reserved

Register	Address	Page	Description	Page
SMB1CN	0xC0	F	SMBus1 Control	216
SMB1DAT	0xC2	F	SMBus1 Data	222
SMBTC	0xB9	F	SMBus0/1 Timing Control	213
SMOD1	0xE5	All Pages	UART1 Mode	246
SP	0x81	All Pages	Stack Pointer	86
SPI0CFG	0xA1	All Pages	SPI Configuration	257
SPI0CKR	0xA2	All Pages	SPI Clock Rate Control	259
SPI0CN	0xF8	All Pages	SPI Control	258
SPI0DAT	0xA3	All Pages	SPI Data	259
TCON	0x88	All Pages	Timer/Counter Control	270
TH0	0x8C	All Pages	Timer/Counter 0 High	273
TH1	0x8D	All Pages	Timer/Counter 1 High	273
TL0	0x8A	All Pages	Timer/Counter 0 Low	272
TL1	0x8B	All Pages	Timer/Counter 1 Low	272
TMOD	0x89	All Pages	Timer/Counter Mode	271
TMR2CN	0xC8	0	Timer/Counter 2 Control	278
TMR2H	0xCD	0	Timer/Counter 2 High	280
TMR2L	0xCC	0	Timer/Counter 2 Low	279
TMR2RLH	0xCB	0	Timer/Counter 2 Reload High	279
TMR2RLL	0xCA	0	Timer/Counter 2 Reload Low	279
TMR3CN	0x91	0	Timer/Counter 3 Control	285
TMR3H	0x95	0	Timer/Counter 3 High	287
TMR3L	0x94	0	Timer/Counter 3 Low	286
TMR3RLH	0x93	0	Timer/Counter 3 Reload High	286
TMR3RLL	0x92	0	Timer/Counter 3 Reload Low	286
TMR4CN	0x91	F	Timer/Counter 4 Control	290
TMR4H	0x95	F	Timer/Counter 4 High	292
TMR4L	0x94	F	Timer/Counter 4 Low	291
TMR4RLH	0x93	F	Timer/Counter 4 Reload High	291
TMR4RLL	0x92	F	Timer/Counter 4 Reload Low	291
TMR5CN	0xC8	F	Timer/Counter 5 Control	295
TMR5H	0xCD	F	Timer/Counter 5 High	297
TMR5L	0xCC	F	Timer/Counter 5 Low	296
TMR5RLH	0xCB	F	Timer/Counter 5 Reload High	296

Table 16.1. Interrupt Summary

Interrupt Source	Interrupt Vector	Priority Order	Pending Flag	Bit Address?	Cleared by HW?	Enable Flag	Priority Control
Reset	0x0000	Top	None	N/A	N/A	Always Enabled	Always Highest
External Interrupt 0 ($\overline{INT0}$)	0x0003	0	IE0 (TCON.1)	Y	Y	EX0 (IE.0)	PX0 (IP.0)
Timer 0 Overflow	0x000B	1	TF0 (TCON.5)	Y	Y	ET0 (IE.1)	PT0 (IP.1)
External Interrupt 1 ($\overline{INT1}$)	0x0013	2	IE1 (TCON.3)	Y	Y	EX1 (IE.2)	PX1 (IP.2)
Timer 1 Overflow	0x001B	3	TF1 (TCON.7)	Y	Y	ET1 (IE.3)	PT1 (IP.3)
UART0	0x0023	4	RI0 (SCON0.0) TI0 (SCON0.1)	Y	N	ES0 (IE.4)	PS0 (IP.4)
Timer 2 Overflow	0x002B	5	TF2H (TMR2CN.7) TF2L (TMR2CN.6)	Y	N	ET2 (IE.5)	PT2 (IP.5)
SPI0	0x0033	6	SPIF (SPI0CN.7) WCOL (SPI0CN.6) MODF (SPI0CN.5) RXOVRN (SPI0CN.4)	Y	N	ESPI0 (IE.6)	PSPI0 (IP.6)
SMB0	0x003B	7	SI (SMB0CN.0)	Y	N	ESMB0 (EIE1.0)	PSMB0 (EIP1.0)
USB0	0x0043	8	Special	N	N	EUSB0 (EIE1.1)	PUSB0 (EIP1.1)
ADC0 Window Compare	0x004B	9	AD0WINT (ADC0CN.3)	Y	N	EWADC0 (EIE1.2)	PWADC0 (EIP1.2)
ADC0 Conversion Complete	0x0053	10	AD0INT (ADC0CN.5)	Y	N	EADC0 (EIE1.3)	PADC0 (EIP1.3)
Programmable Counter Array	0x005B	11	CF (PCA0CN.7) CCFn (PCA0CN.n)	Y	N	EPCA0 (EIE1.4)	PPCA0 (EIP1.4)
Comparator0	0x0063	12	CP0FIF (CPT0CN.4) CP0RIF (CPT0CN.5)	N	N	ECP0 (EIE1.5)	PCP0 (EIP1.5)
Comparator1	0x006B	13	CP1FIF (CPT1CN.4) CP1RIF (CPT1CN.5)	N	N	ECP1 (EIE1.6)	PCP1 (EIP1.6)
Timer 3 Overflow	0x0073	14	TF3H (TMR3CN.7) TF3L (TMR3CN.6)	N	N	ET3 (EIE1.7)	PT3 (EIP1.7)
VBUS Level	0x007B	15	N/A	N/A	N/A	EVBUS (EIE2.0)	PVBUS (EIP2.0)
UART1	0x0083	16	RI1 (SCON1.0) TI1 (SCON1.1)	N	N	ES1 (EIE2.1)	PS1 (EIP2.1)
Reserved	0x008B	17	N/A	N/A	N/A	N/A	N/A
SMB1	0x0093	18	SI (SMB1CN.0)	Y	N	ESMB1 (EIE2.3)	PSMB1 (EIP2.3)
Timer 4 Overflow	0x009B	19	TF4H (TMR4CN.7) TF4L (TMR4CN.6)	N	N	ET4 (EIE2.4)	PT4 (E!P2.4)
Timer 5 Overflow	0x00A3	20	TF5H (TMR5CN.7) TF5L (TMR5CN.6)	Y	N	ET5 (EIE2.5)	PT5 (E!P2.5)

17.1. Power-On Reset

During power-up, the device is held in a reset state and the $\overline{RST}$ pin is driven low until V_{DD} settles above V_{RST}. A delay occurs before the device is released from reset; the delay decreases as the V_{DD} ramp time increases (V_{DD} ramp time is defined as how fast V_{DD} ramps from 0 V to V_{RST}). Figure 17.2. plots the power-on and V_{DD} monitor event timing. The maximum V_{DD} ramp time is 1 ms; slower ramp times may cause the device to be released from reset before V_{DD} reaches the V_{RST} level. For ramp times less than 1 ms, the power-on reset delay ($T_{PORDelay}$) is typically less than 0.3 ms.

On exit from a power-on or V_{DD} monitor reset, the PORSF flag (RSTSRC.1) is set by hardware to logic 1. When PORSF is set, all of the other reset flags in the RSTSRC Register are indeterminate (PORSF is cleared by all other resets). Since all resets cause program execution to begin at the same location (0x0000) software can read the PORSF flag to determine if a power-up was the cause of reset. The content of internal data memory should be assumed to be undefined after a power-on reset. The V_{DD} monitor is enabled following a power-on reset.

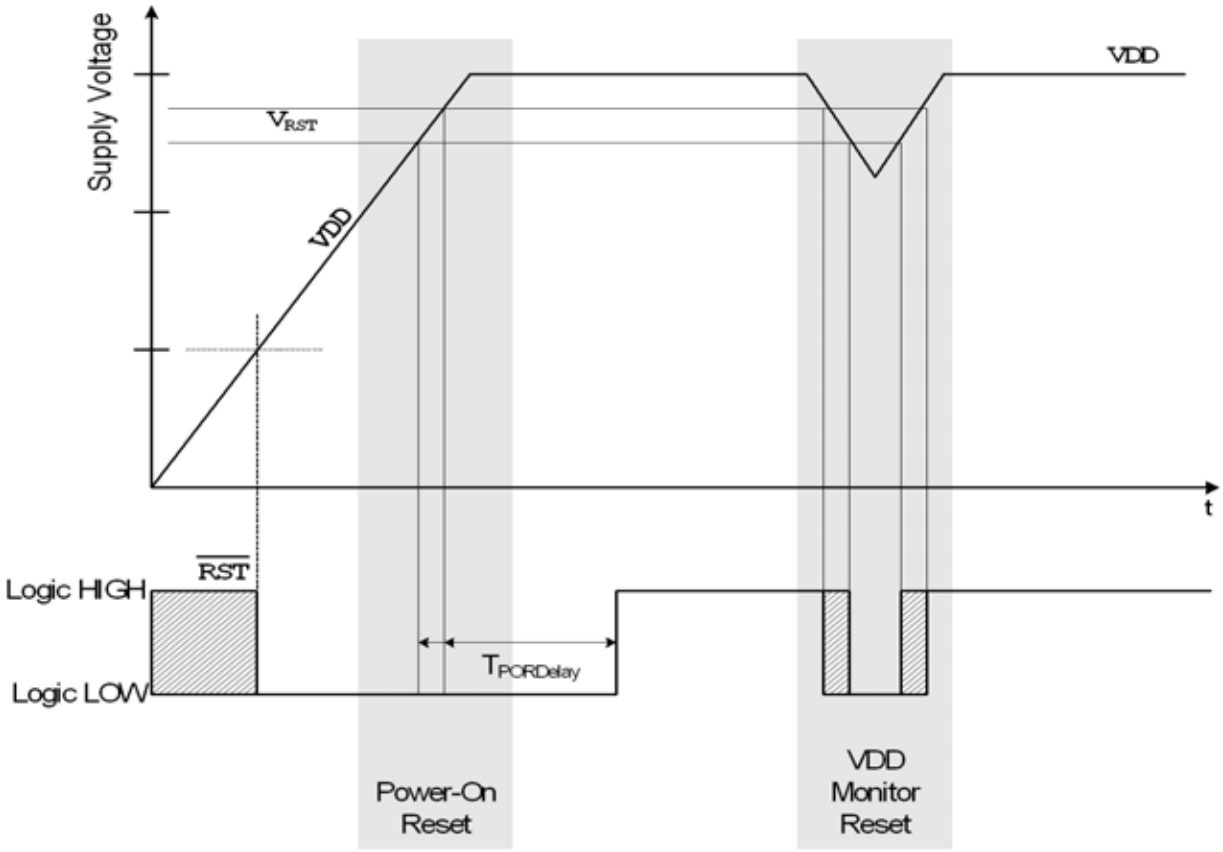

Figure 17.2. Power-On and V_{DD} Monitor Reset Timing

USB Register Definition 21.5. CLKREC: Clock Recovery Control

Bit	7	6	5	4	3	2	1	0
Name	CRE	CRSSEN	CRLOW					
Type	R/W	R/W	R/W	R/W				
Reset	0	0	0	0	1	1	1	1

USB Register Address = 0x0F

Bit	Name	Function
7	CRE	**Clock Recovery Enable Bit.** This bit enables/disables the USB clock recovery feature. 0: Clock recovery disabled. 1: Clock recovery enabled.
6	CRSSEN	**Clock Recovery Single Step.** This bit forces the oscillator calibration into single-step mode during clock recovery. 0: Normal calibration mode. 1: Single step mode.
5	CRLOW	**Low Speed Clock Recovery Mode.** This bit must be set to 1 if clock recovery is used when operating as a Low Speed USB device. 0: Full Speed Mode. 1: Low Speed Mode.
4:0	Reserved	Must Write = 01111b.

21.5. FIFO Management

1024 bytes of on-chip XRAM are used as FIFO space for USB0. This FIFO space is split between Endpoints0-3 as shown in Figure 21.3. FIFO space allocated for Endpoints1-3 is configurable as IN, OUT, or both (Split Mode: half IN, half OUT).

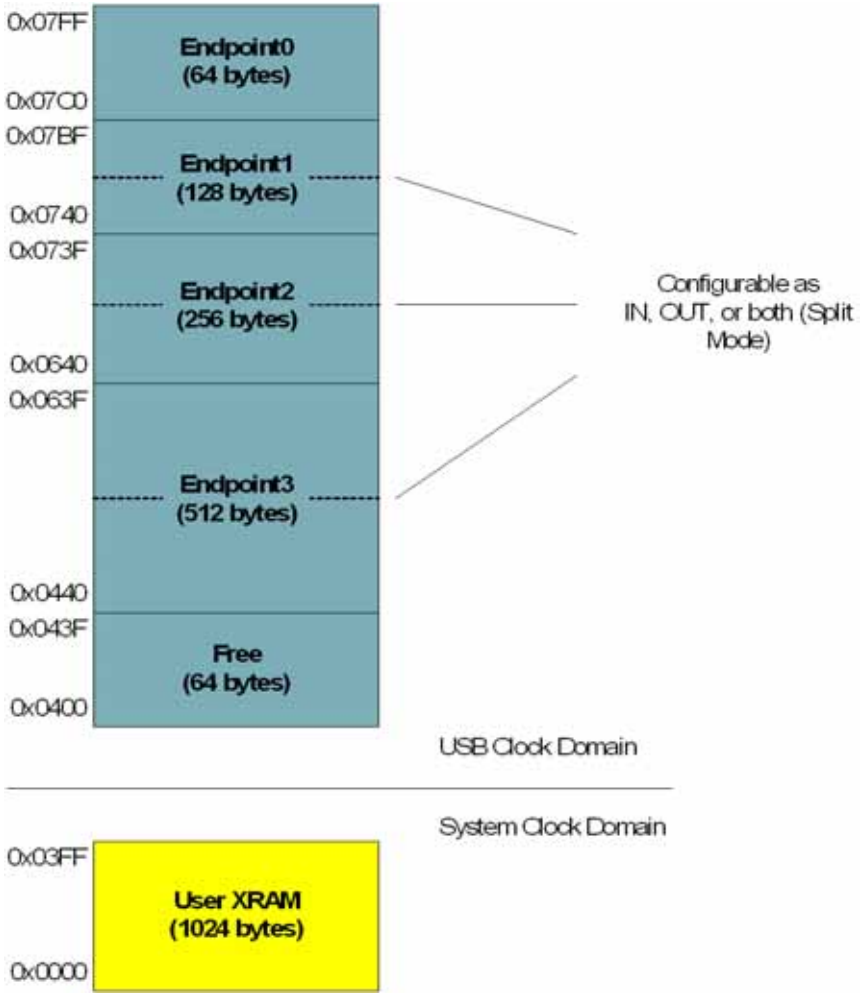

Figure 21.3. USB FIFO Allocation

21.5.1. FIFO Split Mode

The FIFO space for Endpoints1-3 can be split such that the upper half of the FIFO space is used by the IN endpoint, and the lower half is used by the OUT endpoint. For example: if the Endpoint3 FIFO is configured for Split Mode, the upper 256 bytes (0x0540 to 0x063F) are used by Endpoint3 IN and the lower 256 bytes (0x0440 to 0x053F) are used by Endpoint3 OUT.

If an endpoint FIFO is not configured for Split Mode, that endpoint IN/OUT pair's FIFOs are combined to form a single IN *or* OUT FIFO. In this case only one direction of the endpoint IN/OUT pair may be used at a time. The endpoint direction (IN/OUT) is determined by the DIRSEL bit in the corresponding endpoint's EINCSRH register (see SFR Definition 21.13).

USB Register Definition 21.13. CMINT: USB0 Common Interrupt

Bit	7	6	5	4	3	2	1	0
Name					SOF	RSTINT	RSUINT	SUSINT
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

USB Register Address = 0x06

Bit	Name	Function
7:4	Unused	Read = 0000b. Write = don't care.
3	SOF	**Start of Frame Interrupt Flag.** Set by hardware when a SOF token is received. This interrupt event is synthesized by hardware: an interrupt will be generated when hardware expects to receive a SOF event, even if the actual SOF signal is missed or corrupted. This bit is cleared when software reads the CMINT register. 0: SOF interrupt inactive. 1: SOF interrupt active.
2	RSTINT	**Reset Interrupt-Pending Flag.** Set by hardware when Reset signaling is detected on the bus. This bit is cleared when software reads the CMINT register. 0: Reset interrupt inactive. 1: Reset interrupt active.
1	RSUINT	**Resume Interrupt-Pending Flag.** Set by hardware when Resume signaling is detected on the bus while USB0 is in suspend mode. This bit is cleared when software reads the CMINT register. 0: Resume interrupt inactive. 1: Resume interrupt active.
0	SUSINT	**Suspend Interrupt-Pending Flag.** When Suspend detection is enabled (bit SUSEN in register POWER), this bit is set by hardware when Suspend signaling is detected on the bus. This bit is cleared when software reads the CMINT register. 0: Suspend interrupt inactive. 1: Suspend interrupt active.

22.5.3. Write Sequence (Slave)

During a write sequence, an SMBus master writes data to a slave device. The slave in this transfer will be a receiver during the address byte, and a receiver during all data bytes. When slave events are enabled (INH = 0), the interface enters Slave Receiver Mode when a START followed by a slave address and direction bit (WRITE in this case) is received. If hardware ACK generation is disabled, upon entering Slave Receiver Mode, an interrupt is generated and the ACKRQ bit is set. The software must respond to the received slave address with an ACK, or ignore the received slave address with a NACK. If hardware ACK generation is enabled, the hardware will apply the ACK for a slave address which matches the criteria set up by SMB0ADR and SMB0ADM. The interrupt will occur after the ACK cycle.

If the received slave address is ignored (by software or hardware), slave interrupts will be inhibited until the next START is detected. If the received slave address is acknowledged, zero or more data bytes are received.

If hardware ACK generation is disabled, the ACKRQ is set to 1 and an interrupt is generated after each received byte. Software must write the ACK bit at that time to ACK or NACK the received byte.

With hardware ACK generation enabled, the SMBus hardware will automatically generate the ACK/NACK, and then post the interrupt. **It is important to note that the appropriate ACK or NACK value should be set up by the software prior to receiving the byte when hardware ACK generation is enabled.**

The interface exits Slave Receiver Mode after receiving a STOP. The interface will switch to Slave Transmitter Mode if SMB0DAT is written while an active Slave Receiver. Figure 22.7 shows a typical slave write sequence. Two received data bytes are shown, though any number of bytes may be received. Notice that the ‘data byte transferred’ interrupts occur at different places in the sequence, depending on whether hardware ACK generation is enabled. The interrupt occurs **before** the ACK with hardware ACK generation disabled, and **after** the ACK when hardware ACK generation is enabled.

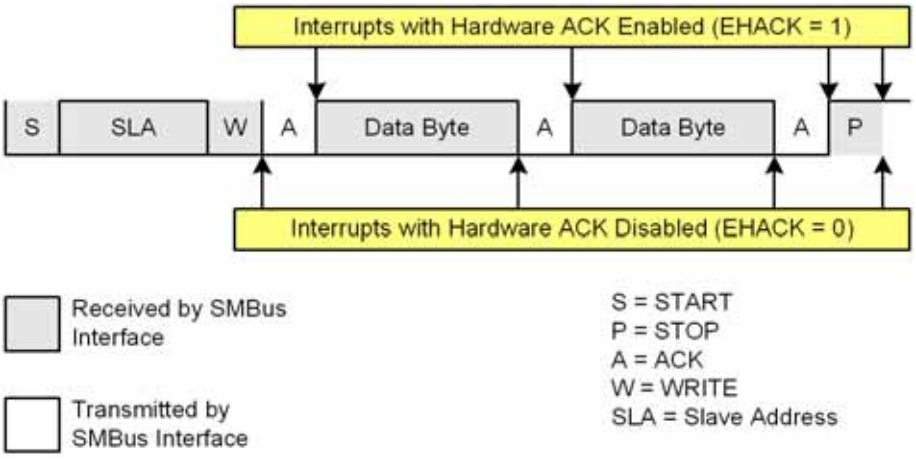

Figure 22.7. Typical Slave Write Sequence

SFR Definition 26.9. TMR2CN: Timer 2 Control

Bit	7	6	5	4	3	2	1	0
Name	TF2H	TF2L	TF2LEN	TF2CEN	T2SPLIT	TR2	T2CSS	T2XCLK
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xC8; SFR Page = 0; Bit-Addressable

Bit	Name	Function
7	TF2H	**Timer 2 High Byte Overflow Flag.** Set by hardware when the Timer 2 high byte overflows from 0xFF to 0x00. In 16 bit mode, this will occur when Timer 2 overflows from 0xFFFF to 0x0000. When the Timer 2 interrupt is enabled, setting this bit causes the CPU to vector to the Timer 2 interrupt service routine. This bit is not automatically cleared by hardware.
6	TF2L	**Timer 2 Low Byte Overflow Flag.** Set by hardware when the Timer 2 low byte overflows from 0xFF to 0x00. TF2L will be set when the low byte overflows regardless of the Timer 2 mode. This bit is not automatically cleared by hardware.
5	TF2LEN	**Timer 2 Low Byte Interrupt Enable.** When set to 1, this bit enables Timer 2 Low Byte interrupts. If Timer 2 interrupts are also enabled, an interrupt will be generated when the low byte of Timer 2 overflows.
4	TF2CEN	**Timer 2 Low-Frequency Oscillator Capture Enable.** When set to 1, this bit enables Timer 2 Low-Frequency Oscillator Capture Mode. If TF2CEN is set and Timer 2 interrupts are enabled, an interrupt will be generated on a falling edge of the low-frequency oscillator output, and the current 16-bit timer value in TMR2H:TMR2L will be copied to TMR2RLH:TMR2RLL.
3	T2SPLIT	**Timer 2 Split Mode Enable.** When this bit is set, Timer 2 operates as two 8-bit timers with auto-reload.
2	TR2	**Timer 2 Run Control.** Timer 2 is enabled by setting this bit to 1. In 8-bit mode, this bit enables/disables TMR2H only; TMR2L is always enabled in split mode.
1	T2CSS	**Timer 2 Capture Source Select.** This bit selects the source of a capture event when bit T2CE is set to 1. 0: Capture source is USB SOF event. 1: Capture source is falling edge of Low-Frequency Oscillator.
0	T2XCLK	**Timer 2 External Clock Select.** This bit selects the external clock source for Timer 2. However, the Timer 2 Clock Select bits (T2MH and T2ML in register CKCON) may still be used to select between the external clock and the system clock for either timer. 0: Timer 2 clock is the system clock divided by 12. 1: Timer 2 clock is the external clock divided by 8 (synchronized with SYSCLK).

SFR Definition 26.15. TMR3RLL: Timer 3 Reload Register Low Byte

Bit	7	6	5	4	3	2	1	0
Name	TMR3RLL[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x92; SFR Page = 0

Bit	Name	Function
7:0	TMR3RLL[7:0]	**Timer 3 Reload Register Low Byte.** TMR3RLL holds the low byte of the reload value for Timer 3.

SFR Definition 26.16. TMR3RLH: Timer 3 Reload Register High Byte

Bit	7	6	5	4	3	2	1	0
Name	TMR3RLH[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x93; SFR Page = 0

Bit	Name	Function
7:0	TMR3RLH[7:0]	**Timer 3 Reload Register High Byte.** TMR3RLH holds the high byte of the reload value for Timer 3.

SFR Definition 26.17. TMR3L: Timer 3 Low Byte

Bit	7	6	5	4	3	2	1	0
Name	TMR3L[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x94; SFR Page = 0

Bit	Name	Function
7:0	TMR3L[7:0]	**Timer 3 Low Byte.** In 16-bit mode, the TMR3L register contains the low byte of the 16-bit Timer 3. In 8-bit mode, TMR3L contains the 8-bit low byte timer value.

27.3.5. 8-bit Pulse Width Modulator Mode

The duty cycle of the PWM output signal in 8-bit PWM mode is varied using the module's PCA0CPLn capture/compare register. When the value in the low byte of the PCA counter/timer (PCA0L) is equal to the value in PCA0CPLn, the output on the CEXn pin will be set. When the count value in PCA0L overflows, the CEXn output will be reset (see Figure 27.8). Also, when the counter/timer low byte (PCA0L) overflows from 0xFF to 0x00, PCA0CPLn is reloaded automatically with the value stored in the module's capture/compare high byte (PCA0CPHn) without software intervention. Setting the ECOMn and PWMn bits in the PCA0CPMn register enables 8-Bit Pulse Width Modulator mode. If the MATn bit is set to 1, the CCFn flag for the module will be set each time an 8-bit comparator match (rising edge) occurs. The duty cycle for 8-Bit PWM Mode is given in Equation 27.2.

Important Note About Capture/Compare Registers: When writing a 16-bit value to the PCA0 Capture/Compare registers, the low byte should always be written first. Writing to PCA0CPLn clears the ECOMn bit to 0; writing to PCA0CPHn sets ECOMn to 1.

$$\text{Duty Cycle} = \frac{(256 - \text{PCA0CPHn})}{256}$$

Equation 27.2. 8-Bit PWM Duty Cycle

Using Equation 27.2, the largest duty cycle is 100% (PCA0CPHn = 0), and the smallest duty cycle is 0.39% (PCA0CPHn = 0xFF). A 0% duty cycle may be generated by clearing the ECOMn bit to 0.

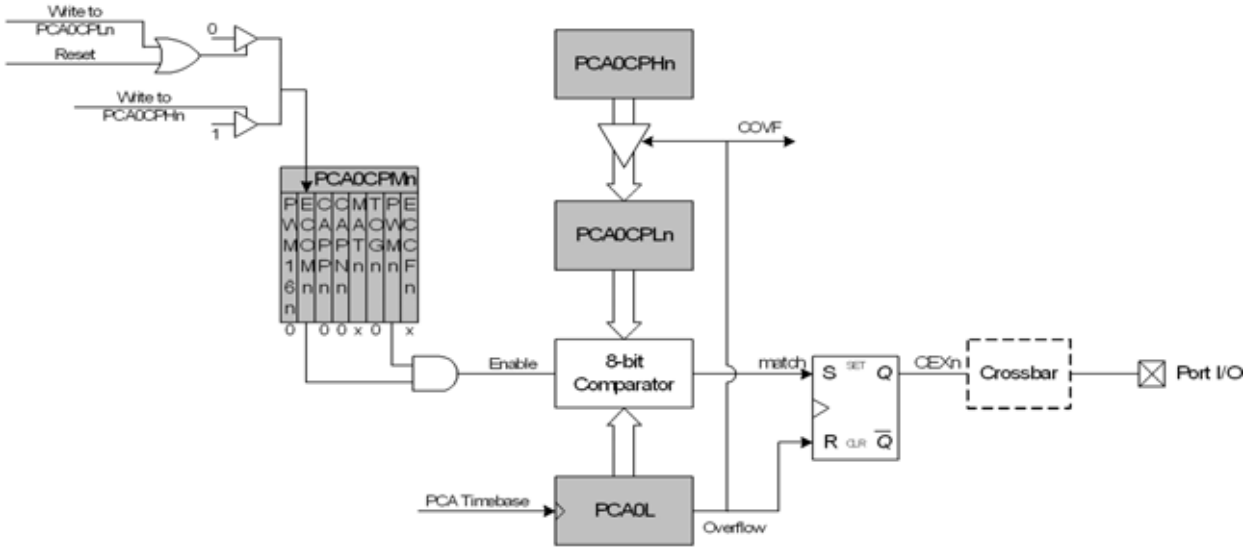

Figure 27.8. PCA 8-Bit PWM Mode Diagram

28. C2 Interface

C8051F380/1/2/3/4/5/6/7/C devices include an on-chip Silicon Labs 2-Wire (C2) debug interface to allow Flash programming and in-system debugging with the production part installed in the end application. The C2 interface uses a clock signal (C2CK) and a bi-directional C2 data signal (C2D) to transfer information between the device and a host system. See the C2 Interface Specification for details on the C2 protocol.

28.1. C2 Interface Registers

The following describes the C2 registers necessary to perform Flash programming through the C2 interface. All C2 registers are accessed through the C2 interface as described in the C2 Interface Specification.

C2 Register Definition 28.1. C2ADD: C2 Address

Bit	7	6	5	4	3	2	1	0
Name	C2ADD[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

Bit	Name	Function	
7:0	C2ADD[7:0]	**C2 Address.** The C2ADD register is accessed via the C2 interface to select the target Data register for C2 Data Read and Data Write commands.	
		Address	**Description**
		0x00	Selects the Device ID register for Data Read instructions
		0x01	Selects the Revision ID register for Data Read instructions
		0x02	Selects the C2 Flash Programming Control register for Data Read/Write instructions
		0xAD	Selects the C2 Flash Programming Data register for Data Read/Write instructions