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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	48 MIPS
Connectivity	EBI/EMI, I²C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	40
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.25V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f386-gqr

List of Tables

Table 1.1. Product Selection Guide

Ordering Part Number	MIPS (Peak)	Flash Memory (Bytes)	RAM	Calibrated Internal Oscillator	Low Frequency Oscillator	USB with 1k Endpoint RAM	Supply Voltage Regulator	SMBus/I2C	Enhanced SPI	UARTs	Timers (16-bit)	Programmable Counter Array	Digital Port I/O	External Memory Interface (EMIF)	10-bit 500ksps ADC	Temperature Sensor	Voltage Reference	Analog Comparators	Package
C8051F380-GQ	48	64k	4352	✓	✓	✓	✓	2	✓	2	6	✓	40	✓	✓	✓	✓	2	TQFP48
C8051F381-GQ	48	64k	4352	✓	✓	✓	✓	2	✓	2	6	✓	25	—	✓	✓	✓	2	LQFP32
C8051F381-GM	48	64k	4352	✓	✓	✓	✓	2	✓	2	6	✓	25	—	✓	✓	✓	2	QFN32
C8051F382-GQ	48	32k	2304	✓	✓	✓	✓	2	✓	2	6	✓	40	✓	✓	✓	✓	2	TQFP48
C8051F383-GQ	48	32k	2304	✓	✓	✓	✓	2	✓	2	6	✓	25	—	✓	✓	✓	2	LQFP32
C8051F383-GM	48	32k	2304	✓	✓	✓	✓	2	✓	2	6	✓	25	—	✓	✓	✓	2	QFN32
C8051F384-GQ	48	64k	4352	✓	✓	✓	✓	2	✓	2	6	✓	40	✓	—	—	—	2	TQFP48
C8051F385-GQ	48	64k	4352	✓	✓	✓	✓	2	✓	2	6	✓	25	—	—	—	—	2	LQFP32
C8051F385-GM	48	64k	4352	✓	✓	✓	✓	2	✓	2	6	✓	25	—	—	—	—	2	QFN32
C8051F386-GQ	48	32k	2304	✓	✓	✓	✓	2	✓	2	6	✓	40	✓	—	—	—	2	TQFP48
C8051F387-GQ	48	32k	2304	✓	✓	✓	✓	2	✓	2	6	✓	25	—	—	—	—	2	LQFP32
C8051F387-GM	48	32k	2304	✓	✓	✓	✓	2	✓	2	6	✓	25	—	—	—	—	2	QFN32
C8051F38C-GQ	48	16k	2304	✓	✓	✓	✓	2	✓	2	6	✓	25	—	✓	✓	✓	2	LQFP32
C8051F38C-GM	48	16k	2304	✓	✓	✓	✓	2	✓	2	6	✓	25	—	✓	✓	✓	2	QFN32

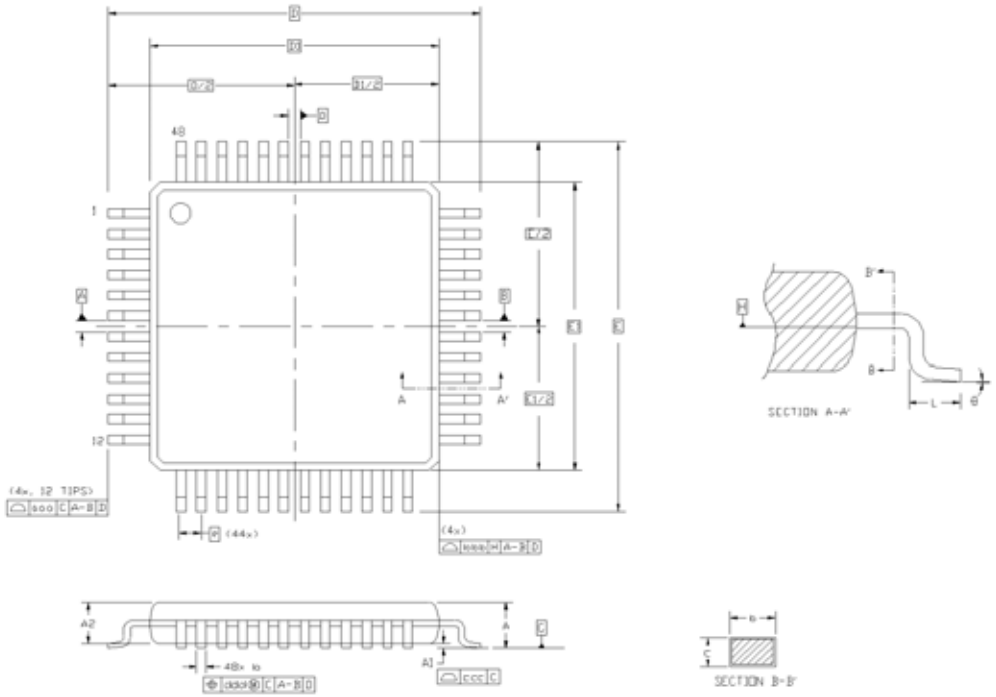

Figure 3.2. TQFP-48 Package Diagram

Table 3.2. TQFP-48 Package Dimensions

Dimension	Min	Nom	Max	Dimension	Min	Nom	Max
A	—	—	1.20	E		9.00 BSC	
A1	0.05	—	0.15	E1		7.00 BSC	
A2	0.95	1.00	1.05	L	0.45	0.60	0.75
b	0.17	0.22	0.27	aaa		0.20	
c	0.09	—	0.20	bbb		0.20	
D		9.00 BSC		ccc		0.08	
D1		7.00 BSC		ddd		0.08	
e		0.50 BSC		q	0°	3.5°	7°

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MS-026, variation ABC.
4. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

4.2. USB

Figure 4.5 shows a typical connection diagram for the USB pins of the C8051F38x devices including a 100 Ω current-limiting resistor on the VBUS sense pin and ESD protection diodes on the USB pins. This current-limiting resistor is recommended for systems that may experience electrostatic discharge (ESD), latch-up, and have a greater opportunity to share signals with systems that do not have the same ground potential. This is not a required component for most applications.

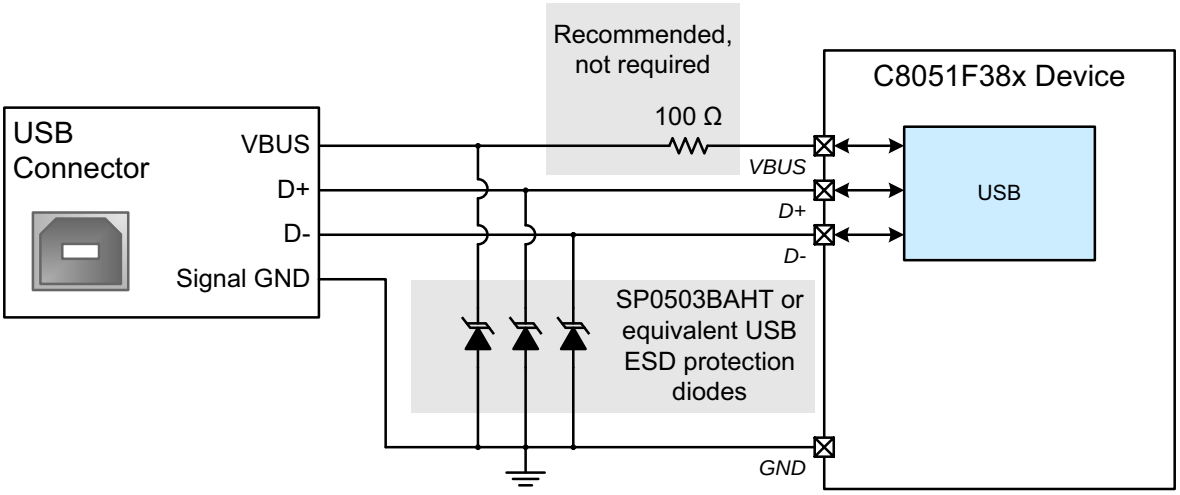

Figure 4.5. Connection Diagram for USB Pins

4.3. Voltage Reference (VREF)

Figure 4.6 shows a typical connection diagram for the voltage reference (VREF) pin of the C8051F38x devices when using the internal voltage reference. When using an external voltage reference, consult the appropriate device's data sheet for connection recommendations.

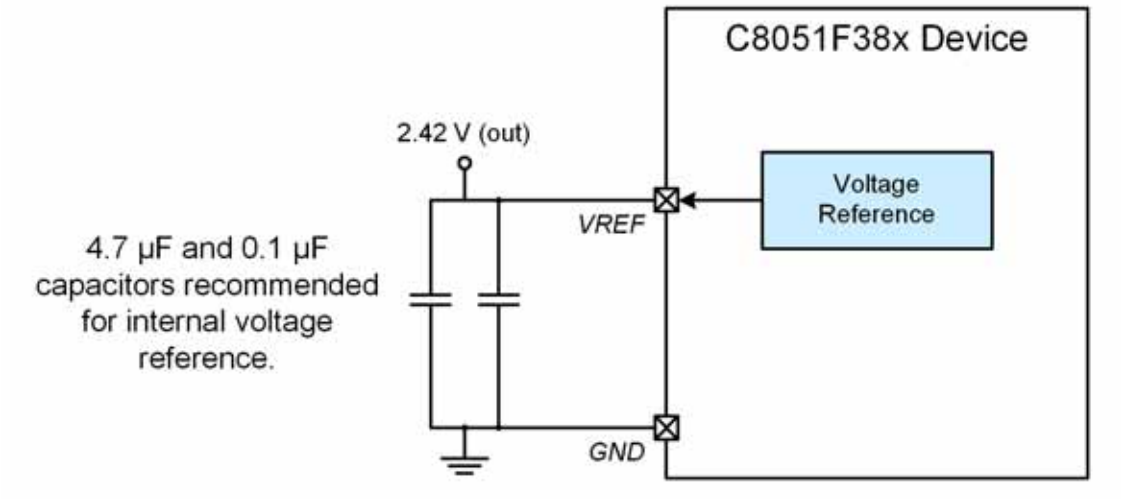

Figure 4.6. Connection Diagram for Internal Voltage Reference

6.4. Programmable Window Detector

The ADC Programmable Window Detector continuously compares the ADC0 output registers to user-programmed limits, and notifies the system when a desired condition is detected. This is especially effective in an interrupt-driven system, saving code space and CPU bandwidth while delivering faster system response times. The window detector interrupt flag (AD0WINT in register ADC0CN) can also be used in polled mode. The ADC0 Greater-Than (ADC0GTH, ADC0GTL) and Less-Than (ADC0LTH, ADC0LTL) registers hold the comparison values. The window detector flag can be programmed to indicate when measured data is inside or outside of the user-programmed limits, depending on the contents of the ADC0 Less-Than and ADC0 Greater-Than registers.

SFR Definition 6.5. ADC0GTH: ADC0 Greater-Than Data High Byte

Bit	7	6	5	4	3	2	1	0
Name	ADC0GTH[7:0]							
Type	R/W							
Reset	1	1	1	1	1	1	1	1

SFR Address = 0xC4; SFR Page = All Pages

Bit	Name	Function
7:0	ADC0GTH[7:0]	**ADC0 Greater-Than Data Word High-Order Bits.**

SFR Definition 6.6. ADC0GTL: ADC0 Greater-Than Data Low Byte

Bit	7	6	5	4	3	2	1	0
Name	ADC0GTL[7:0]							
Type	R/W							
Reset	1	1	1	1	1	1	1	1

SFR Address = 0xC3; SFR Page = All Pages

Bit	Name	Function
7:0	ADC0GTL[7:0]	**ADC0 Greater-Than Data Word Low-Order Bits.**

SFR Definition 6.9. AMX0P: AMUX0 Positive Channel Select

Bit	7	6	5	4	3	2	1	0
Name			AMX0P[5:0]					
Type	R	R	R/W					
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xBB; SFR Page = All Pages

Bit	Name	Function					
7:6	Unused	Read = 00b; Write = don't care.					
5:0	AMX0P[5:0]	**AMUX0 Positive Input Selection.**					
		AMX0P	32-pin Packages	48-pin Packages	AMX0P	32-pin Packages	48-pin Packages
		000000:	P1.0	P2.0	010010:	P0.1	P0.4
		000001:	P1.1	P2.1	010011:	P0.4	P1.1
		000010:	P1.2	P2.2	010100:	P0.5	P1.2
		000011:	P1.3	P2.3	010101:	Reserved	P1.0
		000100:	P1.4	P2.5	010110:	Reserved	P1.3
		000101:	P1.5	P2.6	010111:	Reserved	P1.6
		000110:	P1.6	P3.0	011000:	Reserved	P1.7
		000111:	P1.7	P3.1	011001:	Reserved	P2.4
		001000:	P2.0	P3.4	011010:	Reserved	P2.7
		001001:	P2.1	P3.5	011011:	Reserved	P3.2
		001010:	P2.2	P3.7	011100:	Reserved	P3.3
		001011:	P2.3	P4.0	011101:	Reserved	P3.6
		001100:	P2.4	P4.3	011110:	Temp Sensor	Temp Sensor
		001101:	P2.5	P4.4	011111:	V_{DD}	V_{DD}
		001110:	P2.6	P4.5	100000:	Reserved	P4.1
		001111:	P2.7	P4.6	100001:	Reserved	P4.2
		010000:	P3.0	Reserved	100010:	Reserved	P4.7
		010001:	P0.0	P0.3	100011 - 111111:	Reserved	Reserved

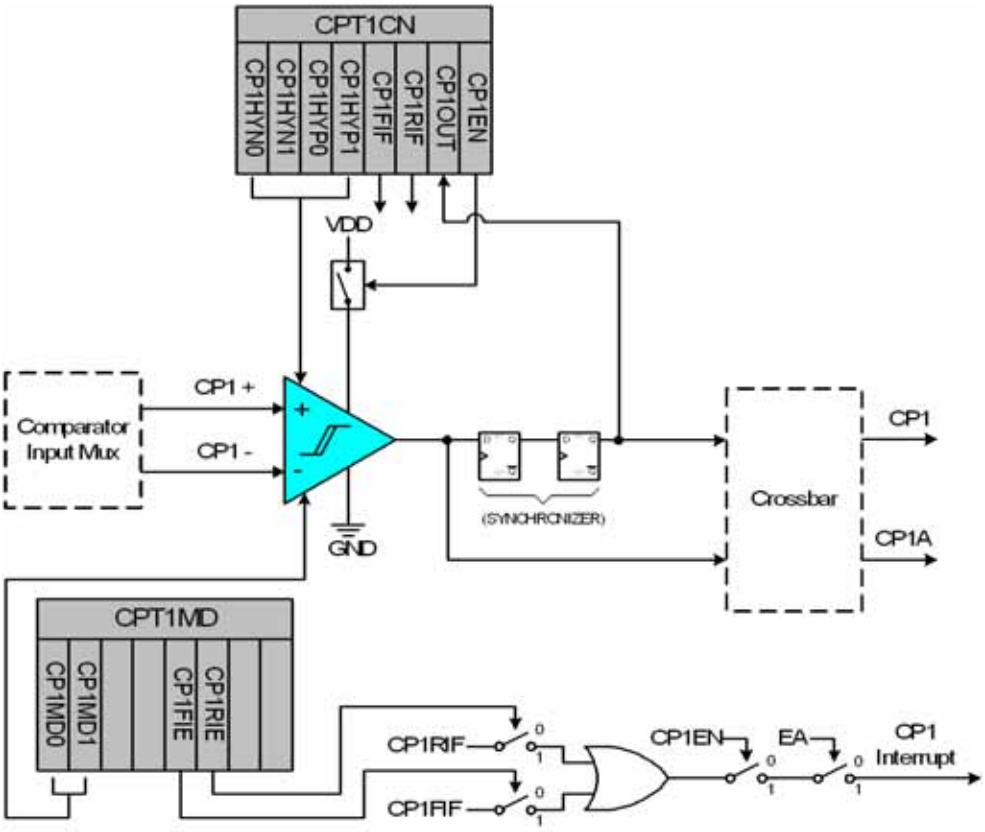

Figure 8.2. Comparator1 Functional Block Diagram

The Comparator output can be polled in software, used as an interrupt source, and/or routed to a Port pin. When routed to a Port pin, the Comparator output is available asynchronous or synchronous to the system clock; the asynchronous output is available even in STOP mode (with no system clock active). When disabled, the Comparator output (if assigned to a Port I/O pin via the Crossbar) defaults to the logic low state, and the power supply to the comparator is turned off. See Section “20.1. Priority Crossbar Decoder” on page 154 for details on configuring Comparator outputs via the digital Crossbar. Comparator inputs can be externally driven from –0.25 V to (V_{DD}) + 0.25 V without damage or upset. The complete Comparator electrical specifications are given in Section “5. Electrical Characteristics” on page 37.

The Comparator response time may be configured in software via the CPTnMD registers (see SFR Definition 8.2 and SFR Definition 8.4). Selecting a longer response time reduces the Comparator supply current.

12. Prefetch Engine

The C8051F380/1/2/3/4/5/6/7/C family of devices incorporate a 2-byte prefetch engine. Because the access time of the Flash memory is 40 ns, and the minimum instruction time is roughly 20 ns, the prefetch engine is necessary for full-speed code execution. Instructions are read from Flash memory two bytes at a time by the prefetch engine and given to the CIP-51 processor core to execute. When running linear code (code without any jumps or branches), the prefetch engine allows instructions to be executed at full speed. When a code branch occurs, the processor may be stalled for up to two clock cycles while the next set of code bytes is retrieved from Flash memory. It is recommended that the prefetch be used for optimal code execution timing.

Note: The prefetch engine can be disabled when the device is in suspend mode to save power.

SFR Definition 12.1. PFE0CN: Prefetch Engine Control

Bit	7	6	5	4	3	2	1	0
Name			PFEN					FLBWE
Type	R	R	R/W	R	R	R	R	R/W
Reset	0	0	1	0	0	0	0	0

SFR Address = 0xAF; SFR Page = All Pages

Bit	Name	Function
7:6	Unused	Read = 00b, Write = don't care.
5	PFEN	**Prefetch Enable.** This bit enables the prefetch engine. 0: Prefetch engine is disabled. 1: Prefetch engine is enabled.
4:1	Unused	Read = 0000b. Write = don't care.
0	FLBWE	**Flash Block Write Enable.** This bit allows block writes to Flash memory from software. 0: Each byte of a software Flash write is written individually. 1: Flash bytes are written in groups of two.

14.7.2.2. 8-bit MOVX without Bank Select: EMI0CF[4:2] = 001 or 011

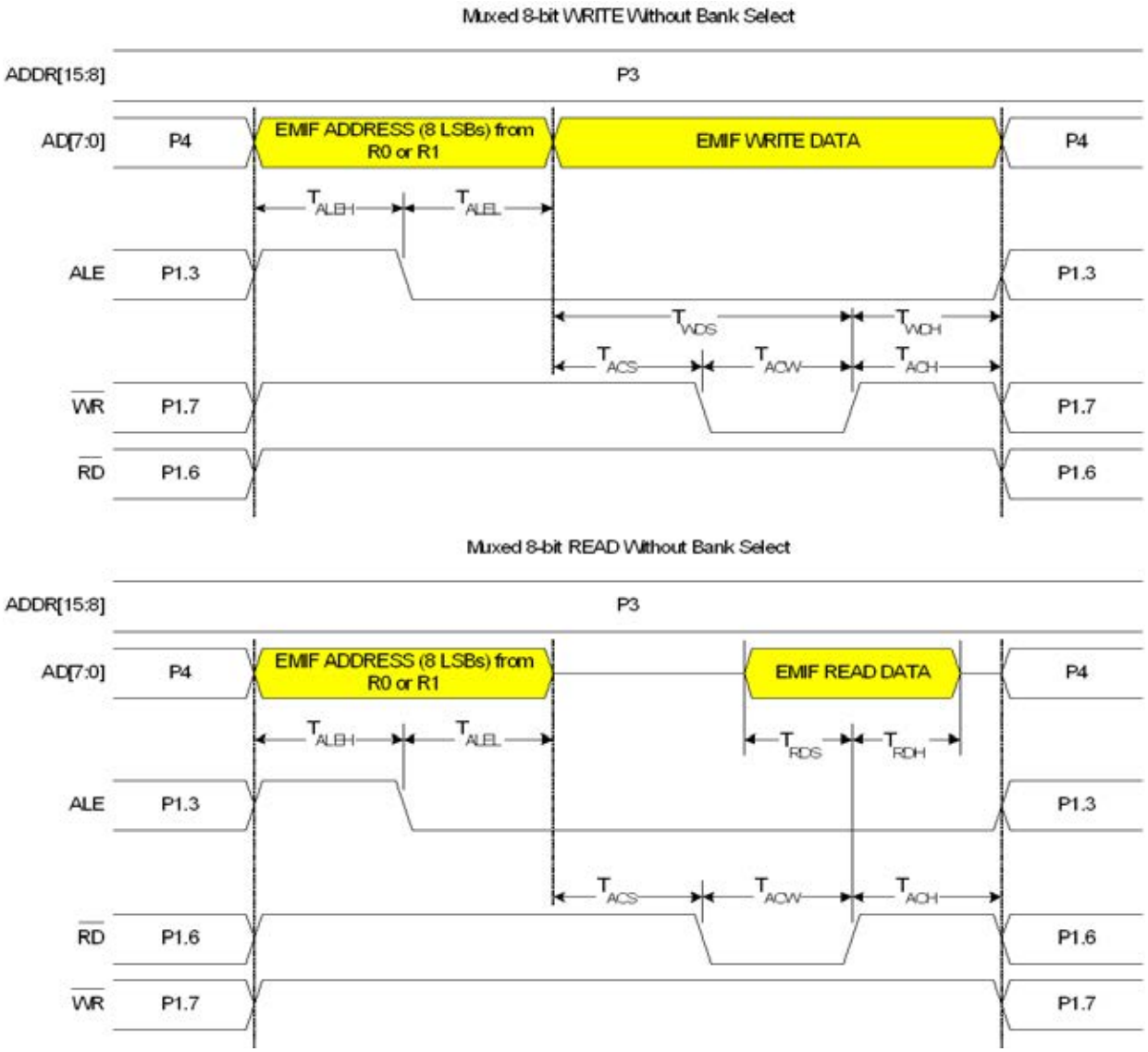

Figure 14.9. Multiplexed 8-bit MOVX without Bank Select Timing

SFR Definition 16.7. IT01CF: $\overline{\text{INT0}}$/$\overline{\text{INT1}}$ Configuration

Bit	7	6	5	4	3	2	1	0
Name	IN1PL	IN1SL[2:0]			IN0PL	IN0SL[2:0]		
Type	R/W	R/W			R/W	R/W		
Reset	0	0	0	0	0	0	0	1

SFR Address = 0xE4; SFR Page = 0

Bit	Name	Function
7	IN1PL	**$\overline{\text{INT1}}$ Polarity.** 0: $\overline{\text{INT1}}$ input is active low. 1: $\overline{\text{INT1}}$ input is active high.
6:4	IN1SL[2:0]	**$\overline{\text{INT1}}$ Port Pin Selection Bits.** These bits select which Port pin is assigned to $\overline{\text{INT1}}$. Note that this pin assignment is independent of the Crossbar; $\overline{\text{INT1}}$ will monitor the assigned Port pin without disturbing the peripheral that has been assigned the Port pin via the Crossbar. The Crossbar will not assign the Port pin to a peripheral if it is configured to skip the selected pin. 000: Select P0.0 001: Select P0.1 010: Select P0.2 011: Select P0.3 100: Select P0.4 101: Select P0.5 110: Select P0.6 111: Select P0.7
3	IN0PL	**$\overline{\text{INT0}}$ Polarity.** 0: $\overline{\text{INT0}}$ input is active low. 1: $\overline{\text{INT0}}$ input is active high.
2:0	IN0SL[2:0]	**$\overline{\text{INT0}}$ Port Pin Selection Bits.** These bits select which Port pin is assigned to $\overline{\text{INT0}}$. Note that this pin assignment is independent of the Crossbar; $\overline{\text{INT0}}$ will monitor the assigned Port pin without disturbing the peripheral that has been assigned the Port pin via the Crossbar. The Crossbar will not assign the Port pin to a peripheral if it is configured to skip the selected pin. 000: Select P0.0 001: Select P0.1 010: Select P0.2 011: Select P0.3 100: Select P0.4 101: Select P0.5 110: Select P0.6 111: Select P0.7

SFR Definition 21.2. USB0ADR: USB0 Indirect Address

Bit	7	6	5	4	3	2	1	0
Name	BUSY	AUTORD	USBADDR[5:0]					
Type	R/W	R/W	R/W					
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x96; SFR Page = All Pages

Bit	Name	Description	Write	Read
7	BUSY	**USB0 Register Read Busy Flag.** This bit is used during indirect USB0 register accesses.	0: No effect. 1: A USB0 indirect register read is initiated at the address specified by the USBADDR bits.	0: USB0DAT register data is valid. 1: USB0 is busy accessing an indirect register; USB0DAT register data is invalid.
6	AUTORD	**USB0 Register Auto-read Flag.** This bit is used for block FIFO reads. 0: BUSY must be written manually for each USB0 indirect register read. 1: The next indirect register read will automatically be initiated when software reads USB0DAT (USBADDR bits will not be changed).		
5:0	USBADDR[5:0]	**USB0 Indirect Register Address Bits.** These bits hold a 6-bit address used to indirectly access the USB0 core registers. Table 21.2 lists the USB0 core registers and their indirect addresses. Reads and writes to USB0DAT will target the register indicated by the USBADDR bits.		

USB Register Definition 21.5. CLKREC: Clock Recovery Control

Bit	7	6	5	4	3	2	1	0
Name	CRE	CRSSEN	CRLOW					
Type	R/W	R/W	R/W	R/W				
Reset	0	0	0	0	1	1	1	1

USB Register Address = 0x0F

Bit	Name	Function
7	CRE	**Clock Recovery Enable Bit.** This bit enables/disables the USB clock recovery feature. 0: Clock recovery disabled. 1: Clock recovery enabled.
6	CRSSEN	**Clock Recovery Single Step.** This bit forces the oscillator calibration into single-step mode during clock recovery. 0: Normal calibration mode. 1: Single step mode.
5	CRLOW	**Low Speed Clock Recovery Mode.** This bit must be set to 1 if clock recovery is used when operating as a Low Speed USB device. 0: Full Speed Mode. 1: Low Speed Mode.
4:0	Reserved	Must Write = 01111b.

21.5. FIFO Management

1024 bytes of on-chip XRAM are used as FIFO space for USB0. This FIFO space is split between Endpoints0-3 as shown in Figure 21.3. FIFO space allocated for Endpoints1-3 is configurable as IN, OUT, or both (Split Mode: half IN, half OUT).

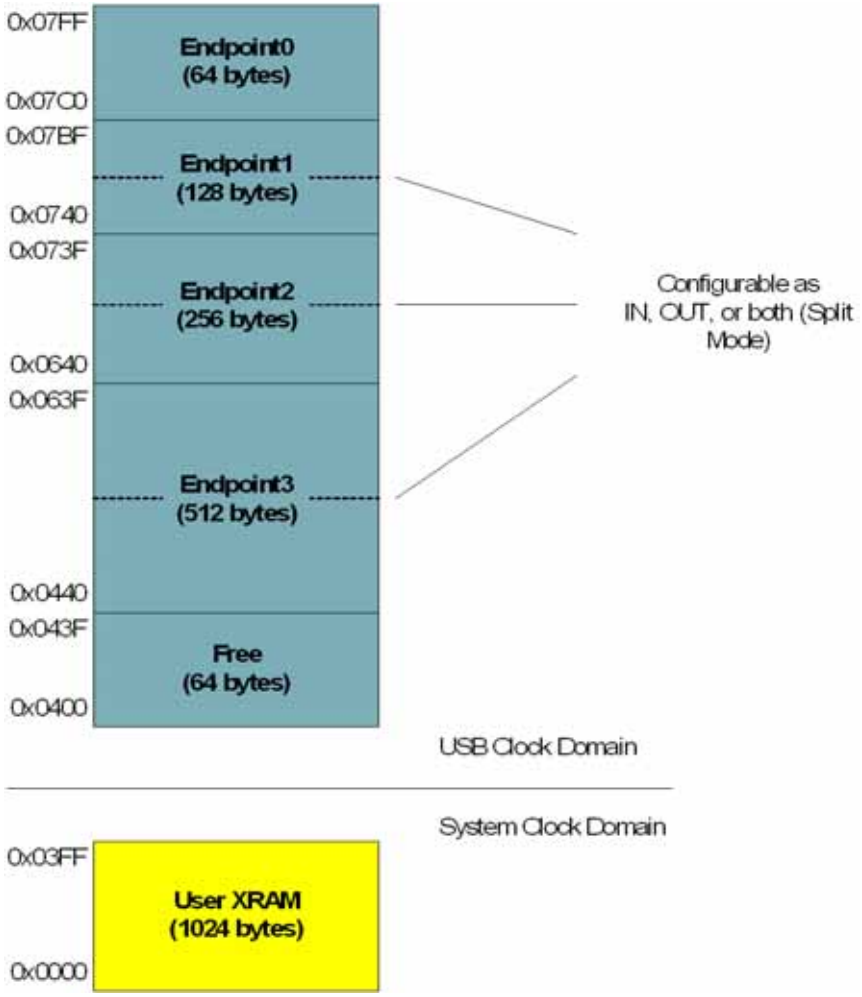

Figure 21.3. USB FIFO Allocation

21.5.1. FIFO Split Mode

The FIFO space for Endpoints1-3 can be split such that the upper half of the FIFO space is used by the IN endpoint, and the lower half is used by the OUT endpoint. For example: if the Endpoint3 FIFO is configured for Split Mode, the upper 256 bytes (0x0540 to 0x063F) are used by Endpoint3 IN and the lower 256 bytes (0x0440 to 0x053F) are used by Endpoint3 OUT.

If an endpoint FIFO is not configured for Split Mode, that endpoint IN/OUT pair's FIFOs are combined to form a single IN *or* OUT FIFO. In this case only one direction of the endpoint IN/OUT pair may be used at a time. The endpoint direction (IN/OUT) is determined by the DIRSEL bit in the corresponding endpoint's EINCSRH register (see SFR Definition 21.13).

25. Enhanced Serial Peripheral Interface (SPI0)

The Enhanced Serial Peripheral Interface (SPI0) provides access to a flexible, full-duplex synchronous serial bus. SPI0 can operate as a master or slave device in both 3-wire or 4-wire modes, and supports multiple masters and slaves on a single SPI bus. The slave-select (NSS) signal can be configured as an input to select SPI0 in slave mode, or to disable Master Mode operation in a multi-master environment, avoiding contention on the SPI bus when more than one master attempts simultaneous data transfers. NSS can also be configured as a chip-select output in master mode, or disabled for 3-wire operation. Additional general purpose port I/O pins can be used to select multiple slave devices in master mode.

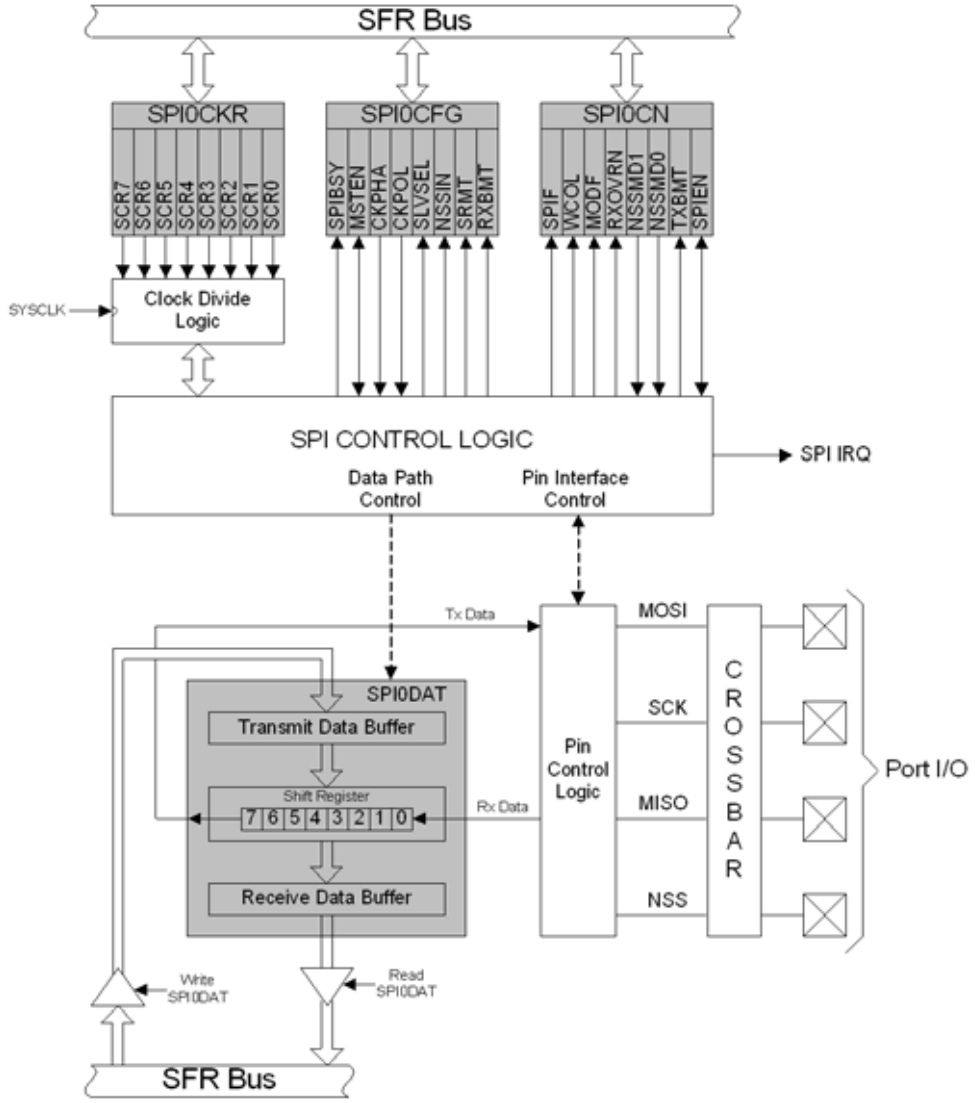

Figure 25.1. SPI Block Diagram

SFR Definition 26.1. CKCON: Clock Control

Bit	7	6	5	4	3	2	1	0
Name	T3MH	T3ML	T2MH	T2ML	T1M	T0M	SCA[1:0]	
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x8E; SFR Page = All Pages

Bit	Name	Function
7	T3MH	**Timer 3 High Byte Clock Select.** Selects the clock supplied to the Timer 3 high byte (split 8-bit timer mode only). 0: Timer 3 high byte uses the clock defined by the T3XCLK bit in TMR3CN. 1: Timer 3 high byte uses the system clock.
6	T3ML	**Timer 3 Low Byte Clock Select.** Selects the clock supplied to Timer 3. Selects the clock supplied to the lower 8-bit timer in split 8-bit timer mode. 0: Timer 3 low byte uses the clock defined by the T3XCLK bit in TMR3CN. 1: Timer 3 low byte uses the system clock.
5	T2MH	**Timer 2 High Byte Clock Select.** Selects the clock supplied to the Timer 2 high byte (split 8-bit timer mode only). 0: Timer 2 high byte uses the clock defined by the T2XCLK bit in TMR2CN. 1: Timer 2 high byte uses the system clock.
4	T2ML	**Timer 2 Low Byte Clock Select.** Selects the clock supplied to Timer 2. If Timer 2 is configured in split 8-bit timer mode, this bit selects the clock supplied to the lower 8-bit timer. 0: Timer 2 low byte uses the clock defined by the T2XCLK bit in TMR2CN. 1: Timer 2 low byte uses the system clock.
3	T1	**Timer 1 Clock Select.** Selects the clock source supplied to Timer 1. Ignored when C/T1 is set to 1. 0: Timer 1 uses the clock defined by the prescale bits SCA[1:0]. 1: Timer 1 uses the system clock.
2	T0	**Timer 0 Clock Select.** Selects the clock source supplied to Timer 0. Ignored when C/T0 is set to 1. 0: Counter/Timer 0 uses the clock defined by the prescale bits SCA[1:0]. 1: Counter/Timer 0 uses the system clock.
1:0	SCA[1:0]	**Timer 0/1 Prescale Bits.** These bits control the Timer 0/1 Clock Prescaler: 00: System clock divided by 12 01: System clock divided by 4 10: System clock divided by 48 11: External clock divided by 8 (synchronized with the system clock)

26.3.2. 8-bit Timers with Auto-Reload

When T3SPLIT is 1 and T3CE = 0, Timer 3 operates as two 8-bit timers (TMR3H and TMR3L). Both 8-bit timers operate in auto-reload mode as shown in Figure 26.9. TMR3RLL holds the reload value for TMR3L; TMR3RLH holds the reload value for TMR3H. The TR3 bit in TMR3CN handles the run control for TMR3H. TMR3L is always running when configured for 8-bit Mode.

Each 8-bit timer may be configured to use SYSCLK, SYSCLK divided by 12, or the external oscillator clock source divided by 8. The Timer 3 Clock Select bits (T3MH and T3ML in CKCON) select either SYSCLK or the clock defined by the Timer 3 External Clock Select bit (T3XCLK in TMR3CN), as follows:

T3MH	T3XCLK	TMR3H Clock Source
0	0	SYSCLK / 12
0	1	External Clock / 8
1	X	SYSCLK

T3ML	T3XCLK	TMR3L Clock Source
0	0	SYSCLK / 12
0	1	External Clock / 8
1	X	SYSCLK

The TF3H bit is set when TMR3H overflows from 0xFF to 0x00; the TF3L bit is set when TMR3L overflows from 0xFF to 0x00. When Timer 3 interrupts are enabled, an interrupt is generated each time TMR3H overflows. If Timer 3 interrupts are enabled and TF3LEN (TMR3CN.5) is set, an interrupt is generated each time either TMR3L or TMR3H overflows. When TF3LEN is enabled, software must check the TF3H and TF3L flags to determine the source of the Timer 3 interrupt. The TF3H and TF3L interrupt flags are not cleared by hardware and must be manually cleared by software.

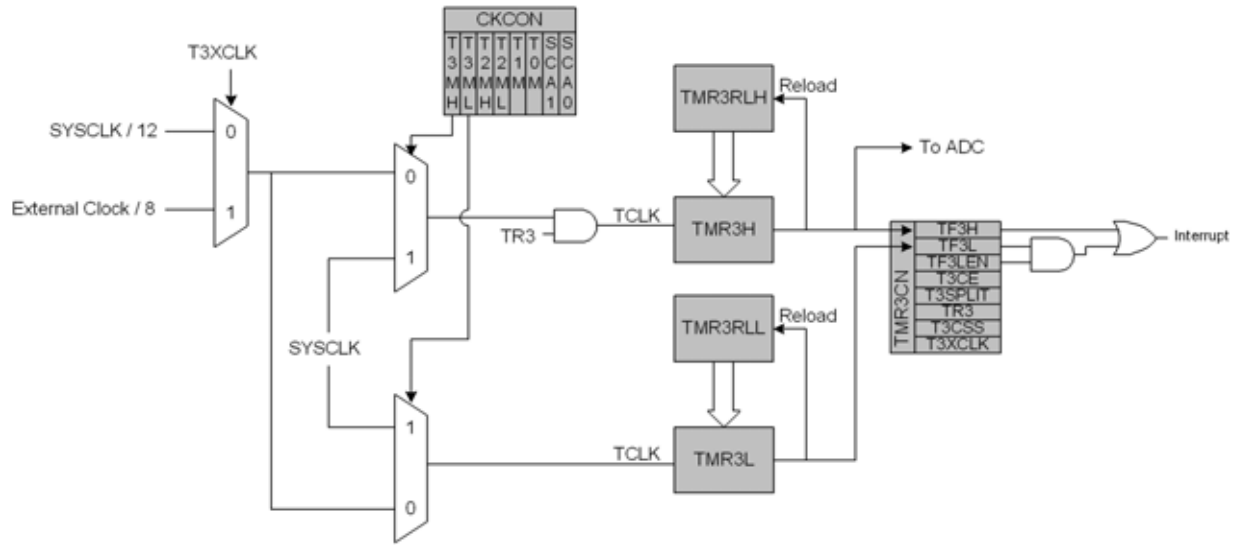

Figure 26.9. Timer 3 8-Bit Mode Block Diagram

26.3.3. Timer 3 Capture Modes: USB Start-of-Frame or LFO Falling Edge

When T3CE = 1, Timer 3 will operate in one of two special capture modes. The capture event can be selected between a USB Start-of-Frame (SOF) capture, and a Low-Frequency Oscillator (LFO) Falling Edge capture, using the T3CSS bit. The USB SOF capture mode can be used to calibrate the system clock or external oscillator against the known USB host SOF clock. The LFO falling-edge capture mode can be used to calibrate the internal Low-Frequency Oscillator against the internal High-Frequency Oscillator or an external clock source. When T3SPLIT = 0, Timer 3 counts up and overflows from 0xFFFF to 0x0000. Each time a capture event is received, the contents of the Timer 3 registers (TMR3H:TMR3L) are latched into the Timer 3 Reload registers (TMR3RLH:TMR3RLL). A Timer 3 interrupt is generated if enabled.

SFR Definition 26.19. TMR4CN: Timer 4 Control

Bit	7	6	5	4	3	2	1	0
Name	TF4H	TF4L	TF4LEN		T4SPLIT	TR4		T4XCLK
Type	R/W	R/W	R/W	R	R/W	R/W	R	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x91; SFR Page = F

Bit	Name	Function
7	TF4H	**Timer 4 High Byte Overflow Flag.** Set by hardware when the Timer 4 high byte overflows from 0xFF to 0x00. In 16 bit mode, this will occur when Timer 4 overflows from 0xFFFF to 0x0000. When the Timer 4 interrupt is enabled, setting this bit causes the CPU to vector to the Timer 4 interrupt service routine. This bit is not automatically cleared by hardware.
6	TF4L	**Timer 4 Low Byte Overflow Flag.** Set by hardware when the Timer 4 low byte overflows from 0xFF to 0x00. TF4L will be set when the low byte overflows regardless of the Timer 4 mode. This bit is not automatically cleared by hardware.
5	TF4LEN	**Timer 4 Low Byte Interrupt Enable.** When set to 1, this bit enables Timer 4 Low Byte interrupts. If Timer 4 interrupts are also enabled, an interrupt will be generated when the low byte of Timer 4 overflows.
4	Unused	Read = 0b; Write = don't care.
3	T4SPLIT	**Timer 4 Split Mode Enable.** When this bit is set, Timer 4 operates as two 8-bit timers with auto-reload. 0: Timer 4 operates in 16-bit auto-reload mode. 1: Timer 4 operates as two 8-bit auto-reload timers.
2	TR4	**Timer 4 Run Control.** Timer 4 is enabled by setting this bit to 1. In 8-bit mode, this bit enables/disables TMR4H only; TMR4L is always enabled in split mode.
1	Unused	Read = 0b; Write = don't care.
0	T4XCLK	**Timer 4 External Clock Select.** This bit selects the external clock source for Timer 4. However, the Timer 4 Clock Select bits (T4MH and T4ML in register CKCON1) may still be used to select between the external clock and the system clock for either timer. 0: Timer 4 clock is the system clock divided by 12. 1: Timer 4 clock is the external clock divided by 8 (synchronized with SYSCLK).

C2 Register Definition 28.2. DEVICEID: C2 Device ID

Bit	7	6	5	4	3	2	1	0
Name	DEVICEID[7:0]							
Type	R/W							
Reset	0	0	1	0	1	0	0	0

C2 Address: 0x00

Bit	Name	Function
7:0	DEVICEID[7:0]	**Device ID.** This read-only register returns the 8-bit device ID: 0x28 (C8051F380/1/2/3/4/5/6/7/C).

C2 Register Definition 28.3. REVID: C2 Revision ID

Bit	7	6	5	4	3	2	1	0
Name	REVID[7:0]							
Type	R/W							
Reset	Varies	Varies	Varies	Varies	Varies	Varies	Varies	Varies

C2 Address: 0x01

Bit	Name	Function
7:0	REVID[7:0]	**Revision ID.** This read-only register returns the 8-bit revision ID. For example: 0x00 = Revision A.