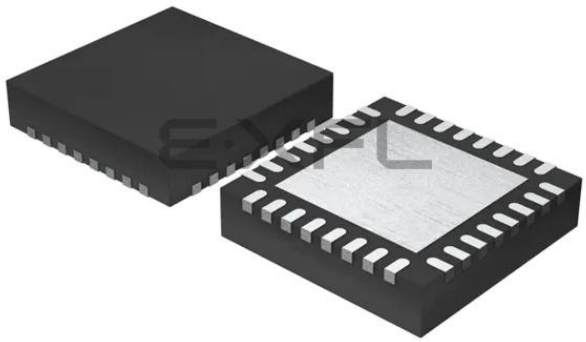

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	48 MIPS
Connectivity	I²C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.25V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f387-gm

6.1. Output Code Formatting

The conversion code format differs between Single-ended and Differential modes. The registers ADC0H and ADC0L contain the high and low bytes of the output conversion code from the ADC at the completion of each conversion. Data can be right-justified or left-justified, depending on the setting of the AD0LJST bit (ADC0CN.0). When in Single-ended Mode, conversion codes are represented as 10-bit unsigned integers. Inputs are measured from 0 to VREF x 1023/1024. Example codes are shown below for both right-justified and left-justified data. Unused bits in the ADC0H and ADC0L registers are set to 0.

Input Voltage (Single-Ended)	Right-Justified ADC0H:ADC0L (AD0LJST = 0)	Left-Justified ADC0H:ADC0L (AD0LJST = 1)
VREF x 1023/1024	0x03FF	0xFFC0
VREF x 512/1024	0x0200	0x8000
VREF x 256/1024	0x0100	0x4000
0	0x0000	0x0000

When in Differential Mode, conversion codes are represented as 10-bit signed 2s complement numbers. Inputs are measured from –VREF to VREF x 511/512. Example codes are shown below for both right-justified and left-justified data. For right-justified data, the unused MSBs of ADC0H are a sign-extension of the data word. For left-justified data, the unused LSBs in the ADC0L register are set to 0.

Input Voltage (Differential)	Right-Justified ADC0H:ADC0L (AD0LJST = 0)	Left-Justified ADC0H:ADC0L (AD0LJST = 1)
VREF x 511/512	0x01FF	0x7FC0
VREF x 256/512	0x0100	0x4000
0	0x0000	0x0000
–VREF x 256/512	0xFF00	0xC000
–VREF	0xFE00	0x8000

6.3.2. Tracking Modes

The AD0TM bit in register ADC0CN controls the ADC0 track-and-hold mode. In its default state, the ADC0 input is continuously tracked, except when a conversion is in progress. When the AD0TM bit is logic 1, ADC0 operates in low-power track-and-hold mode. In this mode, each conversion is preceded by a tracking period of 3 SAR clocks (after the start-of-conversion signal). When the CNVSTR signal is used to initiate conversions in low-power tracking mode, ADC0 tracks only when CNVSTR is low; conversion begins on the rising edge of CNVSTR. See Figure 6.4 for track and convert timing details. Tracking can also be disabled (shutdown) when the device is in low power standby or sleep modes. Low-power track-and-hold mode is also useful when AMUX settings are frequently changed, due to the settling time requirements described in Section “6.3.3. Settling Time Requirements” on page 52.

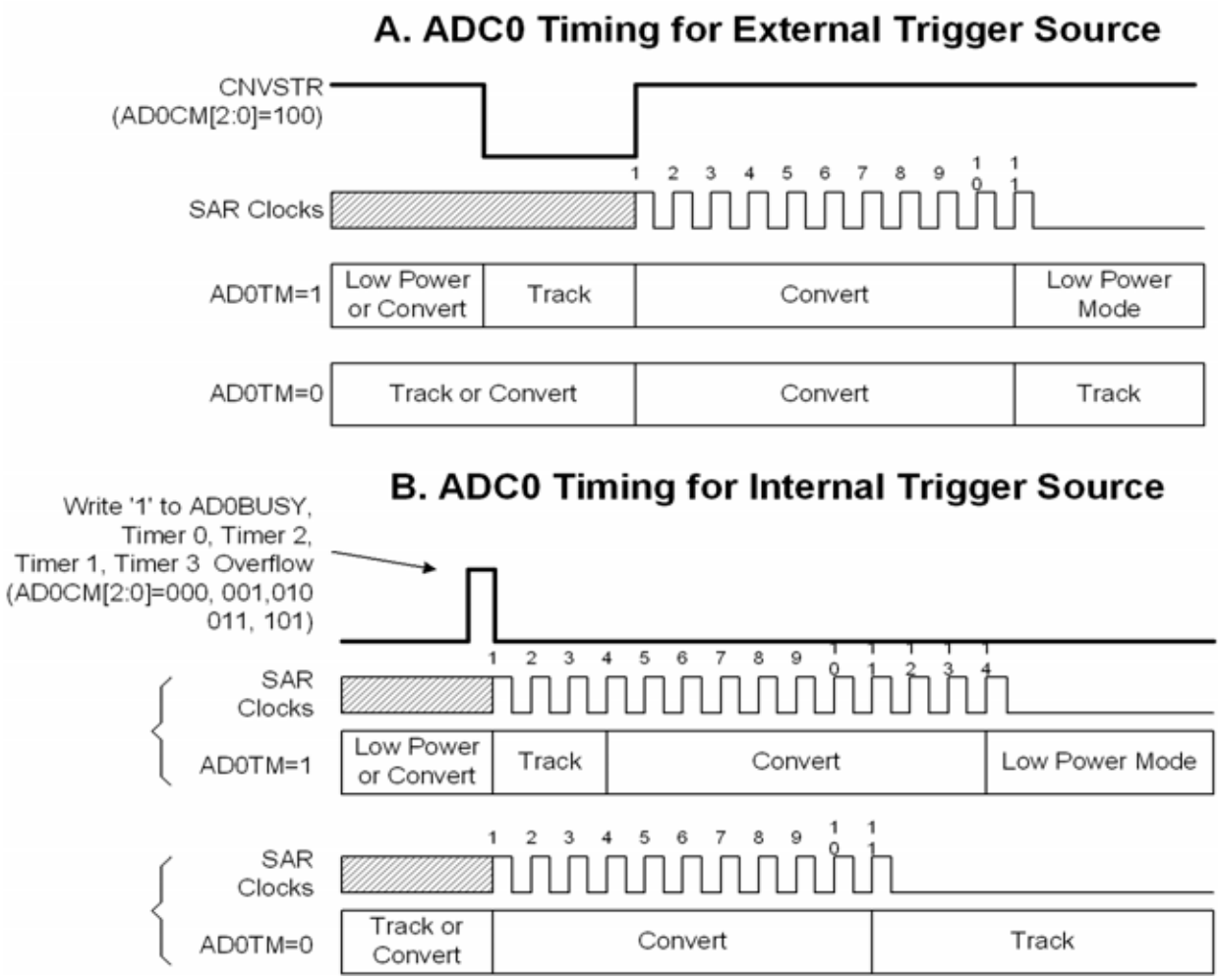

Figure 6.4. 10-Bit ADC Track and Conversion Example Timing

SFR Definition 6.1. ADC0CF: ADC0 Configuration

Bit	7	6	5	4	3	2	1	0
Name	AD0SC[4:0]					AD0LJST	Reserved	
Type	R/W					R/W	R/W	
Reset	1	1	1	1	1	0	0	0

SFR Address = 0xBC; SFR Page = All Pages

Bit	Name	Function
7:3	AD0SC[4:0]	**ADC0 SAR Conversion Clock Period Bits.** SAR Conversion clock is derived from system clock by the following equation, where *AD0SC* refers to the 5-bit value held in bits AD0SC4–0. SAR Conversion clock requirements are given in the ADC specification table. $AD0SC = \frac{SYSCLK}{CLK_{SAR}} - 1$ **Note:** If the Memory Power Controller is enabled (MPCE = '1'), AD0SC must be set to at least "00001" for proper ADC operation.
2	AD0LJST	**ADC0 Left Justify Select.** 0: Data in ADC0H:ADC0L registers are right-justified. 1: Data in ADC0H:ADC0L registers are left-justified. **Note:** The AD0LJST bit is only valid for 10-bit mode (AD08BE = 0).
1:0	Reserved	Must Write 00b.

Table 11.1. CIP-51 Instruction Set Summary (Continued)

Mnemonic	Description	Bytes	Clock Cycles
ANL C, bit	AND direct bit to Carry	2	2
ANL C, /bit	AND complement of direct bit to Carry	2	2
ORL C, bit	OR direct bit to carry	2	2
ORL C, /bit	OR complement of direct bit to Carry	2	2
MOV C, bit	Move direct bit to Carry	2	2
MOV bit, C	Move Carry to direct bit	2	2
Program Flow Timings are listed with the PFE on and FLRT = 0. Extra cycles are required for branches if FLRT = 1.			
JC rel	Jump if Carry is set	2	2/4
JNC rel	Jump if Carry is not set	2	2/4
JB bit, rel	Jump if direct bit is set	3	3/5
JNB bit, rel	Jump if direct bit is not set	3	3/5
JBC bit, rel	Jump if direct bit is set and clear bit	3	3/5
ACALL addr11	Absolute subroutine call	2	4
LCALL addr16	Long subroutine call	3	5
RET	Return from subroutine	1	6
RETI	Return from interrupt	1	6
AJMP addr11	Absolute jump	2	4
LJMP addr16	Long jump	3	5
SJMP rel	Short jump (relative address)	2	4
JMP @A+DPTR	Jump indirect relative to DPTR	1	4
JZ rel	Jump if A equals zero	2	2/4
JNZ rel	Jump if A does not equal zero	2	2/4
CJNE A, direct, rel	Compare direct byte to A and jump if not equal	3	4/6
CJNE A, #data, rel	Compare immediate to A and jump if not equal	3	3/5
CJNE Rn, #data, rel	Compare immediate to Register and jump if not equal	3	3/5
CJNE @Ri, #data, rel	Compare immediate to indirect and jump if not equal	3	4/6
DJNZ Rn, rel	Decrement Register and jump if not zero	2	2/4
DJNZ direct, rel	Decrement direct byte and jump if not zero	3	3/5
NOP	No operation	1	1

11.2. CIP-51 Register Descriptions

Following are descriptions of SFRs related to the operation of the CIP-51 System Controller. Reserved bits should always be written to the value indicated in the SFR description. Future product versions may use these bits to implement new features in which case the reset value of the bit will be the indicated value, selecting the feature's default state. Detailed descriptions of the remaining SFRs are included in the sections of the datasheet associated with their corresponding system function.

SFR Definition 11.1. DPL: Data Pointer Low Byte

Bit	7	6	5	4	3	2	1	0
Name	DPL[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x82; SFR Page = All Pages

Bit	Name	Function
7:0	DPL[7:0]	**Data Pointer Low.** The DPL register is the low byte of the 16-bit DPTR.

SFR Definition 11.2. DPH: Data Pointer High Byte

Bit	7	6	5	4	3	2	1	0
Name	DPH[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x83; SFR Page = All Pages

Bit	Name	Function
7:0	DPH[7:0]	**Data Pointer High.** The DPH register is the high byte of the 16-bit DPTR.

14.5. Multiplexed and Non-multiplexed Selection

The External Memory Interface is capable of acting in a Multiplexed mode or a Non-multiplexed mode, depending on the state of the EMD2 (EMI0CF.4) bit.

14.5.1. Multiplexed Configuration

In Multiplexed mode, the Data Bus and the lower 8-bits of the Address Bus share the same Port pins: AD[7:0]. In this mode, an external latch (74HC373 or equivalent logic gate) is used to hold the lower 8-bits of the RAM address. The external latch is controlled by the ALE (Address Latch Enable) signal, which is driven by the External Memory Interface logic. An example of a Multiplexed Configuration is shown in Figure 14.2.

In Multiplexed mode, the external MOVX operation can be broken into two phases delineated by the state of the ALE signal. During the first phase, ALE is high and the lower 8-bits of the Address Bus are presented to AD[7:0]. During this phase, the address latch is configured such that the 'Q' outputs reflect the states of the 'D' inputs. When ALE falls, signaling the beginning of the second phase, the address latch outputs remain fixed and are no longer dependent on the latch inputs. Later in the second phase, the Data Bus controls the state of the AD[7:0] port at the time $\overline{RD}$ or $\overline{WR}$ is asserted.

See Section "14.7.2. Multiplexed Mode" on page 107 for more information.

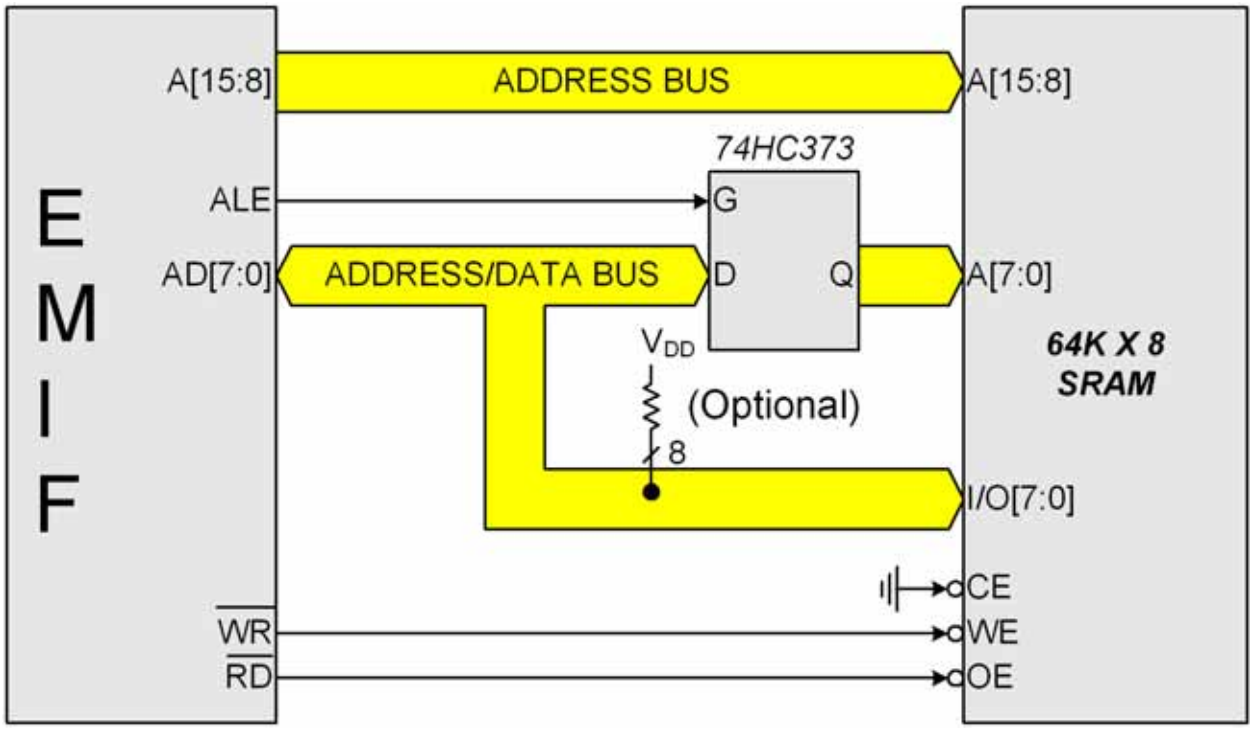

Figure 14.2. Multiplexed Configuration Example

14.5.2. Non-multiplexed Configuration

In Non-multiplexed mode, the Data Bus and the Address Bus pins are not shared. An example of a Non-multiplexed Configuration is shown in Figure 14.3. See Section "14.7.1. Non-multiplexed Mode" on page 104 for more information about Non-multiplexed operation.

Table 15.2. Special Function Registers (Continued)

SFRs are listed in alphabetical order. All undefined SFR locations are reserved

Register	Address	Page	Description	Page
SMB1CN	0xC0	F	SMBus1 Control	216
SMB1DAT	0xC2	F	SMBus1 Data	222
SMBTC	0xB9	F	SMBus0/1 Timing Control	213
SMOD1	0xE5	All Pages	UART1 Mode	246
SP	0x81	All Pages	Stack Pointer	86
SPI0CFG	0xA1	All Pages	SPI Configuration	257
SPI0CKR	0xA2	All Pages	SPI Clock Rate Control	259
SPI0CN	0xF8	All Pages	SPI Control	258
SPI0DAT	0xA3	All Pages	SPI Data	259
TCON	0x88	All Pages	Timer/Counter Control	270
TH0	0x8C	All Pages	Timer/Counter 0 High	273
TH1	0x8D	All Pages	Timer/Counter 1 High	273
TL0	0x8A	All Pages	Timer/Counter 0 Low	272
TL1	0x8B	All Pages	Timer/Counter 1 Low	272
TMOD	0x89	All Pages	Timer/Counter Mode	271
TMR2CN	0xC8	0	Timer/Counter 2 Control	278
TMR2H	0xCD	0	Timer/Counter 2 High	280
TMR2L	0xCC	0	Timer/Counter 2 Low	279
TMR2RLH	0xCB	0	Timer/Counter 2 Reload High	279
TMR2RLL	0xCA	0	Timer/Counter 2 Reload Low	279
TMR3CN	0x91	0	Timer/Counter 3 Control	285
TMR3H	0x95	0	Timer/Counter 3 High	287
TMR3L	0x94	0	Timer/Counter 3 Low	286
TMR3RLH	0x93	0	Timer/Counter 3 Reload High	286
TMR3RLL	0x92	0	Timer/Counter 3 Reload Low	286
TMR4CN	0x91	F	Timer/Counter 4 Control	290
TMR4H	0x95	F	Timer/Counter 4 High	292
TMR4L	0x94	F	Timer/Counter 4 Low	291
TMR4RLH	0x93	F	Timer/Counter 4 Reload High	291
TMR4RLL	0x92	F	Timer/Counter 4 Reload Low	291
TMR5CN	0xC8	F	Timer/Counter 5 Control	295
TMR5H	0xCD	F	Timer/Counter 5 High	297
TMR5L	0xCC	F	Timer/Counter 5 Low	296
TMR5RLH	0xCB	F	Timer/Counter 5 Reload High	296

SFR Definition 19.6. OSCXCN: External Oscillator Control

Bit	7	6	5	4	3	2	1	0
Name	XCLKVLD	XOSCMD[2:0]				XFCN[2:0]		
Type	R	R/W			R	R/W		
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xB1; SFR Page = All Pages

Bit	Name	Function
7	XCLKVLD	**External Oscillator Valid Flag.** Provides External Oscillator status and is valid at all times for all modes of operation except External CMOS Clock Mode and External CMOS Clock Mode with divide by 2. In these modes, XCLKVLD always returns 0. 0: External Oscillator is unused or not yet stable. 1: External Oscillator is running and stable.
6:4	XOSCMD[2:0]	**External Oscillator Mode Select.** 00x: External Oscillator circuit off. 010: External CMOS Clock Mode. 011: External CMOS Clock Mode with divide-by-2 stage. 100: RC Oscillator Mode with divide-by-2 stage. 101: Capacitor Oscillator Mode with divide-by-2 stage. 110: Crystal Oscillator Mode. 111: Crystal Oscillator Mode with divide-by-2 stage.
3	Unused	Read = 0; Write = don't care
2:0	XFCN[2:0]	**External Oscillator Frequency Control Bits.** Set according to the desired frequency for RC mode. Set according to the desired K Factor for C mode.

XFCN	Crystal Mode	RC Mode	C Mode
000	f ≤ 20 kHz	f ≤ 25 kHz	K Factor = 0.87
001	20 kHz < f ≤ 58 kHz	25 kHz < f ≤ 50 kHz	K Factor = 2.6
010	58 kHz < f ≤ 155 kHz	50 kHz < f ≤ 100 kHz	K Factor = 7.7
011	155 kHz < f ≤ 415 kHz	100 kHz < f ≤ 200 kHz	K Factor = 22
100	415 kHz < f ≤ 1.1 MHz	200 kHz < f ≤ 400 kHz	K Factor = 65
101	1.1 MHz < f ≤ 3.1 MHz	400 kHz < f ≤ 800 kHz	K Factor = 180
110	3.1 MHz < f ≤ 8.2 MHz	800 kHz < f ≤ 1.6 MHz	K Factor = 664
111	8.2 MHz < f ≤ 25 MHz	1.6 MHz < f ≤ 3.2 MHz	K Factor = 1590

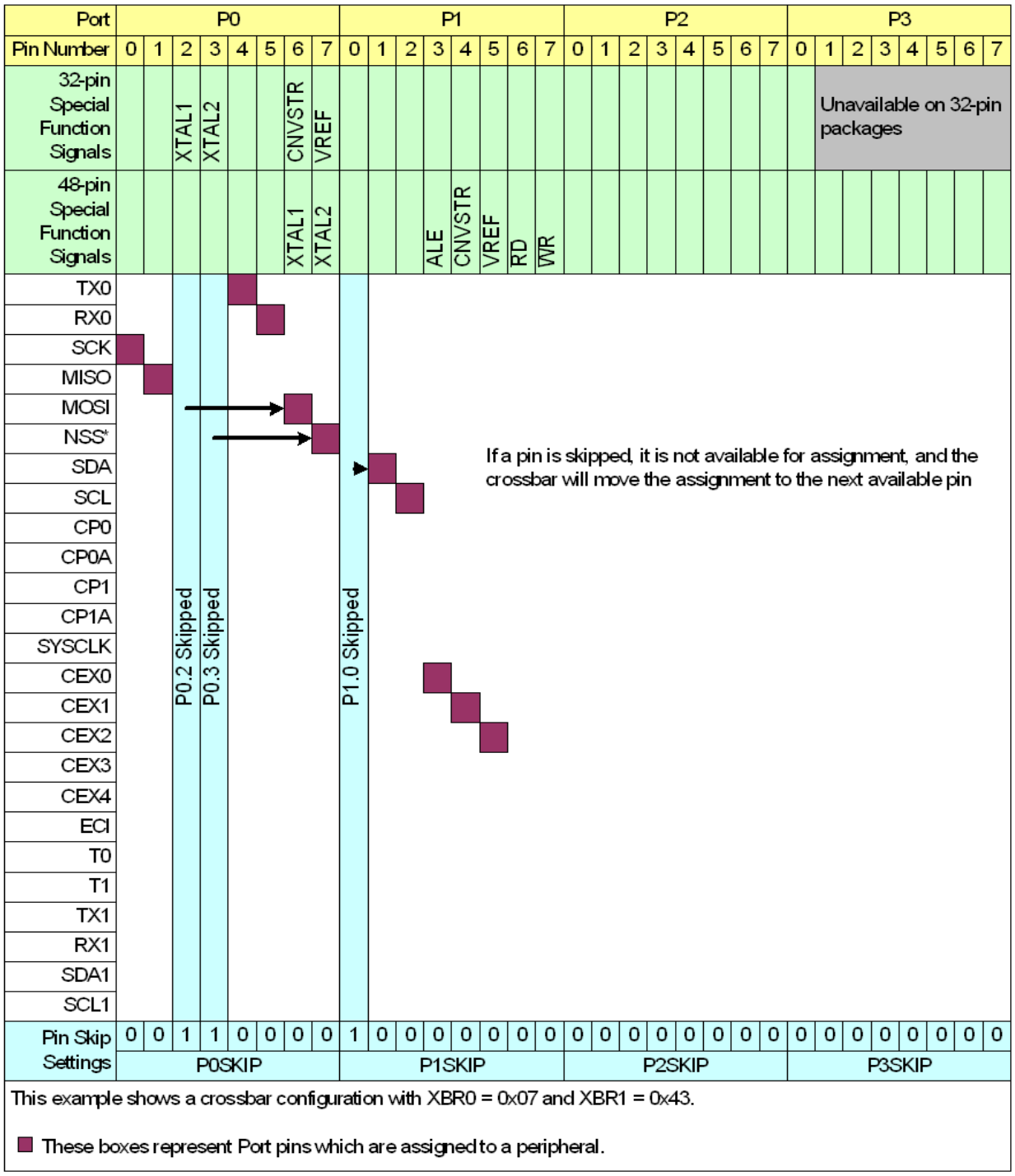

Figure 20.5. Crossbar Priority Decoder in Example Configuration (3 Pins Skipped)

SFR Definition 20.12. P2: Port 2

Bit	7	6	5	4	3	2	1	0
Name	P2[7:0]							
Type	R/W							
Reset	1	1	1	1	1	1	1	1

SFR Address = 0xA0; SFR Page = All Pages; Bit Addressable

Bit	Name	Description	Write	Read
7:0	P2[7:0]	**Port 2 Data.** Sets the Port latch logic value or reads the Port pin logic state in Port cells configured for digital I/O.	0: Set output latch to logic LOW. 1: Set output latch to logic HIGH.	0: P2.n Port pin is logic LOW. 1: P2.n Port pin is logic HIGH.

SFR Definition 20.13. P2MDIN: Port 2 Input Mode

Bit	7	6	5	4	3	2	1	0
Name	P2MDIN[7:0]							
Type	R/W							
Reset	1	1	1	1	1	1	1	1

SFR Address = 0xF3; SFR Page = All Pages

Bit	Name	Function
7:0	P2MDIN[7:0]	**Analog Configuration Bits for P2.7–P2.0 (respectively).** Port pins configured for analog mode have their weak pullup, digital driver, and digital receiver disabled. 0: Corresponding P2.n pin is configured for analog mode. 1: Corresponding P2.n pin is not configured for analog mode.

SFR Definition 21.1. USB0XCN: USB0 Transceiver Control

Bit	7	6	5	4	3	2	1	0
Name	PREN	PHYEN	SPEED	PHYTST[1:0]		DFREC	Dp	Dn
Type	R/W	R/W	R/W	R/W		R	R	R
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xD7; SFR Page = All Pages

Bit	Name	Function
7	PREN	**Internal Pull-up Resistor Enable.** The location of the pull-up resistor (D+ or D-) is determined by the SPEED bit. 0: Internal pull-up resistor disabled (device effectively detached from USB network). 1: Internal pull-up resistor enabled when VBUS is present (device attached to the USB network).
6	PHYEN	**Physical Layer Enable.** 0: USB0 physical layer Transceiver disabled (suspend). 1: USB0 physical layer Transceiver enabled (normal).
5	SPEED	**USB0 Speed Select.** This bit selects the USB0 speed. 0: USB0 operates as a Low Speed device. If enabled, the internal pull-up resistor appears on the D– line. 1: USB0 operates as a Full Speed device. If enabled, the internal pull-up resistor appears on the D+ line.
4:3	PHYTST[1:0]	**Physical Layer Test Bits.** 00: Mode 0: Normal (non-test mode) (D+ = X, D- = X) 01: Mode 1: Differential 1 Forced (D+ = 1, D- = 0) 10: Mode 2: Differential 0 Forced (D+ = 0, D- = 1) 11: Mode 3: Single-Ended 0 Forced (D+ = 0, D– = 0)
2	DFREC	**Differential Receiver Bit** The state of this bit indicates the current differential value present on the D+ and D- lines when PHYEN = 1. 0: Differential 0 signalling on the bus. 1: Differential 1 signalling on the bus.
1	Dp	**D+ Signal Status.** This bit indicates the current logic level of the D+ pin. 0: D+ signal currently at logic 0. 1: D+ signal currently at logic 1.
0	Dn	**D- Signal Status.** This bit indicates the current logic level of the D- pin. 0: D- signal currently at logic 0. 1: D- signal currently at logic 1.

21.6. Function Addressing

The FADDR register holds the current USB0 function address. Software should write the host-assigned 7-bit function address to the FADDR register when received as part of a SET_ADDRESS command. A new address written to FADDR will not take effect (USB0 will not respond to the new address) until the end of the current transfer (typically following the status phase of the SET_ADDRESS command transfer). The UPDATE bit (FADDR.7) is set to 1 by hardware when software writes a new address to the FADDR register. Hardware clears the UPDATE bit when the new address takes effect as described above.

USB Register Definition 21.7. FADDR: USB0 Function Address

Bit	7	6	5	4	3	2	1	0
Name	UPDATE	FADDR[6:0]						
Type	R	R/W						
Reset	0	0	0	0	0	0	0	0

USB Register Address = 0x00

Bit	Name	Function
7	UPDATE	**Function Address Update Bit.** Set to 1 when software writes the FADDR register. USB0 clears this bit to 0 when the new address takes effect. 0: The last address written to FADDR is in effect. 1: The last address written to FADDR is not yet in effect.
6:0	FADDR[6:0]	**Function Address Bits.** Holds the 7-bit function address for USB0. This address should be written by software when the SET_ADDRESS standard device request is received on Endpoint0. The new address takes effect when the device request completes.

21.7. Function Configuration and Control

The USB register POWER (USB Register Definition 21.8) is used to configure and control USB0 at the device level (enable/disable, Reset/Suspend/Resume handling, etc.).

USB Reset: The USBRST bit (POWER.3) is set to 1 by hardware when Reset signaling is detected on the bus. Upon this detection, the following occur:

1. The USB0 Address is reset (FADDR = 0x00).
2. Endpoint FIFOs are flushed.
3. Control/status registers are reset to 0x00 (E0CSR, EINCSRL, EINCSRH, EOUTCSRL, EOUTCSRH).
4. USB register INDEX is reset to 0x00.
5. All USB interrupts (excluding the Suspend interrupt) are enabled and their corresponding flags cleared.
6. A USB Reset interrupt is generated if enabled.

Writing a 1 to the USBRST bit will generate an asynchronous USB0 reset. All USB registers are reset to their default values following this asynchronous reset.

Suspend Mode: With Suspend Detection enabled (SUSEN = 1), USB0 will enter Suspend Mode when Suspend signaling is detected on the bus. An interrupt will be generated if enabled (SUSINTE = 1). The

22. SMBus0 and SMBus1 (I^2C Compatible)

The SMBus I/O interface is a two-wire, bi-directional serial bus. The SMBus is compliant with the System Management Bus Specification, version 1.1, and compatible with the I^2C serial bus. The C8051F380/1/2/3/4/5/6/7/C devices contain two SMBus interfaces, SMBus0 and SMBus1.

Reads and writes to the SMBus by the system controller are byte oriented with the SMBus interface autonomously controlling the serial transfer of the data. Data can be transferred at up to 1/20th of the system clock as a master or slave (this can be faster than allowed by the SMBus specification, depending on the system clock used). A method of extending the clock-low duration is available to accommodate devices with different speed capabilities on the same bus.

The SMBus may operate as a master and/or slave, and may function on a bus with multiple masters. The SMBus provides control of SDA (serial data), SCL (serial clock) generation and synchronization, arbitration logic, and START/STOP control and generation. The SMBus peripherals can be fully driven by software (i.e., software accepts/rejects slave addresses, and generates ACKs), or hardware slave address recognition and automatic ACK generation can be enabled to minimize software overhead. A block diagram of the SMBus0 peripheral and the associated SFRs is shown in Figure 22.1. SMBus1 is identical,with the exception of the available timer options for the clock source, and the timer used to implement the SCL low timeout feature. Refer to the specific SFR definitions for more details.

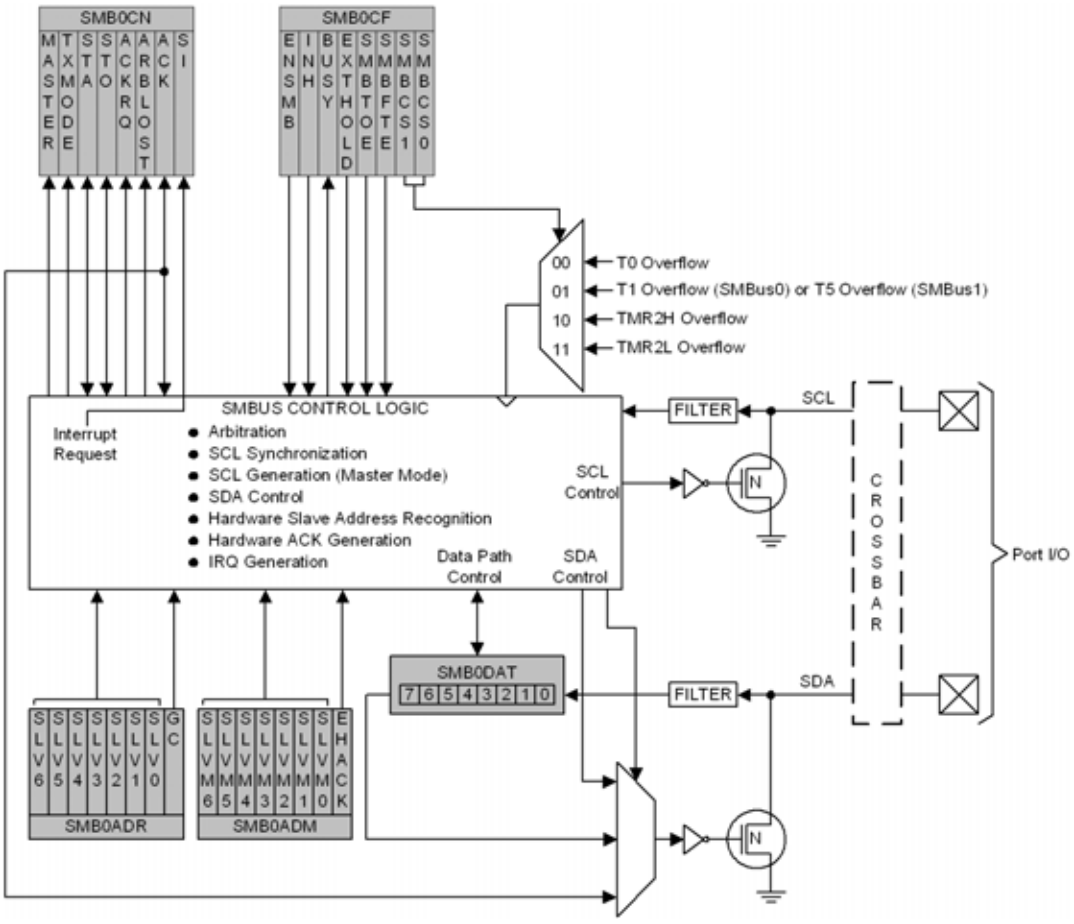

Figure 22.1. SMBus Block Diagram

SFR Definition 22.1. SMB0CF: SMBus Clock/Configuration

Bit	7	6	5	4	3	2	1	0
Name	ENSMB0	INH0	BUSY0	EXTHOLD0	SMB0TOE	SMB0FTE	SMB0CS[1:0]	
Type	R/W	R/W	R	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xC1; SFR Page = 0

Bit	Name	Function
7	ENSMB0	**SMBus0 Enable.** This bit enables the SMBus0 interface when set to 1. When enabled, the interface constantly monitors the SDA0 and SCL0 pins.
6	INH0	**SMBus0 Slave Inhibit.** When this bit is set to logic 1, the SMBus0 does not generate an interrupt when slave events occur. This effectively removes the SMBus0 slave from the bus. Master Mode interrupts are not affected.
5	BUSY0	**SMBus0 Busy Indicator.** This bit is set to logic 1 by hardware when a transfer is in progress. It is cleared to logic 0 when a STOP or free-timeout is sensed.
4	EXTHOLD0	**SMBus0 Setup and Hold Time Extension Enable.** This bit controls the SDA0 setup and hold times according to Table 22.2. 0: SDA0 Extended Setup and Hold Times disabled. 1: SDA0 Extended Setup and Hold Times enabled.
3	SMB0TOE	**SMBus0 SCL Timeout Detection Enable.** This bit enables SCL low timeout detection. If set to logic 1, the SMBus0 forces Timer 3 to reload while SCL0 is high and allows Timer 3 to count when SCL0 goes low. If Timer 3 is configured to Split Mode, only the High Byte of the timer is held in reload while SCL0 is high. Timer 3 should be programmed to generate interrupts at 25 ms, and the Timer 3 interrupt service routine should reset SMBus0 communication.
2	SMB0FTE	**SMBus0 Free Timeout Detection Enable.** When this bit is set to logic 1, the bus will be considered free if SCL0 and SDA0 remain high for more than 10 SMBus clock source periods.
1:0	SMB0CS[1:0]	**SMBus0 Clock Source Selection.** These two bits select the SMBus0 clock source, which is used to generate the SMBus0 bit rate. The selected device should be configured according to Equation 22.1. 00: Timer 0 Overflow 01: Timer 1 Overflow 10: Timer 2 High Byte Overflow 11: Timer 2 Low Byte Overflow

SFR Definition 24.2. SMOD1: UART1 Mode

Bit	7	6	5	4	3	2	1	0
Name	MCE1	S1PT[1:0]		PE1	S1DL[1:0]		XBE1	SBL1
Type	R/W	R/W		R/W	R/W		R/W	R/W
Reset	0	0	0	0	1	1	0	0

SFR Address = 0xE5; SFR Page = All Pages

Bit	Name	Function
7	MCE1	**Multiprocessor Communication Enable.** 0: RI will be activated if stop bit(s) are 1. 1: RI will be activated if stop bit(s) and extra bit are 1 (extra bit must be enabled using XBE1). Note: This function is not available when hardware parity is enabled.
6:5	S1PT[1:0]	**Parity Type Bits.** 00: Odd 01: Even 10: Mark 11: Space
4	PE1	**Parity Enable.** This bit activates hardware parity generation and checking. The parity type is selected by bits S1PT1-0 when parity is enabled. 0: Hardware parity is disabled. 1: Hardware parity is enabled.
3:2	S1DL[1:0]	**Data Length.** 00: 5-bit data 01: 6-bit data 10: 7-bit data 11: 8-bit data
1	XBE1	**Extra Bit Enable.** When enabled, the value of TBX1 will be appended to the data field. 0: Extra Bit Disabled. 1: Extra Bit Enabled.
0	SBL1	**Stop Bit Length.** 0: Short—Stop bit is active for one bit time. 1: Long—Stop bit is active for two bit times (data length = 6, 7, or 8 bits), or 1.5 bit times (data length = 5 bits).

SFR Definition 25.3. SPI0CKR: SPI0 Clock Rate

Bit	7	6	5	4	3	2	1	0
Name	SCR[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xA2; SFR Page = All Pages

Bit	Name	Function
7:0	SCR[7:0]	**SPI0 Clock Rate.** These bits determine the frequency of the SCK output when the SPI0 module is configured for master mode operation. The SCK clock frequency is a divided version of the system clock, and is given in the following equation, where *SYSCLK* is the system clock frequency and *SPI0CKR* is the 8-bit value held in the SPI0CKR register. $f_{SCK} = \frac{SYSCLK}{2 \times (SPI0CKR[7:0] + 1)}$ for $0 \leq SPI0CKR \leq 255$ Example: If SYSCLK = 2 MHz and SPI0CKR = 0x04, $f_{SCK} = \frac{2000000}{2 \times (4 + 1)}$ $f_{SCK} = 200kHz$

SFR Definition 25.4. SPI0DAT: SPI0 Data

Bit	7	6	5	4	3	2	1	0
Name	SPI0DAT[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xA3; SFR Page = All Pages

Bit	Name	Function
7:0	SPI0DAT[7:0]	**SPI0 Transmit and Receive Data.** The SPI0DAT register is used to transmit and receive SPI0 data. Writing data to SPI0DAT places the data into the transmit buffer and initiates a transfer when in Master Mode. A read of SPI0DAT returns the contents of the receive buffer.

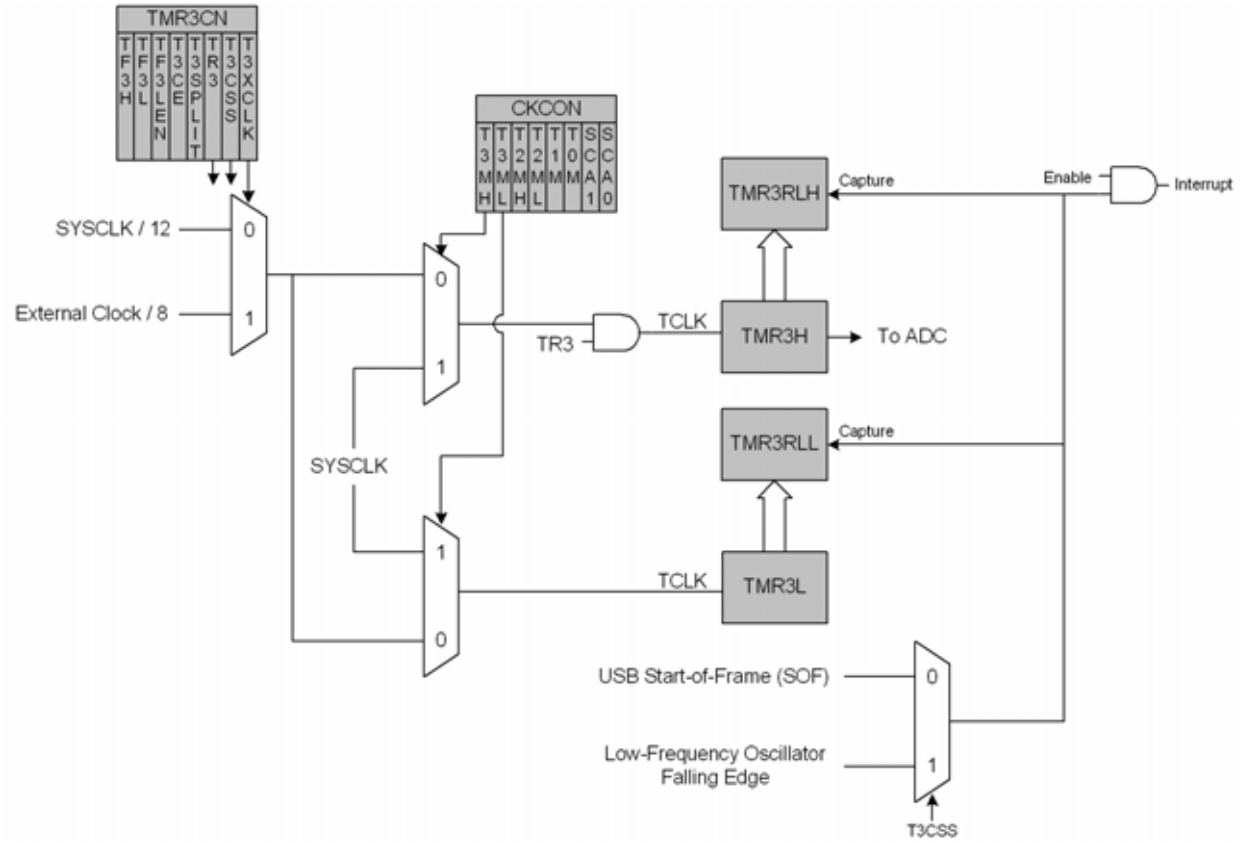

Figure 26.11. Timer 3 Capture Mode (T3SPLIT = 0)

27.3.3. High-Speed Output Mode

In High-Speed Output mode, a module's associated CEXn pin is toggled each time a match occurs between the PCA Counter and the module's 16-bit capture/compare register (PCA0CPHn and PCA0CPLn). When a match occurs, the Capture/Compare Flag (CCFn) in PCA0CN is set to logic 1. An interrupt request is generated if the CCFn interrupt for that module is enabled. The CCFn bit is not automatically cleared by hardware when the CPU vectors to the interrupt service routine, and must be cleared by software. Setting the TOGn, MATn, and ECOMn bits in the PCA0CPMn register enables the High-Speed Output mode. If ECOMn is cleared, the associated pin will retain its state, and not toggle on the next match event.

Important Note About Capture/Compare Registers: When writing a 16-bit value to the PCA0 Capture/Compare registers, the low byte should always be written first. Writing to PCA0CPLn clears the ECOMn bit to 0; writing to PCA0CPHn sets ECOMn to 1.

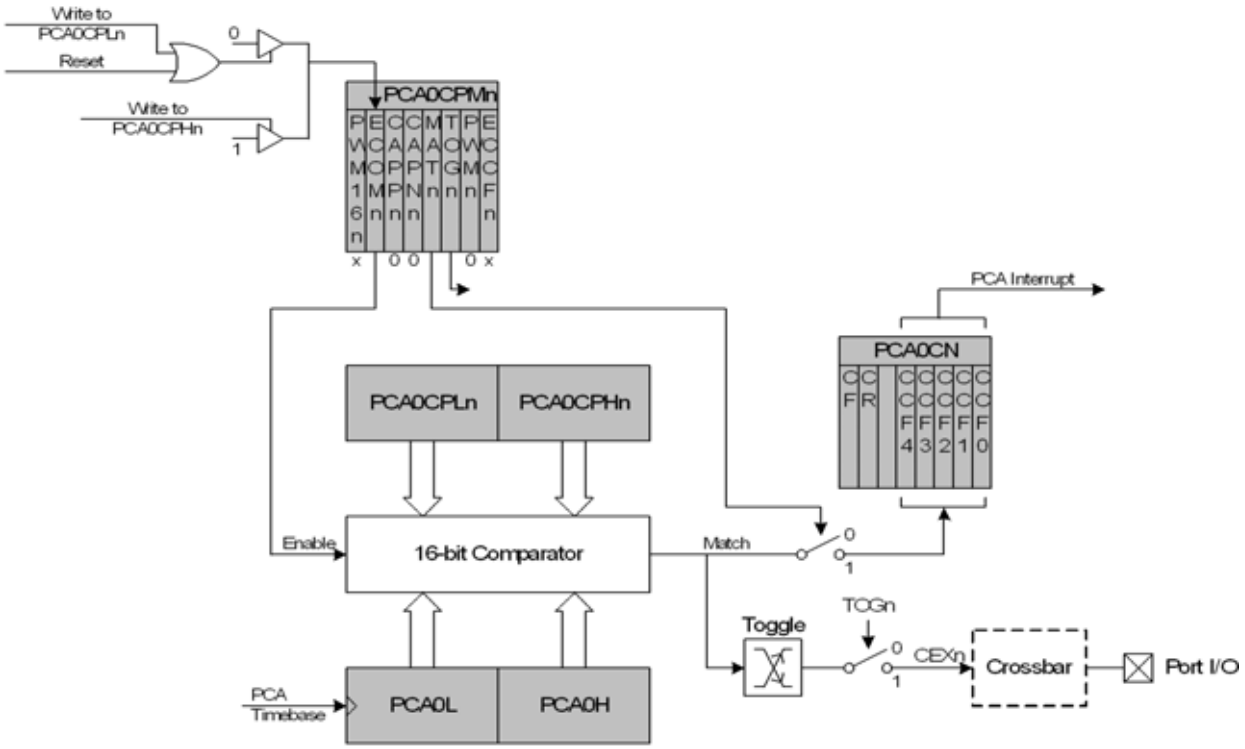

Figure 27.6. PCA High-Speed Output Mode Diagram

SFR Definition 27.3. PCA0CPMn: PCA Capture/Compare Mode

Bit	7	6	5	4	3	2	1	0
Name	PWM16n	ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMn	ECCFn
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Addresses: 0xDA (n = 0), 0xDB (n = 1), 0xDC (n = 2), 0xDD (n = 3), 0xDE (n = 4)

SFR Pages: All Pages (n = 0), All Pages (n = 1), All Pages (n = 2), All Pages (n = 3), All Pages (n = 4)

Bit	Name	Function
7	PWM16n	**16-bit Pulse Width Modulation Enable.** This bit enables 16-bit mode when Pulse Width Modulation mode is enabled. 0: 8-bit PWM selected. 1: 16-bit PWM selected.
6	ECOMn	**Comparator Function Enable.** This bit enables the comparator function for PCA module n when set to 1.
5	CAPPn	**Capture Positive Function Enable.** This bit enables the positive edge capture for PCA module n when set to 1.
4	CAPNn	**Capture Negative Function Enable.** This bit enables the negative edge capture for PCA module n when set to 1.
3	MATn	**Match Function Enable.** This bit enables the match function for PCA module n when set to 1. When enabled, matches of the PCA counter with a module's capture/compare register cause the CCFn bit in PCA0MD register to be set to logic 1.
2	TOGn	**Toggle Function Enable.** This bit enables the toggle function for PCA module n when set to 1. When enabled, matches of the PCA counter with a module's capture/compare register cause the logic level on the CEXn pin to toggle. If the PWMn bit is also set to logic 1, the module operates in Frequency Output Mode.
1	PWMn	**Pulse Width Modulation Mode Enable.** This bit enables the PWM function for PCA module n when set to 1. When enabled, a pulse width modulated signal is output on the CEXn pin. 8-bit PWM is used if PWM16n is cleared; 16-bit mode is used if PWM16n is set to logic 1. If the TOGn bit is also set, the module operates in Frequency Output Mode.
0	ECCFn	**Capture/Compare Flag Interrupt Enable.** This bit sets the masking of the Capture/Compare Flag (CCFn) interrupt. 0: Disable CCFn interrupts. 1: Enable a Capture/Compare Flag interrupt request when CCFn is set.
Note: When the WDTE bit is set to 1, the PCA0CPM4 register cannot be modified, and module 4 acts as the watchdog timer. To change the contents of the PCA0CPM4 register or the function of module 4, the Watchdog Timer must be disabled.		