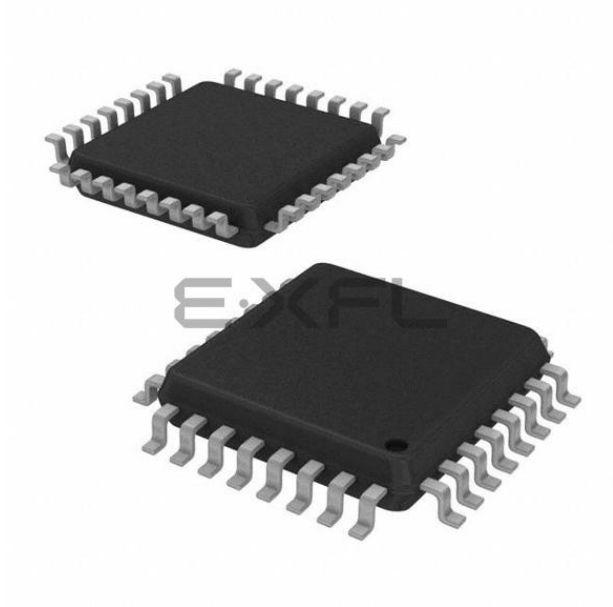

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	48 MIPS
Connectivity	I²C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	25
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.25V
Data Converters	A/D 21x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f38c-gq

4.2. USB

Figure 4.5 shows a typical connection diagram for the USB pins of the C8051F38x devices including a 100 Ω current-limiting resistor on the VBUS sense pin and ESD protection diodes on the USB pins. This current-limiting resistor is recommended for systems that may experience electrostatic discharge (ESD), latch-up, and have a greater opportunity to share signals with systems that do not have the same ground potential. This is not a required component for most applications.

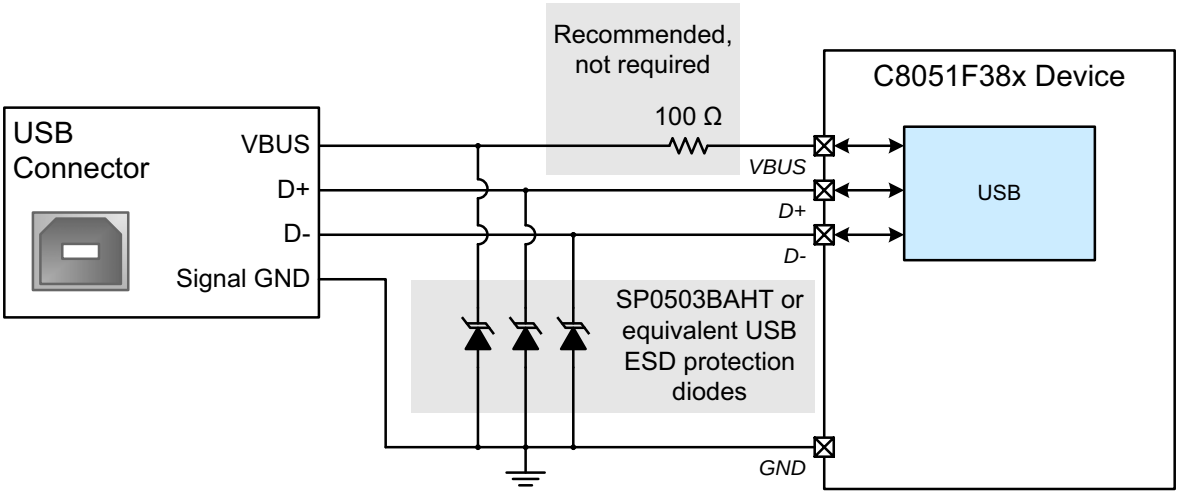

Figure 4.5. Connection Diagram for USB Pins

4.3. Voltage Reference (VREF)

Figure 4.6 shows a typical connection diagram for the voltage reference (VREF) pin of the C8051F38x devices when using the internal voltage reference. When using an external voltage reference, consult the appropriate device's data sheet for connection recommendations.

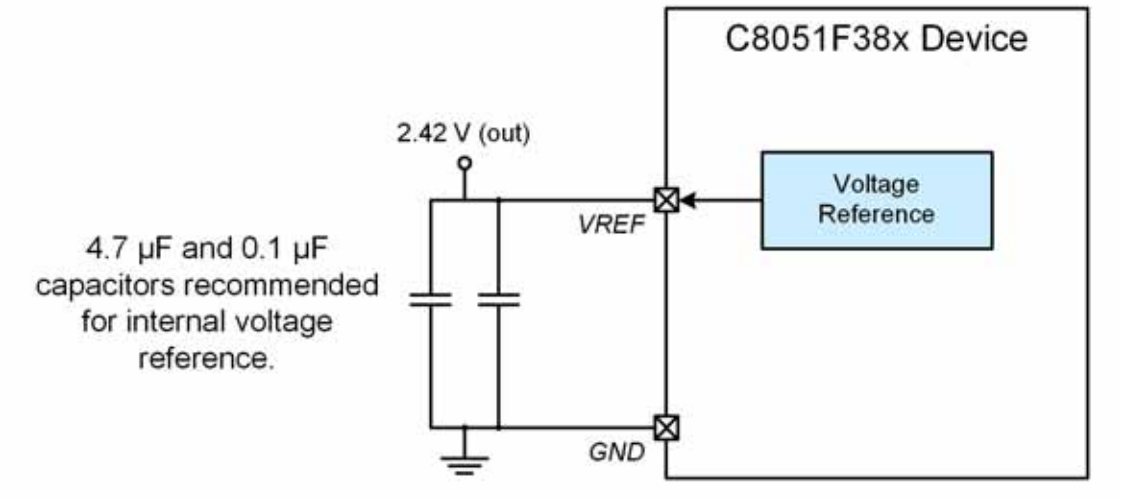

Figure 4.6. Connection Diagram for Internal Voltage Reference

5.2. Electrical Characteristics

Table 5.2. Global Electrical Characteristics

–40 to +85 °C, 25 MHz system clock unless otherwise specified.

Parameter	Test Condition	Min	Typ	Max	Unit
Digital Supply Voltage[1]		V_{RST}[1]	3.3	3.6	V
Digital Supply RAM Data Retention Voltage		—	1.5	—	V
SYSCLK (System Clock)[2]		0	—	48	MHz
Specified Operating Temperature Range		–40	—	+85	°C
Digital Supply Current—CPU Active (Normal Mode, fetching instructions from Flash)					
I_{DD}[3]	SYSCLK = 48 MHz, V_{DD} = 3.3 V	—	12	14	mA
	SYSCLK = 24 MHz, V_{DD} = 3.3 V	—	7	8	mA
	SYSCLK = 1 MHz, V_{DD} = 3.3 V	—	0.45	0.85	mA
	SYSCLK = 80 kHz, V_{DD} = 3.3 V	—	280	—	µA
Digital Supply Current—CPU Inactive (Idle Mode, not fetching instructions from Flash)					
Idle I_{DD}[3]	SYSCLK = 48 MHz, V_{DD} = 3.3 V	—	6.5	8	mA
	SYSCLK = 24 MHz, V_{DD} = 3.3 V	—	3.5	5	mA
	SYSCLK = 1 MHz, V_{DD} = 3.3 V	—	0.35	—	mA
	SYSCLK = 80 kHz, V_{DD} = 3.3 V	—	220	—	µA
Digital Supply Current (Stop or Suspend Mode, shut-down)	Oscillator not running (STOP mode), Internal Regulators OFF, V_{DD} = 3.3 V	—	1	—	µA
	Oscillator not running (STOP or SUS-PEND mode), REG0 and REG1 both in low power mode, V_{DD} = 3.3 V.	—	100	—	µA
	Oscillator not running (STOP or SUS-PEND mode), REG0 OFF, V_{DD} = 3.3 V.	—	150	—	µA
Digital Supply Current for USB Module (USB Active Mode[4])	USB Clock = 48 MHz, V_{DD} = 3.3 V	—	8	—	mA

Notes:

1. USB Requires 3.0 V Minimum Supply Voltage.
2. SYSCLK must be at least 32 kHz to enable debugging.
3. Includes normal mode bias current for REG0 and REG1. Does not include current from internal oscillators, USB, or other analog peripherals.
4. An additional 220uA is sourced by the D+ or D- pull-up to the USB bus when the USB pull-up is active.

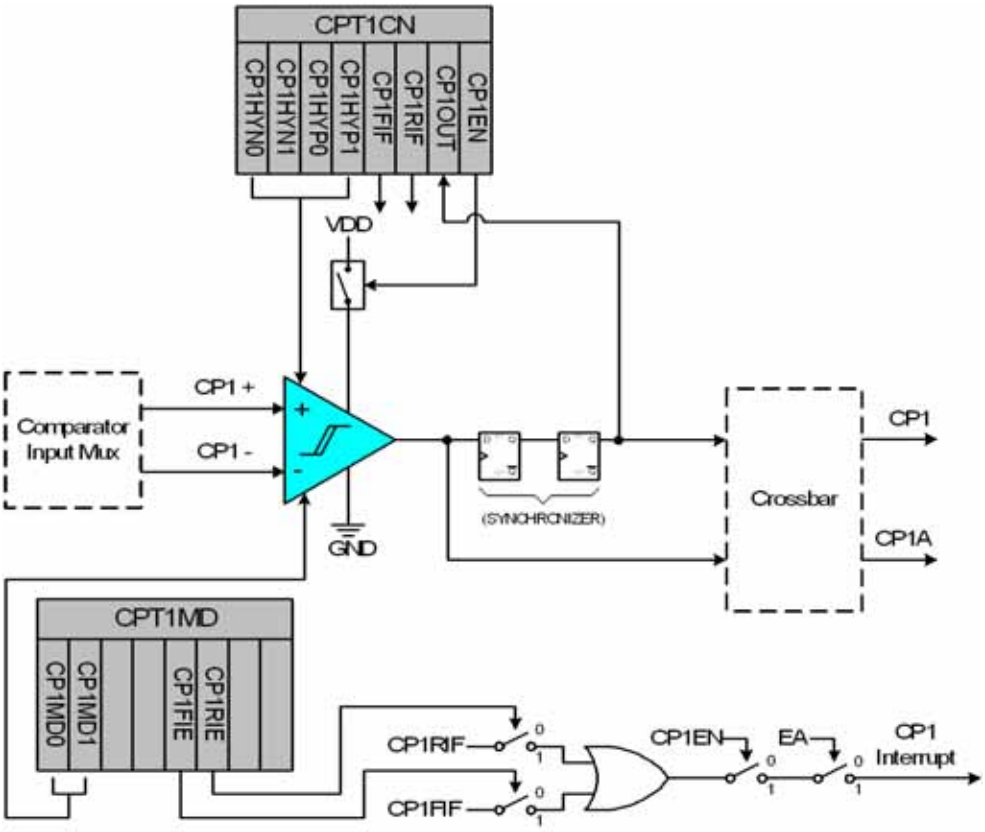

Figure 8.2. Comparator1 Functional Block Diagram

The Comparator output can be polled in software, used as an interrupt source, and/or routed to a Port pin. When routed to a Port pin, the Comparator output is available asynchronous or synchronous to the system clock; the asynchronous output is available even in STOP mode (with no system clock active). When disabled, the Comparator output (if assigned to a Port I/O pin via the Crossbar) defaults to the logic low state, and the power supply to the comparator is turned off. See Section “20.1. Priority Crossbar Decoder” on page 154 for details on configuring Comparator outputs via the digital Crossbar. Comparator inputs can be externally driven from –0.25 V to (V_{DD}) + 0.25 V without damage or upset. The complete Comparator electrical specifications are given in Section “5. Electrical Characteristics” on page 37.

The Comparator response time may be configured in software via the CPTnMD registers (see SFR Definition 8.2 and SFR Definition 8.4). Selecting a longer response time reduces the Comparator supply current.

Table 11.1. CIP-51 Instruction Set Summary (Continued)

Mnemonic	Description	Bytes	Clock Cycles
ANL C, bit	AND direct bit to Carry	2	2
ANL C, /bit	AND complement of direct bit to Carry	2	2
ORL C, bit	OR direct bit to carry	2	2
ORL C, /bit	OR complement of direct bit to Carry	2	2
MOV C, bit	Move direct bit to Carry	2	2
MOV bit, C	Move Carry to direct bit	2	2
Program Flow Timings are listed with the PFE on and FLRT = 0. Extra cycles are required for branches if FLRT = 1.			
JC rel	Jump if Carry is set	2	2/4
JNC rel	Jump if Carry is not set	2	2/4
JB bit, rel	Jump if direct bit is set	3	3/5
JNB bit, rel	Jump if direct bit is not set	3	3/5
JBC bit, rel	Jump if direct bit is set and clear bit	3	3/5
ACALL addr11	Absolute subroutine call	2	4
LCALL addr16	Long subroutine call	3	5
RET	Return from subroutine	1	6
RETI	Return from interrupt	1	6
AJMP addr11	Absolute jump	2	4
LJMP addr16	Long jump	3	5
SJMP rel	Short jump (relative address)	2	4
JMP @A+DPTR	Jump indirect relative to DPTR	1	4
JZ rel	Jump if A equals zero	2	2/4
JNZ rel	Jump if A does not equal zero	2	2/4
CJNE A, direct, rel	Compare direct byte to A and jump if not equal	3	4/6
CJNE A, #data, rel	Compare immediate to A and jump if not equal	3	3/5
CJNE Rn, #data, rel	Compare immediate to Register and jump if not equal	3	3/5
CJNE @Ri, #data, rel	Compare immediate to indirect and jump if not equal	3	4/6
DJNZ Rn, rel	Decrement Register and jump if not zero	2	2/4
DJNZ direct, rel	Decrement direct byte and jump if not zero	3	3/5
NOP	No operation	1	1

Notes on Registers, Operands and Addressing Modes:
Rn - Register R0–R7 of the currently selected register bank. **@Ri** - Data RAM location addressed indirectly through R0 or R1. **rel** - 8-bit, signed (two's complement) offset relative to the first byte of the following instruction. Used by SJMP and all conditional jumps. **direct** - 8-bit internal data location's address. This could be a direct-access Data RAM location (0x00–0x7F) or an SFR (0x80–0xFF). **#data** - 8-bit constant **#data16** - 16-bit constant **bit** - Direct-accessed bit in Data RAM or SFR **addr11** - 11-bit destination address used by ACALL and AJMP. The destination must be within the same 2 kB page of program memory as the first byte of the following instruction. **addr16** - 16-bit destination address used by LCALL and LJMP. The destination may be anywhere within the 8 kB program memory space. There is one unused opcode (0xA5) that performs the same function as NOP. All mnemonics copyrighted © Intel Corporation 1980.

14. External Data Memory Interface and On-Chip XRAM

4 kB (C8051F380/1/4/5) or 2 kB (C8051F382/3/6/7/C) of RAM are included on-chip, and mapped into the external data memory space (XRAM). The 1 kB of USB FIFO space can also be mapped into XRAM address space for additional general-purpose data storage. Additionally, an External Memory Interface (EMIF) is available on the C8051F380/2/4/6 devices, which can be used to access off-chip data memories and memory-mapped devices connected to the GPIO ports. The external memory space may be accessed using the external move instruction (MOVX) and the data pointer (DPTR), or using the MOVX indirect addressing mode using R0 or R1. If the MOVX instruction is used with an 8-bit address operand (such as @R1), then the high byte of the 16-bit address is provided by the External Memory Interface Control Register (EMI0CN, shown in SFR Definition 14.1). Note: the MOVX instruction can also be used for writing to the FLASH memory. See Section “18. Flash Memory” on page 135 for details. The MOVX instruction accesses XRAM by default.

14.1. Accessing XRAM

The XRAM memory space is accessed using the MOVX instruction. The MOVX instruction has two forms, both of which use an indirect addressing method. The first method uses the Data Pointer, DPTR, a 16-bit register which contains the effective address of the XRAM location to be read from or written to. The second method uses R0 or R1 in combination with the EMI0CN register to generate the effective XRAM address. Examples of both of these methods are given below.

14.1.1. 16-Bit MOVX Example

The 16-bit form of the MOVX instruction accesses the memory location pointed to by the contents of the DPTR register. The following series of instructions reads the value of the byte at address 0x1234 into the accumulator A:

```
MOV    DPTR, #1234h        ; load DPTR with 16-bit address to read (0x1234)
MOVX   A, @DPTR            ; load contents of 0x1234 into accumulator A
```

The above example uses the 16-bit immediate MOV instruction to set the contents of DPTR. Alternately, the DPTR can be accessed through the SFR registers DPH, which contains the upper 8-bits of DPTR, and DPL, which contains the lower 8-bits of DPTR.

14.1.2. 8-Bit MOVX Example

The 8-bit form of the MOVX instruction uses the contents of the EMI0CN SFR to determine the upper 8-bits of the effective address to be accessed and the contents of R0 or R1 to determine the lower 8-bits of the effective address to be accessed. The following series of instructions read the contents of the byte at address 0x1234 into the accumulator A.

```
MOV    EMI0CN, #12h        ; load high byte of address into EMI0CN
MOV    R0, #34h            ; load low byte of address into R0 (or R1)
MOVX   a, @R0              ; load contents of 0x1234 into accumulator A
```

14.7.1.3. 8-bit MOVX with Bank Select: EMI0CF[4:2] = 110

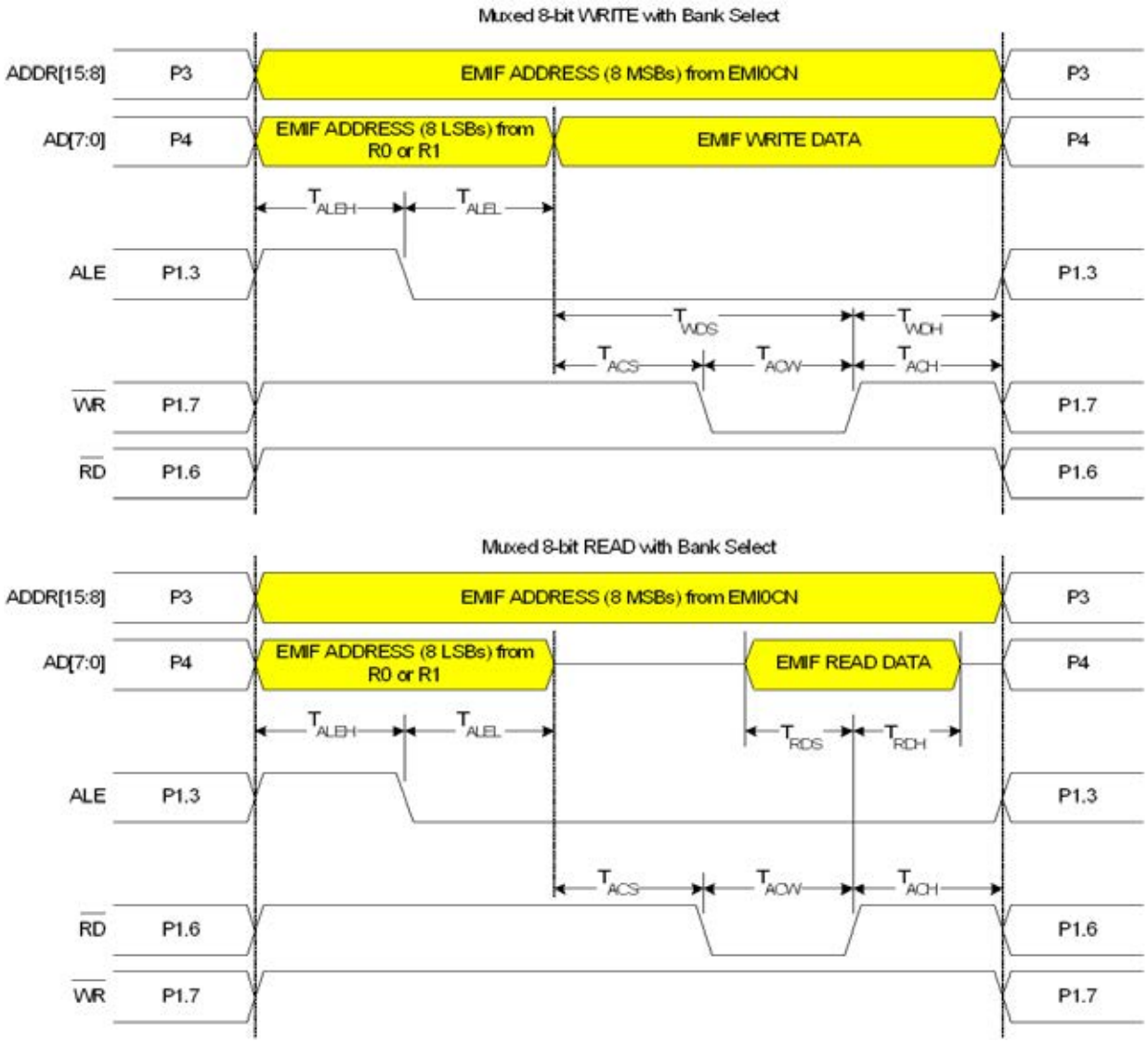

Figure 14.7. Non-multiplexed 8-bit MOVX with Bank Select Timing

19.3. Programmable Internal High-Frequency (H-F) Oscillator

All C8051F380/1/2/3/4/5/6/7/C devices include a programmable internal high-frequency oscillator that defaults as the system clock after a system reset. The internal oscillator period can be adjusted via the OSCICL register as defined by SFR Definition 19.2.

On C8051F380/1/2/3/4/5/6/7/C devices, OSCICL is factory calibrated to obtain a 48 MHz base frequency. Note that the system clock may be derived from the programmed internal oscillator divided by 1, 2, 4, or 8 after a divide by 4 stage, as defined by the IFCN bits in register OSCICN. The divide value defaults to 8 following a reset, which results in a 1.5 MHz system clock.

19.3.1. Internal Oscillator Suspend Mode

When software writes a logic 1 to SUSPEND (OSCICN.5), the internal oscillator is suspended. If the system clock is derived from the internal oscillator, the input clock to the peripheral or CIP-51 will be stopped until a non-idle USB event is detected or a rising or falling edge occurs on the VBUS signal. Note that the USB transceiver can still detect USB events when it is disabled.

When one of the oscillator awakening events occur, the internal oscillator, CIP-51, and affected peripherals resume normal operation. The CPU resumes execution at the instruction following the write to the SUSPEND bit.

Note: The prefetch engine can be turned off in suspend mode to save power. Additionally, both Voltage Regulators (REG0 and REG1) have low-power modes for additional power savings in suspend mode.

SFR Definition 19.2. OSCICL: Internal H-F Oscillator Calibration

Bit	7	6	5	4	3	2	1	0
Name		OSCICL[6:0]						
Type	R	R/W						
Reset	0	Varies	Varies	Varies	Varies	Varies	Varies	Varies

SFR Address = 0xB3; SFR Page = All Pages

Bit	Name	Function
7	Unused	Read = 0; Write = don't care
6:0	OSCICL[6:0]	**Internal Oscillator Calibration Bits.** These bits determine the internal oscillator period. When set to 0000000b, the H-F oscillator operates at its fastest setting. When set to 1111111b, the H-F oscillator operates at its slowest setting. The reset value is factory calibrated to generate an internal oscillator frequency of 48 MHz. OSCICL should only be changed by firmware when the H-F oscillator is disabled (IOSCEN = 0).

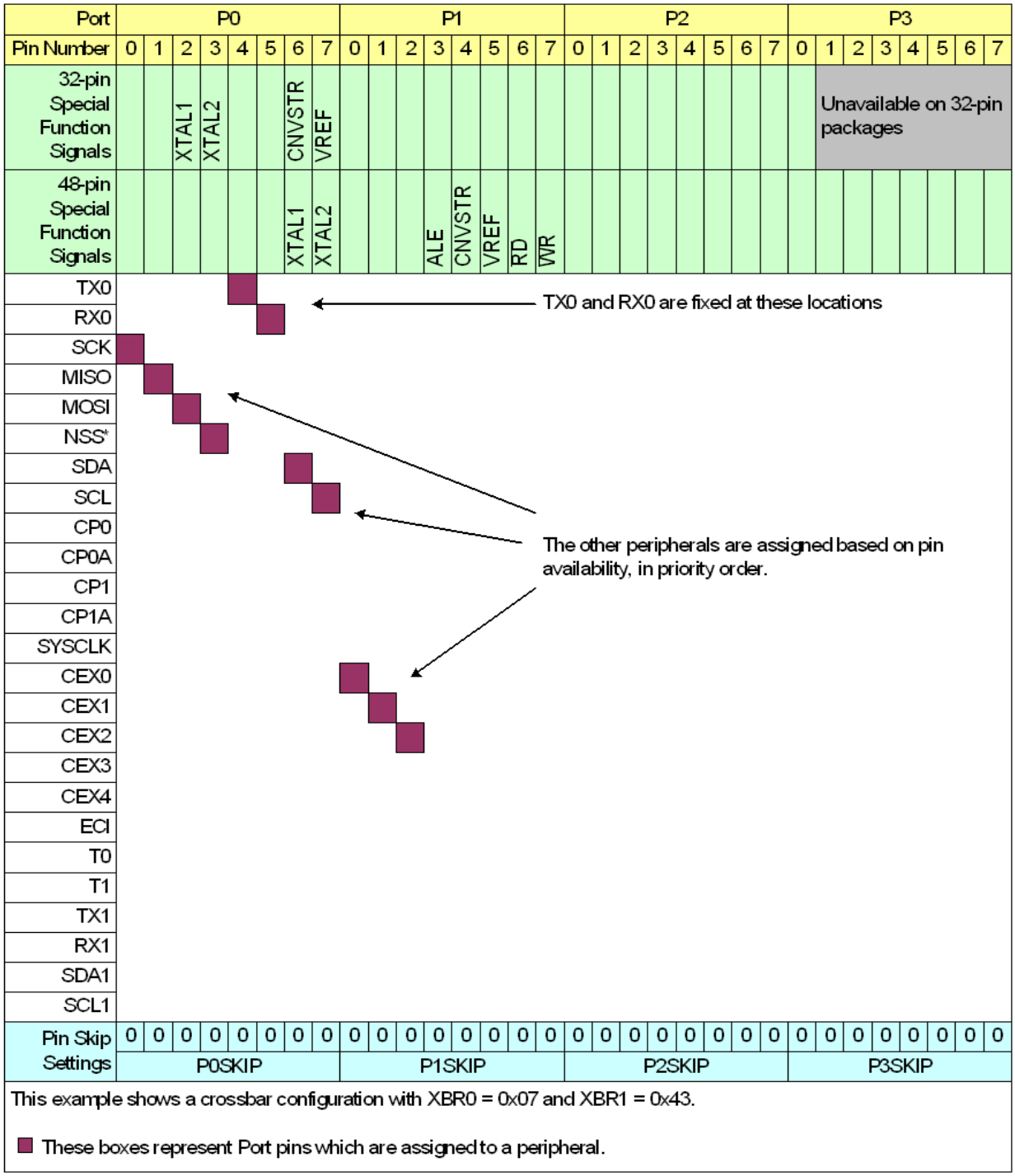

Figure 20.4. Crossbar Priority Decoder in Example Configuration (No Pins Skipped)

Table 21.1. Endpoint Addressing Scheme

Endpoint	Associated Pipes	USB Protocol Address
Endpoint0	Endpoint0 IN	0x00
	Endpoint0 OUT	0x00
Endpoint1	Endpoint1 IN	0x81
	Endpoint1 OUT	0x01
Endpoint2	Endpoint2 IN	0x82
	Endpoint2 OUT	0x02
Endpoint3	Endpoint3 IN	0x83
	Endpoint3 OUT	0x03

21.2. USB Transceiver

The USB Transceiver is configured via the USB0XCN register shown in SFR Definition 21.1. This configuration includes Transceiver enable/disable, pull-up resistor enable/disable, and device speed selection (Full or Low Speed). When bit SPEED = 1, USB0 operates as a Full Speed USB function, and the on-chip pull-up resistor (if enabled) appears on the D+ pin. When bit SPEED = 0, USB0 operates as a Low Speed USB function, and the on-chip pull-up resistor (if enabled) appears on the D- pin. Bits4-0 of register USB0XCN can be used for Transceiver testing as described in SFR Definition 21.1. The pull-up resistor is enabled only when VBUS is present (see Section “9.1.2. VBUS Detection” on page 74 for details on VBUS detection).

Important Note: The USB clock should be active before the Transceiver is enabled.

SFR Definition 22.3. SMBTC: SMBus Timing Control

Bit	7	6	5	4	3	2	1	0
Name					SMB1SDD[1:0]		SMB0SDD[1:0]	
Type	R	R	R	R	R/W		R/W	
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xB9; SFR Page = F

Bit	Name	Function
7:4	Unused	Read = 0000b; Write = don't care.
3:2	SMB1SDD[1:0]	**SMBus1 Start Detection Window** These bits increase the hold time requirement between SDA falling and SCL falling for START detection. 00: No additional hold time requirement (0-1 SYSCLK). 01: Increase hold time window to 2-3 SYSCLKs. 10: Increase hold time window to 4-5 SYSCLKs. 11: Increase hold time window to 8-9 SYSCLKs.
1:0	SMB0SDD[1:0]	**SMBus0 Start Detection Window** These bits increase the hold time requirement between SDA falling and SCL falling for START detection. 00: No additional hold time window (0-1 SYSCLK). 01: Increase hold time window to 2-3 SYSCLKs. 10: Increase hold time window to 4-5 SYSCLKs. 11: Increase hold time window to 8-9 SYSCLKs.

SFR Definition 24.1. SCON1: UART1 Control

Bit	7	6	5	4	3	2	1	0
Name	OVR1	PERR1	THRE1	REN1	TBX1	RBX1	TI1	RI1
Type	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W
Reset	0	0	1	0	0	0	0	0

SFR Address = 0xD2; SFR Page = All Pages

Bit	Name	Function
7	OVR1	**Receive FIFO Overrun Flag.** This bit indicates a receive FIFO overrun condition, where an incoming character is discarded due to a full FIFO. This bit must be cleared to 0 by software. 0: Receive FIFO Overrun has not occurred. 1: Receive FIFO Overrun has occurred.
6	PERR1	**Parity Error Flag.** When parity is enabled, this bit indicates that a parity error has occurred. It is set to 1 when the parity of the oldest byte in the FIFO does not match the selected Parity Type. This bit must be cleared to 0 by software. 0: Parity Error has not occurred. 1: Parity Error has occurred.
5	THRE1	**Transmit Holding Register Empty Flag.** 0: Transmit Holding Register not Empty - do not write to SBUF1. 1: Transmit Holding Register Empty - it is safe to write to SBUF1.
4	REN1	**Receive Enable.** This bit enables/disables the UART receiver. When disabled, bytes can still be read from the receive FIFO. 0: UART1 reception disabled. 1: UART1 reception enabled.
3	TBX1	**Extra Transmission Bit.** The logic level of this bit will be assigned to the extra transmission bit when XBE1 = 1. This bit is not used when Parity is enabled.
2	RBX1	**Extra Receive Bit.** RBX1 is assigned the value of the extra bit when XBE1 = 1. If XBE1 is cleared to 0, RBX1 is assigned the logic level of the first stop bit. This bit is not valid when Parity is enabled.
1	TI1	**Transmit Interrupt Flag.** Set to a 1 by hardware after data has been transmitted at the beginning of the STOP bit. When the UART1 interrupt is enabled, setting this bit causes the CPU to vector to the UART1 interrupt service routine. This bit must be cleared manually by software.
0	RI1	**Receive Interrupt Flag.** Set to 1 by hardware when a byte of data has been received by UART1 (set at the STOP bit sampling time). When the UART1 interrupt is enabled, setting this bit to 1 causes the CPU to vector to the UART1 interrupt service routine. This bit must be cleared manually by software. Note that RI1 will remain set to '1' as long as there is still data in the UART FIFO. After the last byte has been shifted from the FIFO to SBUF1, RI1 can be cleared.

26.1. Timer 0 and Timer 1

Each timer is implemented as a 16-bit register accessed as two separate bytes: a low byte (TL0 or TL1) and a high byte (TH0 or TH1). The Counter/Timer Control register (TCON) is used to enable Timer 0 and Timer 1 as well as indicate status. Timer 0 interrupts can be enabled by setting the ET0 bit in the IE register; Timer 1 interrupts can be enabled by setting the ET1 bit in the IE register. Both counter/timers operate in one of four primary modes selected by setting the Mode Select bits T1M1–T0M0 in the Counter/Timer Mode register (TMOD). Each timer can be configured independently. Each operating mode is described below.

26.1.1. Mode 0: 13-bit Counter/Timer

Timer 0 and Timer 1 operate as 13-bit counter/timers in Mode 0. The following describes the configuration and operation of Timer 0. However, both timers operate identically, and Timer 1 is configured in the same manner as described for Timer 0.

The TH0 register holds the eight MSBs of the 13-bit counter/timer. TL0 holds the five LSBs in bit positions TL0.4–TL0.0. The three upper bits of TL0 (TL0.7–TL0.5) are indeterminate and should be masked out or ignored when reading. As the 13-bit timer register increments and overflows from 0x1FFF (all ones) to 0x0000, the timer overflow flag TF0 in TCON is set and an interrupt will occur if Timer 0 interrupts are enabled.

The C/T0 bit in the TMOD register selects the counter/timer's clock source. When C/T0 is set to logic 1, high-to-low transitions at the selected Timer 0 input pin (T0) increment the timer register (Refer to Section “20.1. Priority Crossbar Decoder” on page 154 for information on selecting and configuring external I/O pins). Clearing C/T selects the clock defined by the T0M bit in register CKCON. When T0M is set, Timer 0 is clocked by the system clock. When T0M is cleared, Timer 0 is clocked by the source selected by the Clock Scale bits in CKCON (see SFR Definition 26.1).

Setting the TR0 bit (TCON.4) enables the timer when either GATE0 in the TMOD register is logic 0 or the input signal $\overline{INT0}$ is active as defined by bit IN0PL in register IT01CF. Setting GATE0 to 1 allows the timer to be controlled by the external input signal $\overline{INT0}$, facilitating pulse width measurements

TR0	GATE0	$\overline{INT0}$	Counter/Timer
0	X	X	Disabled
1	0	X	Enabled
1	1	0	Disabled
1	1	1	Enabled
Note: X = Don't Care			

Setting TR0 does not force the timer to reset. The timer registers should be loaded with the desired initial value before the timer is enabled.

TL1 and TH1 form the 13-bit register for Timer 1 in the same manner as described above for TL0 and TH0. Timer 1 is configured and controlled using the relevant TCON and TMOD bits just as with Timer 0. The input signal $\overline{INT1}$ is used with Timer 1; the $\overline{INT1}$ polarity is defined by bit IN1PL in register IT01CF.

SFR Definition 26.5. TL0: Timer 0 Low Byte

Bit	7	6	5	4	3	2	1	0
Name	TL0[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x8A; SFR Page = All Pages

Bit	Name	Function
7:0	TL0[7:0]	**Timer 0 Low Byte.** The TL0 register is the low byte of the 16-bit Timer 0.

SFR Definition 26.6. TL1: Timer 1 Low Byte

Bit	7	6	5	4	3	2	1	0
Name	TL1[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x8B; SFR Page = All Pages

Bit	Name	Function
7:0	TL1[7:0]	**Timer 1 Low Byte.** The TL1 register is the low byte of the 16-bit Timer 1.

Each time a capture event is received, the contents of the Timer 2 registers (TMR2H:TMR2L) are latched into the Timer 2 Reload registers (TMR2RLH:TMR2RLL). A Timer 2 interrupt is generated if enabled.

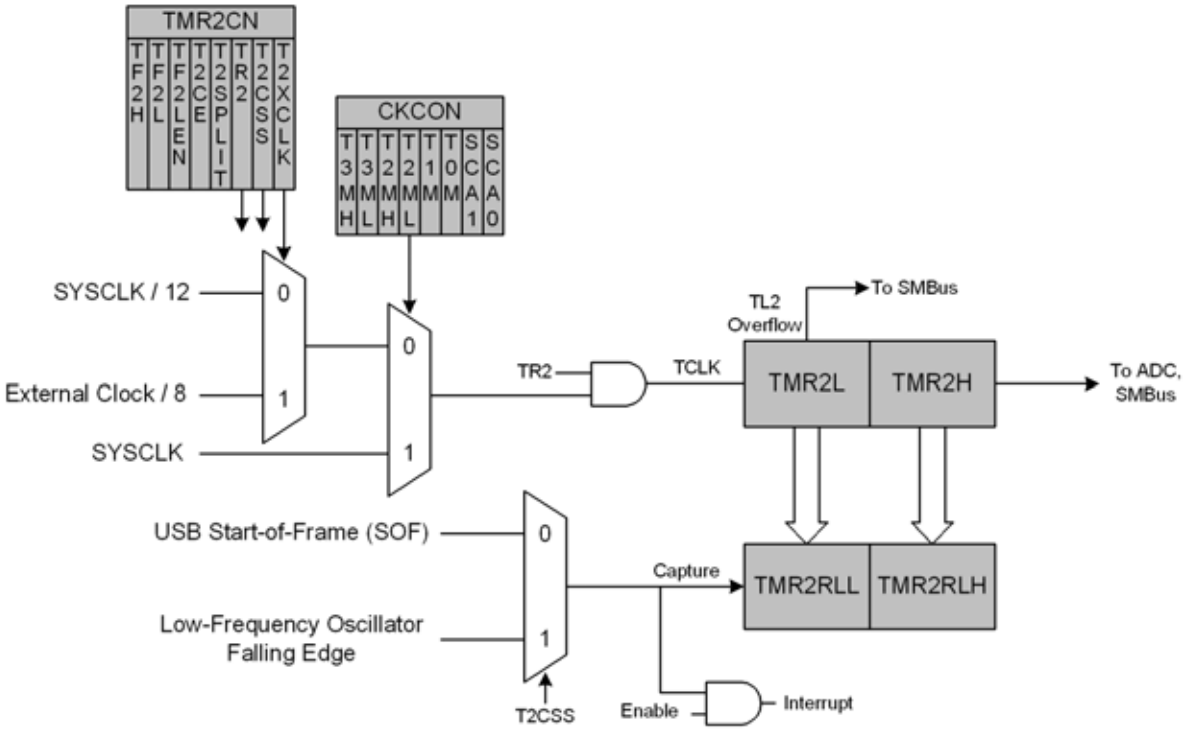

Figure 26.6. Timer 2 Capture Mode (T2SPLIT = 0)

When T2SPLIT = 1, the Timer 2 registers (TMR2H and TMR2L) act as two 8-bit counters. Each counter counts up independently and overflows from 0xFF to 0x00. Each time a capture event is received, the contents of the Timer 2 registers are latched into the Timer 2 Reload registers (TMR2RLH and TMR2RLL). A Timer 2 interrupt is generated if enabled.

SFR Definition 26.14. TMR3CN: Timer 3 Control

Bit	7	6	5	4	3	2	1	0
Name	TF3H	TF3L	TF3LEN	TF3CEN	T3SPLIT	TR3	T3CSS	T3XCLK
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x91; SFR Page = 0

Bit	Name	Function
7	TF3H	**Timer 3 High Byte Overflow Flag.** Set by hardware when the Timer 3 high byte overflows from 0xFF to 0x00. In 16 bit mode, this will occur when Timer 3 overflows from 0xFFFF to 0x0000. When the Timer 3 interrupt is enabled, setting this bit causes the CPU to vector to the Timer 3 interrupt service routine. This bit is not automatically cleared by hardware.
6	TF3L	**Timer 3 Low Byte Overflow Flag.** Set by hardware when the Timer 3 low byte overflows from 0xFF to 0x00. TF3L will be set when the low byte overflows regardless of the Timer 3 mode. This bit is not automatically cleared by hardware.
5	TF3LEN	**Timer 3 Low Byte Interrupt Enable.** When set to 1, this bit enables Timer 3 Low Byte interrupts. If Timer 3 interrupts are also enabled, an interrupt will be generated when the low byte of Timer 3 overflows.
4	TF3CEN	**Timer 3 Low-Frequency Oscillator Capture Enable.** When set to 1, this bit enables Timer 3 Low-Frequency Oscillator Capture Mode. If TF3CEN is set and Timer 3 interrupts are enabled, an interrupt will be generated on a falling edge of the low-frequency oscillator output, and the current 16-bit timer value in TMR3H:TMR3L will be copied to TMR3RLH:TMR3RLL.
3	T3SPLIT	**Timer 3 Split Mode Enable.** When this bit is set, Timer 3 operates as two 8-bit timers with auto-reload.
2	TR3	**Timer 3 Run Control.** Timer 3 is enabled by setting this bit to 1. In 8-bit mode, this bit enables/disables TMR3H only; TMR3L is always enabled in split mode.
1	T3CSS	**Timer 3 Capture Source Select.** This bit selects the source of a capture event when bit T2CE is set to 1. 0: Capture source is USB SOF event. 1: Capture source is falling edge of Low-Frequency Oscillator.
0	T3XCLK	**Timer 3 External Clock Select.** This bit selects the external clock source for Timer 3. However, the Timer 3 Clock Select bits (T3MH and T3ML in register CKCON) may still be used to select between the external clock and the system clock for either timer. 0: Timer 3 clock is the system clock divided by 12. 1: Timer 3 clock is the external clock divided by 8 (synchronized with SYSCLK).

26.5. Timer 5

Timer 5 is a 16-bit timer formed by two 8-bit SFRs: TMR5L (low byte) and TMR5H (high byte). Timer 5 may operate in 16-bit auto-reload mode or (split) 8-bit auto-reload mode. The T5SPLIT bit (TMR5CN.3) defines

Timer 5 may be clocked by the system clock, the system clock divided by 12, or the external oscillator source divided by 8. Note that the external oscillator source divided by 8 is synchronized with the system clock.

26.5.1. 16-bit Timer with Auto-Reload

When T5SPLIT (TMR5CN.3) is zero, Timer 5 operates as a 16-bit timer with auto-reload. Timer 5 can be clocked by SYSCLK, SYSCLK divided by 12, or the external oscillator clock source divided by 8. As the 16-bit timer register increments and overflows from 0xFFFF to 0x0000, the 16-bit value in the Timer 5 reload registers (TMR5RLH and TMR5RLL) is loaded into the Timer 5 register as shown in Figure 26.14, and the Timer 5 High Byte Overflow Flag (TMR5CN.7) is set. If Timer 5 interrupts are enabled (if EIE1.7 is set), an interrupt will be generated on each Timer 5 overflow. Additionally, if Timer 5 interrupts are enabled and the TF5LEN bit is set (TMR5CN.5), an interrupt will be generated each time the lower 8 bits (TMR5L) overflow from 0xFF to 0x00.

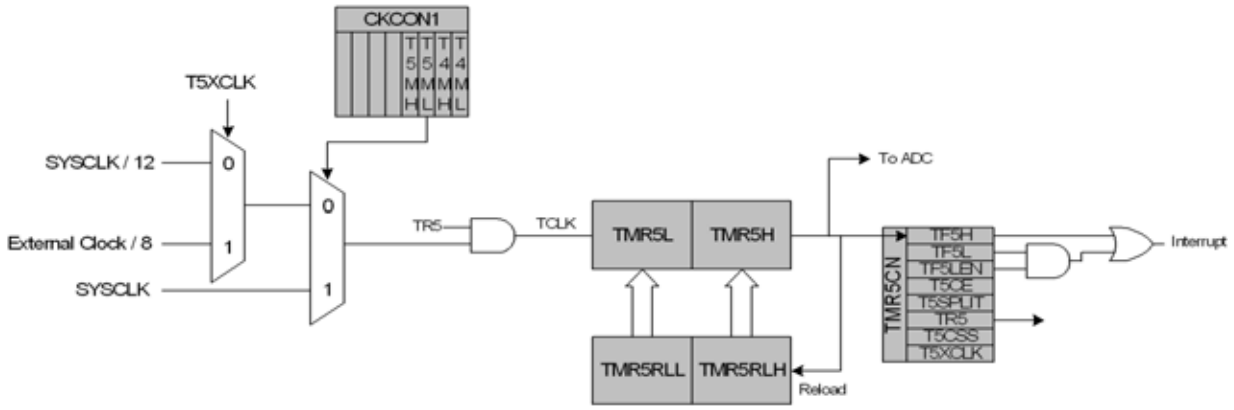

Figure 26.14. Timer 5 16-Bit Mode Block Diagram