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### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	HC08
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	LED, LVD, POR, PWM
Number of I/O	15
Program Memory Size	1.5KB (1.5K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.3V
Data Converters	A/D 12x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	20-DIP
Purchase URL	<a href="https://www.e-xfl.com/product-detail/nxp-semiconductors/mc68hc908jk1cp">https://www.e-xfl.com/product-detail/nxp-semiconductors/mc68hc908jk1cp</a>

## 4.7 FLASH Program Operation

Programming of the FLASH memory is done on a row basis. A row consists of 32 consecutive bytes starting from addresses \$XX00, \$XX20, \$XX40, \$XX60, \$XX80, \$XXA0, \$XXC0 or \$XXE0. Use this step-by-step procedure to program a row of FLASH memory: (Figure 4-2 shows a flowchart of the programming algorithm.)

**NOTE:** *In order to avoid program disturbs, the row must be erased before any byte on that row is programmed.*

1. Set the PGM bit. This configures the memory for program operation and enables the latching of address and data for programming.
2. Write any data to any FLASH location within the address range of the row to be programmed.
3. Wait for a time,  $t_{nvs}$  (10 $\mu$ s).
4. Set the HVEN bit.
5. Wait for a time,  $t_{pgs}$  (5 $\mu$ s).
6. Write data to the byte being programmed.
7. Wait for time,  $t_{prog}$  (30 $\mu$ s).
8. Repeat step 6 and 7 until all the bytes within the row are programmed.
9. Clear the PGM bit.
10. Wait for time,  $t_{nvh}$  (5 $\mu$ s).
11. Clear the HVEN bit.
12. After time,  $t_{rcv}$  (1 $\mu$ s), the memory can be accessed in read mode again.

This program sequence is repeated throughout the memory until all data is programmed.

Table 6-2. Opcode Map

MSB LSB	Bit Manipulation		Branch	Read-Modify-Write						Control		Register/Memory							
	DIR	DIR	REL	DIR	INH	INH	IX1	SP1	IX	INH	INH	IMM	DIR	EXT	IX2	SP2	IX1	SP1	IX
	0	1	2	3	4	5	6	9E6	7	8	9	A	B	C	D	9ED	E	9EE	F
0	BRSET0 3 DIR	BSET0 2 DIR	BRA 2 REL	NEG 2 DIR	NEGA 1 INH	NEGX 1 INH	NEG 2 IX1	NEG 3 SP1	NEG 1 IX	RTI 1 INH	BGE 2 REL	SUB 2 IMM	SUB 2 DIR	SUB 3 EXT	SUB 3 IX2	SUB 4 SP2	SUB 2 IX1	SUB 3 SP1	SUB 1 IX
1	BRCLR0 3 DIR	BCLR0 2 DIR	BRN 2 REL	CBEQ 3 DIR	CBEQA 3 IMM	CBEQX 3 IMM	CBEQ 3 IX1+	CBEQ 4 SP1	CBEQ 2 IX+	RTS 1 INH	BLT 2 REL	CMP 2 IMM	CMP 2 DIR	CMP 3 EXT	CMP 3 IX2	CMP 4 SP2	CMP 2 IX1	CMP 3 SP1	CMP 1 IX
2	BRSET1 3 DIR	BSET1 2 DIR	BHI 2 REL		MUL 1 INH	DIV 1 INH	NSA 1 INH		DAA 1 INH		BGT 2 REL	SBC 2 IMM	SBC 2 DIR	SBC 3 EXT	SBC 3 IX2	SBC 4 SP2	SBC 2 IX1	SBC 3 SP1	SBC 1 IX
3	BRCLR1 3 DIR	BCLR1 2 DIR	BLS 2 REL	COM 2 DIR	COMA 1 INH	COMX 1 INH	COM 2 IX1	COM 3 SP1	COM 1 IX	SWI 1 INH	BLE 2 REL	CPX 2 IMM	CPX 2 DIR	CPX 3 EXT	CPX 3 IX2	CPX 4 SP2	CPX 2 IX1	CPX 3 SP1	CPX 1 IX
4	BRSET2 3 DIR	BSET2 2 DIR	BCC 2 REL	LSR 2 DIR	LSRA 1 INH	LSRX 1 INH	LSR 2 IX1	LSR 3 SP1	LSR 1 IX	TAP 1 INH	TXS 1 INH	AND 2 IMM	AND 2 DIR	AND 3 EXT	AND 3 IX2	AND 4 SP2	AND 2 IX1	AND 3 SP1	AND 1 IX
5	BRCLR2 3 DIR	BCLR2 2 DIR	BCS 2 REL	STHX 2 DIR	LDHX 3 IMM	LDHX 2 DIR	CPHX 3 IMM		CPHX 2 DIR	TPA 1 INH	TSX 1 INH	BIT 2 IMM	BIT 2 DIR	BIT 3 EXT	BIT 3 IX2	BIT 4 SP2	BIT 2 IX1	BIT 3 SP1	BIT 1 IX
6	BRSET3 3 DIR	BSET3 2 DIR	BNE 2 REL	ROR 2 DIR	RORA 1 INH	RORX 1 INH	ROR 2 IX1	ROR 5 SP1	ROR 1 IX	PULA 1 INH		LDA 2 IMM	LDA 2 DIR	LDA 3 EXT	LDA 3 IX2	LDA 4 SP2	LDA 2 IX1	LDA 3 SP1	LDA 1 IX
7	BRCLR3 3 DIR	BCLR3 2 DIR	BEQ 2 REL	ASR 2 DIR	ASRA 1 INH	ASRX 1 INH	ASR 2 IX1	ASR 3 SP1	ASR 1 IX	PSHA 1 INH	TAX 1 INH	AIS 2 IMM	STA 2 DIR	STA 3 EXT	STA 3 IX2	STA 4 SP2	STA 2 IX1	STA 3 SP1	STA 1 IX
8	BRSET4 3 DIR	BSET4 2 DIR	BHCC 2 REL	LSL 2 DIR	LSLA 1 INH	LSLX 1 INH	LSL 2 IX1	LSL 3 SP1	LSL 1 IX	PULX 1 INH	CLC 1 INH	EOR 2 IMM	EOR 2 DIR	EOR 3 EXT	EOR 3 IX2	EOR 4 SP2	EOR 2 IX1	EOR 3 SP1	EOR 1 IX
9	BRCLR4 3 DIR	BCLR4 2 DIR	BHCS 2 REL	ROL 2 DIR	ROLA 1 INH	ROLX 1 INH	ROL 2 IX1	ROL 3 SP1	ROL 1 IX	PSHX 1 INH	SEC 1 INH	ADC 2 IMM	ADC 2 DIR	ADC 3 EXT	ADC 3 IX2	ADC 4 SP2	ADC 2 IX1	ADC 3 SP1	ADC 1 IX
A	BRSET5 3 DIR	BSET5 2 DIR	BPL 2 REL	DEC 2 DIR	DECA 1 INH	DECX 1 INH	DEC 2 IX1	DEC 3 SP1	DEC 1 IX	PULH 1 INH	CLI 1 INH	ORA 2 IMM	ORA 2 DIR	ORA 3 EXT	ORA 3 IX2	ORA 4 SP2	ORA 2 IX1	ORA 3 SP1	ORA 1 IX
B	BRCLR5 3 DIR	BCLR5 2 DIR	BMI 2 REL	DBNZ 3 DIR	DBNZA 2 INH	DBNZX 2 INH	DBNZ 3 IX1	DBNZ 6 SP1	DBNZ 2 IX	PSHH 1 INH	SEI 1 INH	ADD 2 IMM	ADD 2 DIR	ADD 3 EXT	ADD 3 IX2	ADD 4 SP2	ADD 2 IX1	ADD 3 SP1	ADD 1 IX
C	BRSET6 3 DIR	BSET6 2 DIR	BMC 2 REL	INC 2 DIR	INCA 1 INH	INCX 1 INH	INC 2 IX1	INC 3 SP1	INC 1 IX	CLRH 1 INH	RSP 1 INH		JMP 2 DIR	JMP 3 EXT	JMP 3 IX2		JMP 2 IX1		JMP 1 IX
D	BRCLR6 3 DIR	BCLR6 2 DIR	BMS 2 REL	TST 2 DIR	TSTA 1 INH	TSTX 1 INH	TST 2 IX1	TST 3 SP1	TST 1 IX		NOP 1 INH	BSR 2 REL	JSR 2 DIR	JSR 3 EXT	JSR 3 IX2		JSR 2 IX1		JSR 1 IX
E	BRSET7 3 DIR	BSET7 2 DIR	BIL 2 REL		MOV 3 DD	MOV 2 DIX+	MOV 3 IMD		MOV 2 IX+D	STOP 1 INH	*	LDX 2 IMM	LDX 2 DIR	LDX 3 EXT	LDX 3 IX2	LDX 4 SP2	LDX 2 IX1	LDX 3 SP1	LDX 1 IX
F	BRCLR7 3 DIR	BCLR7 2 DIR	BIH 2 REL	CLR 2 DIR	CLRA 1 INH	CLR 1 INH	CLR 2 IX1	CLR 3 SP1	CLR 1 IX	WAIT 1 INH	TXA 1 INH	AIX 2 IMM	STX 2 DIR	STX 3 EXT	STX 3 IX2	STX 4 SP2	STX 2 IX1	STX 3 SP1	STX 1 IX

INH Inherent  
IMM Immediate  
DIR Direct  
EXT Extended  
DD Direct-Direct  
IX+D Indexed-Direct

REL Relative  
IX Indexed, No Offset  
IX1 Indexed, 8-Bit Offset  
IX2 Indexed, 16-Bit Offset  
IMD Immediate-Direct  
DIX+ Direct-Indexed

SP1 Stack Pointer, 8-Bit Offset  
SP2 Stack Pointer, 16-Bit Offset  
IX+ Indexed, No Offset with Post Increment  
IX1+ Indexed, 1-Byte Offset with Post Increment

\*Pre-byte for stack pointer indexed instructions

Low Byte of Opcode in Hexadecimal

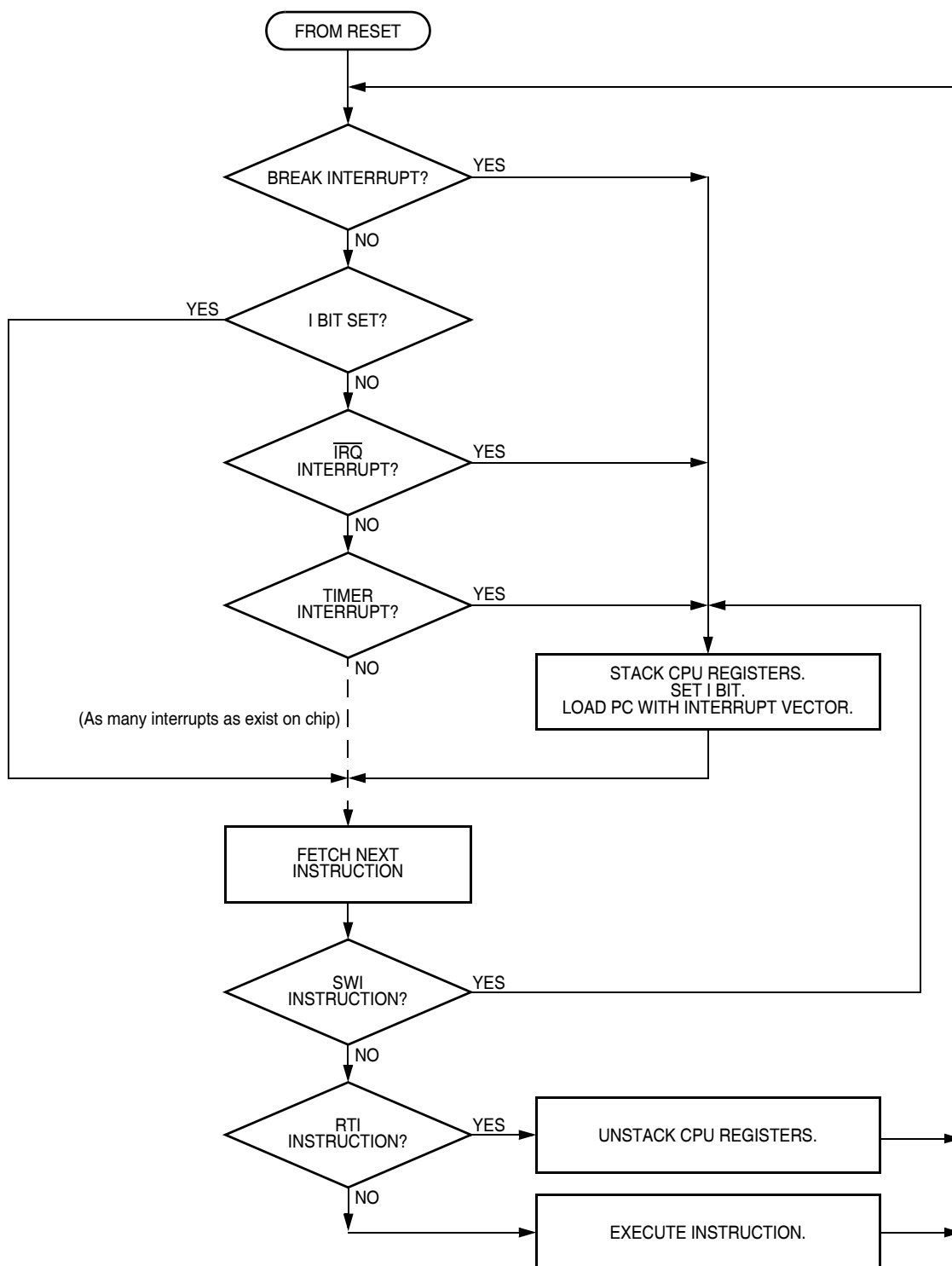
MSB LSB	0	High Byte of Opcode in Hexadecimal
0	5 BRSET0 3 DIR	Cycles Opcode Mnemonic Number of Bytes / Addressing Mode

7.7	Low-Power Modes .....	88
7.7.1	Wait Mode .....	88
7.7.2	Stop Mode .....	90
7.8	SIM Registers .....	91
7.8.1	Break Status Register (BSR) .....	91
7.8.2	Reset Status Register (RSR) .....	92
7.8.3	Break Flag Control Register (BFCR) .....	94

## 7.2 Introduction

This section describes the system integration module (SIM), which supports up to 24 external and/or internal interrupts. Together with the CPU, the SIM controls all MCU activities. A block diagram of the SIM is shown in [Figure 7-1](#). [Figure 7-2](#) is a summary of the SIM I/O registers. The SIM is a system state controller that coordinates CPU and exception timing. The SIM is responsible for:

- Bus clock generation and control for CPU and peripherals
  - Stop/wait/reset/break entry and recovery
  - Internal clock control
- Master reset control, including power-on reset (POR) and COP timeout
- Interrupt control:
  - Acknowledge timing
  - Arbitration control timing
  - Vector address generation
- CPU enable/disable timing
- Modular architecture expandable to 128 interrupt sources



**Figure 7-8. Interrupt Processing**

## Section 8. Oscillator (OSC)

### 8.1 Contents

8.2	Introduction . . . . .	95
8.3	X-tal Oscillator (MC68HC908xxx) . . . . .	96
8.4	RC Oscillator (MC68HRC908xxx) . . . . .	97
8.5	I/O Signals . . . . .	98
8.5.1	Crystal Amplifier Input Pin (OSC1) . . . . .	98
8.5.2	Crystal Amplifier Output Pin (OSC2/PTA6/RCCLK) . . . . .	98
8.5.3	Oscillator Enable Signal (SIMOSCEN) . . . . .	98
8.5.4	X-tal Oscillator Clock (XTALCLK) . . . . .	98
8.5.5	RC Oscillator Clock (RCCLK) . . . . .	99
8.5.6	Oscillator Out 2 (2OSCOUT) . . . . .	99
8.5.7	Oscillator Out (OSCOUT) . . . . .	99
8.6	Low Power Modes . . . . .	99
8.6.1	Wait Mode . . . . .	99
8.6.2	Stop Mode . . . . .	99
8.7	Oscillator During Break Mode . . . . .	100

### 8.2 Introduction

The oscillator module provides the reference clock for the MCU system and bus. Two types of oscillator modules are available:

- MC68HC908xxx— built-in oscillator module (X-tal oscillator) that requires an external crystal or ceramic-resonator. This option also allows an external clock that can be driven directly into OSC1.
- MC68HRC908xxx — built-in oscillator module (RC oscillator) that requires an external RC connection only.

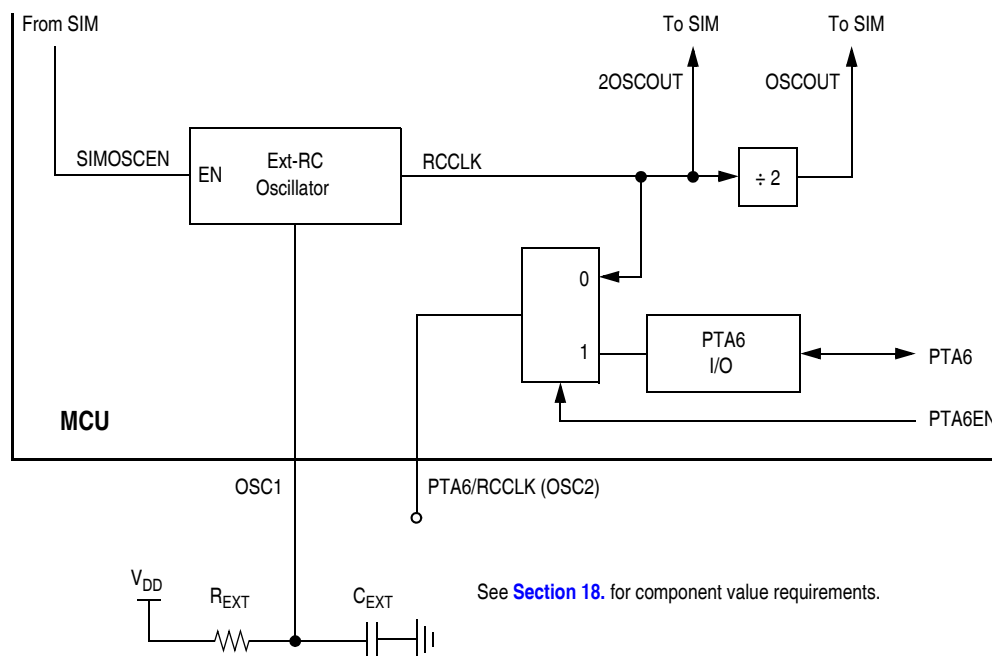
The series resistor ( $R_S$ ) is included in the diagram to follow strict Pierce oscillator guidelines and may not be required for all ranges of operation, especially with high frequency crystals. Refer to the crystal manufacturer's data for more information.

## 8.4 RC Oscillator (MC68HRC908xxx)

The RC oscillator circuit is designed for use with external R and C to provide a clock source with tolerance less than 10%.

In its typical configuration, the RC oscillator requires two external components, one R and one C. Component values should have a tolerance of 1% or less, to obtain a clock source with less than 10% tolerance. The oscillator configuration uses two components:

- $C_{EXT}$
- $R_{EXT}$

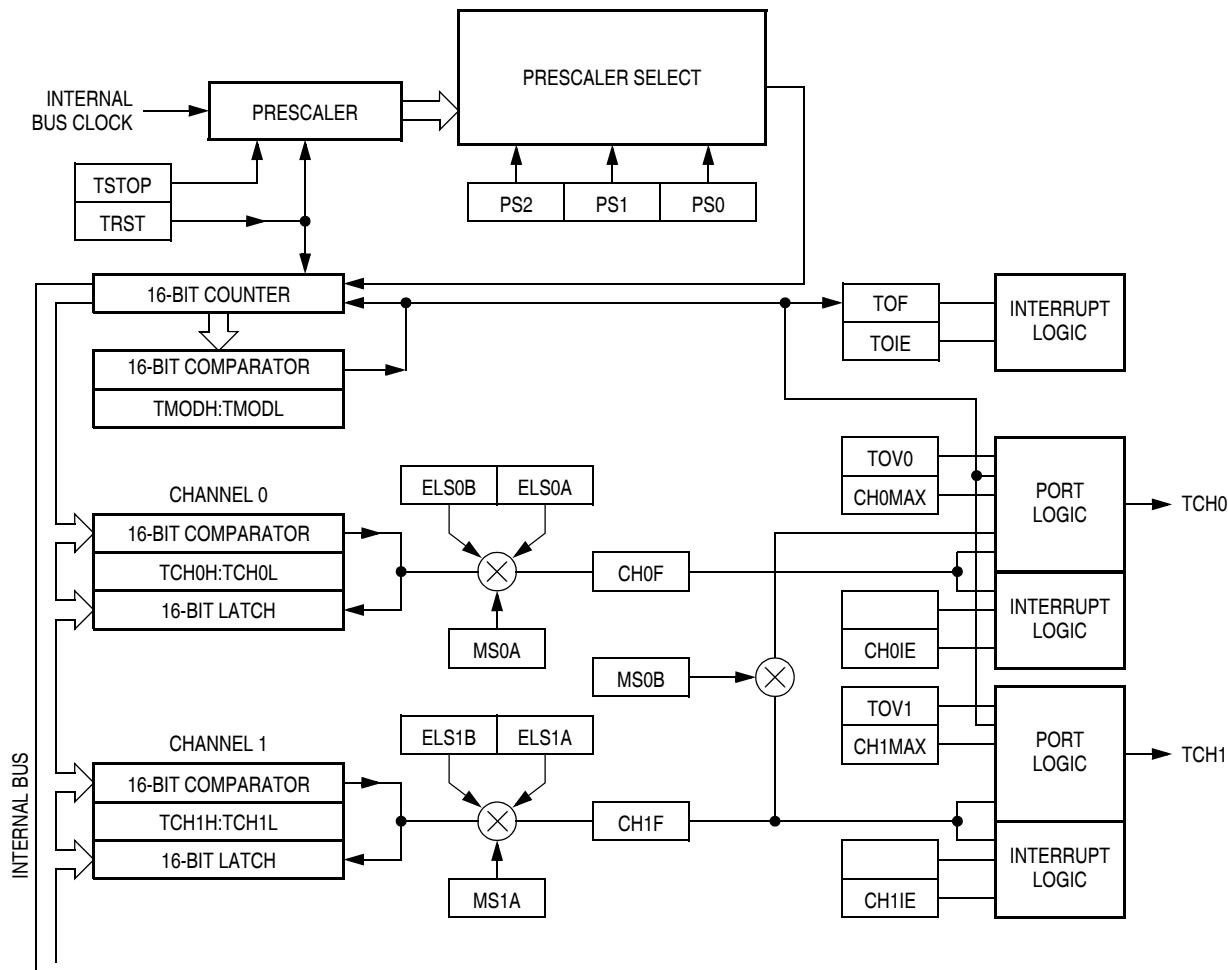


**Figure 8-2. RC Oscillator External Connections**

# 10.5 Functional Description

**Figure 10-1** shows the structure of the TIM. The central component of the TIM is the 16-bit TIM counter that can operate as a free-running counter or a modulo up-counter. The TIM counter provides the timing reference for the input capture and output compare functions. The TIM counter modulo registers, TMODH:TMODL, control the modulo value of the TIM counter. Software can read the TIM counter value at any time without affecting the counting sequence.

The two TIM channels are programmable independently as input capture or output compare channels.



**Figure 10-1. TIM Block Diagram**



## 10.5.3.1 Unbuffered Output Compare

Any output compare channel can generate unbuffered output compare pulses as described in [10.5.3 Output Compare](#). The pulses are unbuffered because changing the output compare value requires writing the new value over the old value currently in the TIM channel registers.

An unsynchronized write to the TIM channel registers to change an output compare value could cause incorrect operation for up to two counter overflow periods. For example, writing a new value before the counter reaches the old value but after the counter reaches the new value prevents any compare during that counter overflow period. Also, using a TIM overflow interrupt routine to write a new, smaller output compare value may cause the compare to be missed. The TIM may pass the new value before it is written.

Use the following methods to synchronize unbuffered changes in the output compare value on channel x:

- When changing to a smaller value, enable channel x output compare interrupts and write the new value in the output compare interrupt routine. The output compare interrupt occurs at the end of the current output compare pulse. The interrupt routine has until the end of the counter overflow period to write the new value.
- When changing to a larger output compare value, enable channel x TIM overflow interrupts and write the new value in the TIM overflow interrupt routine. The TIM overflow interrupt occurs at the end of the current counter overflow period. Writing a larger value in an output compare interrupt routine (at the end of the current pulse) could cause two output compares to occur in the same counter overflow period.

## 10.5.3.2 Buffered Output Compare

Channels 0 and 1 can be linked to form a buffered output compare channel whose output appears on the TCH0 pin. The TIM channel registers of the linked pair alternately control the output.

Setting the MS0B bit in TIM channel 0 status and control register (TSC0) links channel 0 and channel 1. The output compare value in the TIM

**Table 10-2. Prescaler Selection**

PS2	PS1	PS0	TIM Clock Source
0	0	0	Internal Bus Clock ÷ 1
0	0	1	Internal Bus Clock ÷ 2
0	1	0	Internal Bus Clock ÷ 4
0	1	1	Internal Bus Clock ÷ 8
1	0	0	Internal Bus Clock ÷ 16
1	0	1	Internal Bus Clock ÷ 32
1	1	0	Internal Bus Clock ÷ 64
1	1	1	Not available

### 10.10.2 TIM Counter Registers (TCNTH:TCNTL)

The two read-only TIM counter registers contain the high and low bytes of the value in the TIM counter. Reading the high byte (TCNTH) latches the contents of the low byte (TCNTL) into a buffer. Subsequent reads of TCNTH do not affect the latched TCNTL value until TCNTL is read. Reset clears the TIM counter registers. Setting the TIM reset bit (TRST) also clears the TIM counter registers.

**NOTE:** *If you read TCNTH during a break interrupt, be sure to unlatch TCNTL by reading TCNTL before exiting the break interrupt. Otherwise, TCNTL retains the value latched during the break.*

## Section 11. Analog-to-Digital Converter (ADC)

### 11.1 Contents

11.2	Introduction	137
11.3	Features	138
11.4	Functional Description	138
11.4.1	ADC Port I/O Pins	139
11.4.2	Voltage Conversion	140
11.4.3	Conversion Time	140
11.4.4	Continuous Conversion	140
11.4.5	Accuracy and Precision	141
11.5	Interrupts	141
11.6	Low-Power Modes	141
11.6.1	Wait Mode	141
11.6.2	Stop Mode	141
11.7	I/O Signals	141
11.7.1	ADC Voltage In (ADCVIN)	142
11.8	I/O Registers	142
11.8.1	ADC Status and Control Register	142
11.8.2	ADC Data Register	144
11.8.3	ADC Input Clock Register	145

### 11.2 Introduction

This section describes the analog-to-digital converter (ADC). The ADC is an 8-bit, 12-channels analog-to-digital converter.

**Table 11-1. MUX Channel Select**

CH4	CH3	CH2	CH1	CH0	ADC Channel	Input Select
0	0	0	0	0	ADC0	PTB0
0	0	0	0	1	ADC1	PTB1
0	0	0	1	0	ADC2	PTB2
0	0	0	1	1	ADC3	PTB3
0	0	1	0	0	ADC4	PTB4
0	0	1	0	1	ADC5	PTB5
0	0	1	1	0	ADC6	PTB6
0	0	1	1	1	ADC7	PTB7
0	1	0	0	0	ADC8	PTD3
0	1	0	0	1	ADC9	PTD2
0	1	0	1	0	ADC10	PTD1
0	1	0	1	1	ADC11	PTD0
0	1	1	0	0	—	Unused (see Note 1)
:	:	:	:	:		
1	1	0	1	0	—	Reserved
1	1	0	1	1		
1	1	1	0	0	—	Unused
1	1	1	0	1		V <sub>DDA</sub> (see Note 2)
1	1	1	1	0		V <sub>SSA</sub> (see Note 2)
1	1	1	1	1		ADC power off

**NOTES:**

1. If any unused channels are selected, the resulting ADC conversion will be unknown.
2. The voltage levels supplied from internal reference nodes as specified in the table are used to verify the operation of the ADC converter both in production test and for user applications.

## 11.8.2 ADC Data Register

One 8-bit result register is provided. This register is updated each time an ADC conversion completes.

## Section 13. External Interrupt (IRQ)

### 13.1 Contents

- 13.2 Introduction .....159
- 13.3 Features .....159
- 13.4 Functional Description .....160
  - 13.4.1  $\overline{\text{IRQ1}}$  Pin.....161
- 13.5 IRQ Module During Break Interrupts .....163
- 13.6 IRQ Status and Control Register (ISCR) .....163

### 13.2 Introduction

The IRQ (external interrupt) module provides a maskable interrupt input.

### 13.3 Features

Features of the IRQ module include the following:

- A dedicated external interrupt pin,  $\overline{\text{IRQ1}}$
- IRQ1 interrupt control bits
- Hysteresis buffer
- Programmable edge-only or edge and level interrupt sensitivity
- Automatic interrupt acknowledge
- Selectable internal pullup resistor

### 13.5 IRQ Module During Break Interrupts

The system integration module (SIM) controls whether the IRQ1 latch can be cleared during the break state. The BCFE bit in the break flag control register (BFCR) enables software to clear the latches during the break state. (See [Section 7. System Integration Module \(SIM\)](#).)

To allow software to clear the IRQ1 latch during a break interrupt, write a logic one to the BCFE bit. If a latch is cleared during the break state, it remains cleared when the MCU exits the break state.

To protect the latches during the break state, write a logic zero to the BCFE bit. With BCFE at logic zero (its default state), writing to the ACK1 bit in the IRQ status and control register during the break state has no effect on the IRQ latch.


### 13.6 IRQ Status and Control Register (ISCR)

The IRQ Status and Control Register (ISCR) controls and monitors operation of the IRQ module. The ISCR has the following functions:

- Shows the state of the IRQ1 flag
- Clears the IRQ1 latch
- Masks IRQ1 and interrupt request
- Controls triggering sensitivity of the  $\overline{\text{IRQ1}}$  interrupt pin

Address: \$001D

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	IRQF1		IMASK1	MODE1
Write:						ACK1		
Reset:	0	0	0	0	0	0	0	0

 = Unimplemented

**Figure 13-3. IRQ Status and Control Register (INTSCR)**

## Section 14. Keyboard Interrupt Module (KBI)

### 14.1 Contents

14.2	Introduction .....	165
14.3	Features .....	165
14.4	Functional Description .....	166
14.4.1	Keyboard Initialization .....	168
14.4.2	Keyboard Status and Control Register .....	169
14.4.3	Keyboard Interrupt Enable Register .....	170
14.5	Wait Mode .....	171
14.6	Stop Mode .....	171
14.7	Keyboard Module During Break Interrupts .....	171

### 14.2 Introduction

The keyboard interrupt module (KBI) provides seven independently maskable external interrupts which are accessible via PTA0–PTA6 pins.

### 14.3 Features

Features of the keyboard interrupt module include the following:

- Seven keyboard interrupt pins with separate keyboard interrupt enable bits and one keyboard interrupt mask
- Software configurable pull-up device if input pin is configured as input port bit
- Programmable edge-only or edge- and level- interrupt sensitivity
- Exit from low-power modes

## Section 16. Low Voltage Inhibit (LVI)

### 16.1 Contents

16.2	Introduction .....	179
16.3	Features .....	179
16.4	Functional Description .....	180
16.5	LVI Control Register (CONFIG2/CONFIG1) .....	180
16.6	Low-Power Modes .....	181
16.6.1	Wait Mode .....	181
16.6.2	Stop Mode .....	181

### 16.2 Introduction

This section describes the low-voltage inhibit module (LVI), which monitors the voltage on the  $V_{DD}$  pin and generates a reset when the  $V_{DD}$  voltage falls to the LVI trip ( $LVI_{TRIP}$ ) voltage.

### 16.3 Features

Features of the LVI module include the following:

- Selectable LVI trip voltage
- Selectable LVI circuit disable



Address: \$001F

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	COPRS	R	R	LVID	R	SSREC	STOP	COPD
Write:								
Reset:	0	0	0	0	0	0	0	0

R = Reserved

**Figure 16-3. Configuration Register 1 (CONFIG1)**

**LVID** —pLow Voltage Inhibit Disable Bit  
 1 = Low voltage inhibit disabled  
 0 = Low voltage inhibit enabled

**LVIT1, LVIT0** — LVI Trip Voltage Selection  
 These two bits determine at which level of  $V_{DD}$  the LVI module will come into action. LVIT1 and LVIT0 are cleared by a Power-On Reset only.

LVIT1	LVIT0	Trip Voltage <sup>(1)</sup>	Comments
0	0	$V_{LVR3}$ (2.4V)	For $V_{DD}$ =3V operation
0	1	$V_{LVR3}$ (2.4V)	For $V_{DD}$ =3V operation
1	0	$V_{LVR5}$ (4.0V)	For $V_{DD}$ =5V operation
1	1	Reserved	

1. See [Section 18. Electrical Specifications](#) for full parameters.

## 16.6 Low-Power Modes

The STOP and WAIT instructions put the MCU in low-power-consumption standby modes.

### 16.6.1 Wait Mode

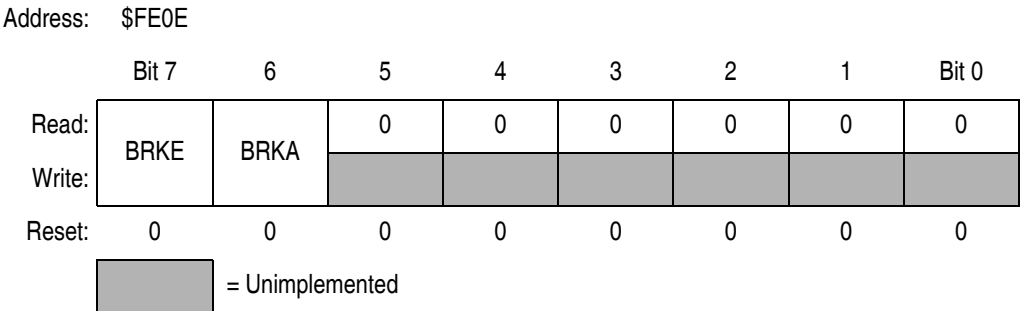
The LVI module, when enabled, will continue to operate in WAIT Mode.

### 16.6.2 Stop Mode

The LVI module, when enabled, will continue to operate in STOP Mode.

### 17.5.1 Break Status and Control Register (BRKSCR)

The break status and control register contains break module enable and status bits.



**Figure 17-3. Break Status and Control Register (BRKSCR)**

#### BRKE — Break Enable Bit

This read/write bit enables breaks on break address register matches. Clear BRKE by writing a logic zero to bit 7. Reset clears the BRKE bit.

- 1 = Breaks enabled on 16-bit address match
- 0 = Breaks disabled

#### BRKA — Break Active Bit

This read/write status and control bit is set when a break address match occurs. Writing a logic one to BRKA generates a break interrupt. Clear BRKA by writing a logic zero to it before exiting the break routine. Reset clears the BRKA bit.

- 1 = Break address match
- 0 = No break address match

## 18.3 Absolute Maximum Ratings

Maximum ratings are the extreme limits to which the MCU can be exposed without permanently damaging it.

**NOTE:** *This device is not guaranteed to operate properly at the maximum ratings. Refer to Sections 18.6 and 18.9 for guaranteed operating conditions.*

**Table 18-1. Absolute Maximum Ratings<sup>(1)</sup>**

Characteristic	Symbol	Value	Unit
Supply voltage	$V_{DD}$	−0.3 to +6.0	V
Input voltage	$V_{IN}$	$V_{SS} - 0.3$ to $V_{DD} + 0.3$	V
Mode entry voltage, $\overline{IRQ1}$ pin	$V_{DD} + V_{HI}$	$V_{SS} - 0.3$ to +8.5	V
Maximum current per pin excluding $V_{DD}$ and $V_{SS}$	I	±25	mA
Storage temperature	$T_{STG}$	−55 to +150	°C
Maximum current out of $V_{SS}$	$I_{MVSS}$	100	mA
Maximum current into $V_{DD}$	$I_{MVDD}$	100	mA

NOTE:

1. Voltages referenced to  $V_{SS}$ .

**NOTE:** *This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. For proper operation, it is recommended that  $V_{IN}$  and  $V_{OUT}$  be constrained to the range  $V_{SS} \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{DD}$ . Reliability of operation is enhanced if unused inputs are connected to an appropriate logic voltage level (for example, either  $V_{SS}$  or  $V_{DD}$ .)*

## 18.14 Memory Characteristics

**Table 18-11. Memory Characteristics**

Characteristic	Symbol	Min	Max	Unit
RAM data retention voltage	$V_{RDR}$	1.3	—	V
FLASH program bus clock frequency	—	1	—	MHz
FLASH read bus clock frequency	$f_{Read}^{(1)}$	32k	8M	Hz
FLASH page erase time	$t_{Erase}^{(2)}$	1	—	ms
FLASH mass erase time	$t_{MErase}^{(3)}$	4	—	ms
FLASH PGM/ERASE to HVEN set up time	$t_{nvs}$	10	—	$\mu s$
FLASH high-voltage hold time	$t_{nvh}$	5	—	$\mu s$
FLASH high-voltage hold time (mass erase)	$t_{nvhl}$	100	—	$\mu s$
FLASH program hold time	$t_{pgs}$	5	—	$\mu s$
FLASH program time	$t_{PROG}$	30	40	$\mu s$
FLASH return to read time	$t_{rcv}^{(4)}$	1	—	$\mu s$
FLASH cumulative program hv period	$t_{HV}^{(5)}$	—	4	ms
FLASH row erase endurance <sup>(6)</sup>	—	10k	—	cycles
FLASH row program endurance <sup>(7)</sup>	—	10k	—	cycles
FLASH data retention time <sup>(8)</sup>	—	10	—	years

**NOTES:**

- $f_{Read}$  is defined as the frequency range for which the FLASH memory can be read.
- If the page erase time is longer than  $t_{Erase}$  (Min), there is no erase-disturb, but it reduces the endurance of the FLASH memory.
- If the mass erase time is longer than  $t_{MErase}$  (Min), there is no erase-disturb, but it reduces the endurance of the FLASH memory.
- $t_{rcv}$  is defined as the time it needs before the FLASH can be read after turning off the high voltage charge pump, by clearing HVEN to logic 0.
- $t_{HV}$  is defined as the cumulative high voltage programming time to the same row before next erase.  
 $t_{HV}$  must satisfy this condition:  $t_{nvs} + t_{nvh} + t_{pgs} + (t_{PROG} \times 32) \leq t_{HV} \text{ max.}$
- The minimum row endurance value specifies each row of the FLASH memory is guaranteed to work for at least this many erase / program cycles.
- The minimum row endurance value specifies each row of the FLASH memory is guaranteed to work for at least this many erase / program cycles.
- The FLASH is guaranteed to retain data over the entire operating temperature range for at least the minimum time specified.



## Section 20. Ordering Information

### 20.1 Contents

20.2 Introduction .....207

20.3 MC Order Numbers .....208

### 20.2 Introduction

This section contains ordering numbers for the MC68H(R)C908JL3, MC68H(R)C908JK3, and MC68H(R)C908JK1.