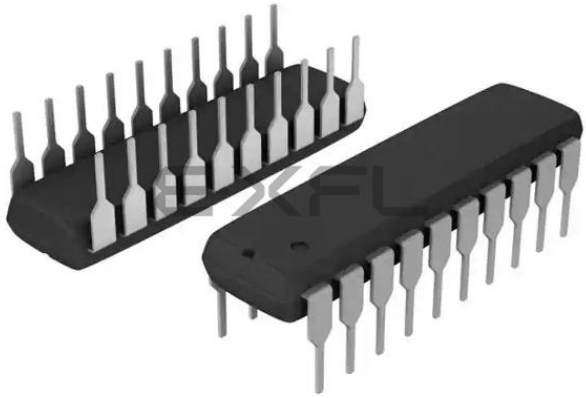

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC08
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	LED, LVD, POR, PWM
Number of I/O	15
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.3V
Data Converters	A/D 12x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	20-DIP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc68hc908jk3cp

List of Sections

Section 10. Timer Interface Module (TIM)

Section 19. Mechanical Specifications

Section 20. Ordering Information

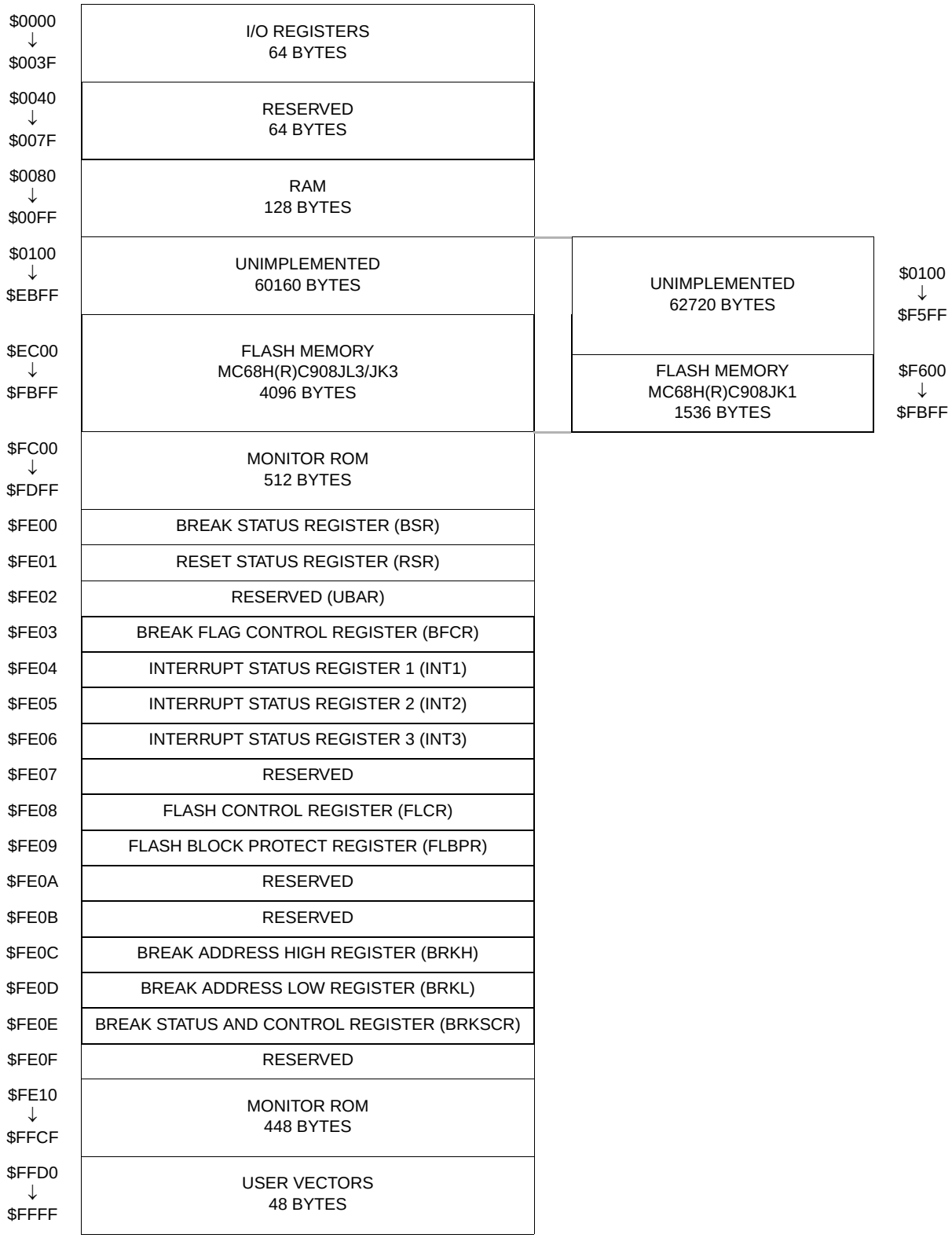

Figure 2-1. Memory Map

Table 2-1. Vector Addresses

Vector Priority	Vector	Address	Vector
Lowest	IF15	$FFDE	ADC Conversion Complete Vector (High)
		$FFDF	ADC Conversion Complete Vector (Low)
	IF14	$FFE0	Keyboard Vector (High)
		$FFE1	Keyboard Vector (Low)
	IF13 to IF6	—	Not Used
	IF5	$FFF2	TIM Overflow Vector (High)
		$FFF3	TIM Overflow Vector (Low)
	IF4	$FFF4	TIM Channel 1 Vector (High)
		$FFF5	TIM Channel 1 Vector (Low)
	IF3	$FFF6	TIM Channel 0 Vector (High)
		$FFF7	TIM Channel 0 Vector (Low)
	IF2	—	Not Used
	IF1	$FFFA	$\overline{\text{IRQ}}$ Vector (High)
		$FFFB	$\overline{\text{IRQ}}$ Vector (Low)
	—	$FFFC	SWI Vector (High)
		$FFFD	SWI Vector (Low)
	—	$FFFE	Reset Vector (High)
Highest		$FFFF	Reset Vector (Low)

4.7 FLASH Program Operation

Programming of the FLASH memory is done on a row basis. A row consists of 32 consecutive bytes starting from addresses $XX00, $XX20, $XX40, $XX60, $XX80, $XXA0, $XXC0 or $XXE0. Use this step-by-step procedure to program a row of FLASH memory: (**Figure 4-2** shows a flowchart of the programming algorithm.)

NOTE: *In order to avoid program disturbs, the row must be erased before any byte on that row is programmed.*

1. Set the PGM bit. This configures the memory for program operation and enables the latching of address and data for programming.
2. Write any data to any FLASH location within the address range of the row to be programmed.
3. Wait for a time, t_{nvs} (10μs).
4. Set the HVEN bit.
5. Wait for a time, t_{pgs} (5μs).
6. Write data to the byte being programmed.
7. Wait for time, t_{PROG} (30μs).
8. Repeat step 6 and 7 until all the bytes within the row are programmed.
9. Clear the PGM bit.
10. Wait for time, t_{nvh} (5μs).
11. Clear the HVEN bit.
12. After time, t_{rcv} (1μs), the memory can be accessed in read mode again.

This program sequence is repeated throughout the memory until all data is programmed.

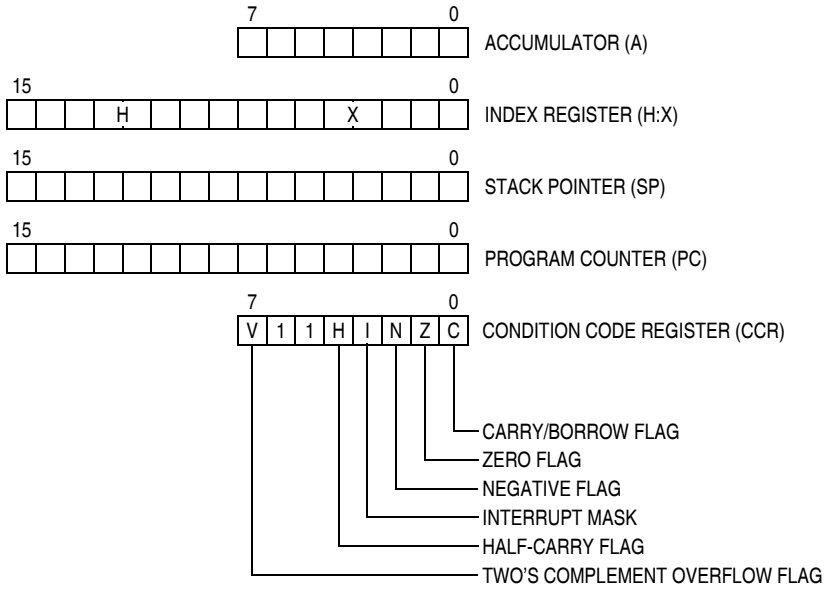

Figure 6-1. CPU Registers

6.4.1 Accumulator

The accumulator is a general-purpose 8-bit register. The CPU uses the accumulator to hold operands and the results of arithmetic/logic operations.

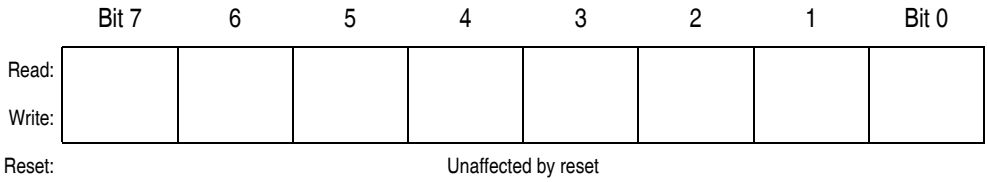

Figure 6-2. Accumulator (A)

6.6.2 Stop Mode

The STOP instruction:

- Clears the interrupt mask (I bit) in the condition code register, enabling external interrupts. After exit from stop mode by external interrupt, the I bit remains clear. After exit by reset, the I bit is set.
- Disables the CPU clock

After exiting stop mode, the CPU clock begins running after the oscillator stabilization delay.

6.7 CPU During Break Interrupts

If a break module is present on the MCU, the CPU starts a break interrupt by:

- Loading the instruction register with the SWI instruction
- Loading the program counter with $FFFC:$FFFD or with $FEFC:$FEFD in monitor mode

The break interrupt begins after completion of the CPU instruction in progress. If the break address register match occurs on the last cycle of a CPU instruction, the break interrupt begins immediately.

A return-from-interrupt instruction (RTI) in the break routine ends the break interrupt and returns the MCU to normal operation if the break interrupt has been deasserted.

6.8 Instruction Set Summary

6.9 Opcode Map

See **Table 6-2**.

7.3 SIM Bus Clock Control and Generation

The bus clock generator provides system clock signals for the CPU and peripherals on the MCU. The system clocks are generated from an incoming clock, OSCOUT, as shown in **Figure 7-3**.

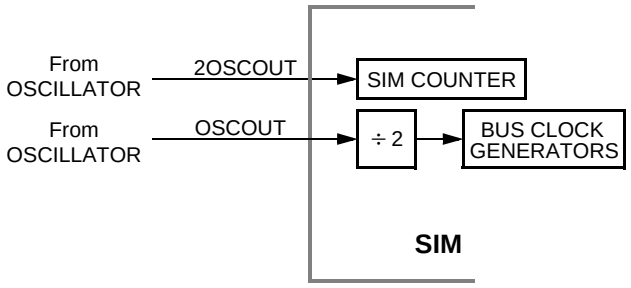

Figure 7-3. SIM Clock Signals

7.3.1 Bus Timing

In user mode**,** the internal bus frequency is the oscillator frequency (2OSCOUT) divided by four.

7.3.2 Clock Start-Up from POR

When the power-on reset module generates a reset, the clocks to the CPU and peripherals are inactive and held in an inactive phase until after the 4096 2OSCOUT cycle POR time-out has completed. The $\overline{\text{RST}}$ pin is driven low by the SIM during this entire period. The IBUS clocks start upon completion of the time-out.

7.3.3 Clocks in Stop Mode and Wait Mode

Upon exit from stop mode by an interrupt, break, or reset, the SIM allows 2OSCOUT to clock the SIM counter. The CPU and peripheral clocks do not become active until after the stop delay time-out. This time-out is selectable as 4096 or 32 2OSCOUT cycles. (See **7.7.2 Stop Mode**.)

The active reset feature allows the part to issue a reset to peripherals and other chips within a system built around the MCU.

7.4.2.1 Power-On Reset

When power is first applied to the MCU, the power-on reset module (POR) generates a pulse to indicate that power-on has occurred. The external reset pin ($\overline{RST}$) is held low while the SIM counter counts out 4096 2OSCOUT cycles. Sixty-four 2OSCOUT cycles later, the CPU and memories are released from reset to allow the reset vector sequence to occur.

At power-on, the following events occur:

- A POR pulse is generated.
- The internal reset signal is asserted.
- The SIM enables the oscillator to drive 2OSCOUT.
- Internal clocks to the CPU and modules are held inactive for 4096 2OSCOUT cycles to allow stabilization of the oscillator.
- The $\overline{RST}$ pin is driven low during the oscillator stabilization time.
- The POR bit of the reset status register (RSR) is set and all other bits in the register are cleared.

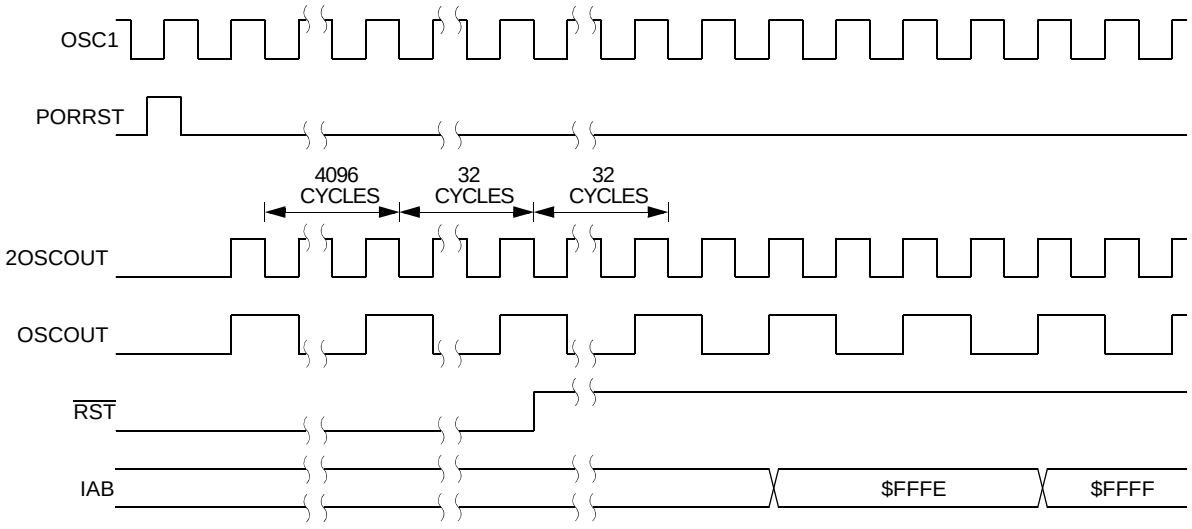

Figure 7-7. POR Recovery

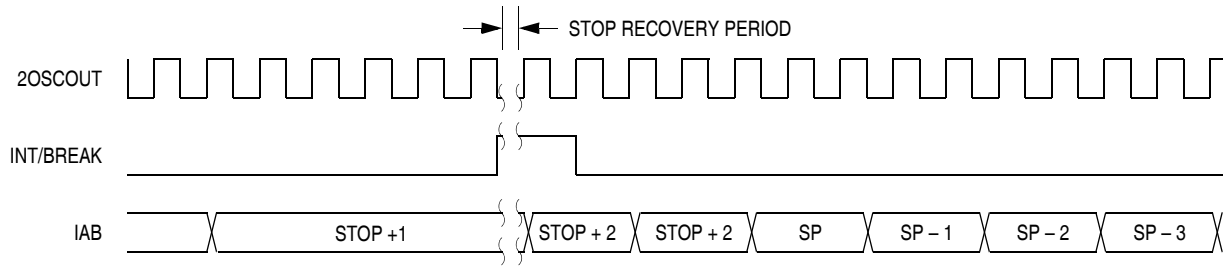

Figure 7-19. Stop Mode Recovery from Interrupt or Break

7.8 SIM Registers

The SIM has three memory mapped registers. **Table 7-4** shows the mapping of these registers.

Table 7-4. SIM Registers

Address	Register	Access Mode
$FE00	BSR	User
$FE01	RSR	User
$FE03	BFCR	User

7.8.1 Break Status Register (BSR)

The break status register contains a flag to indicate that a break caused an exit from stop or wait mode.

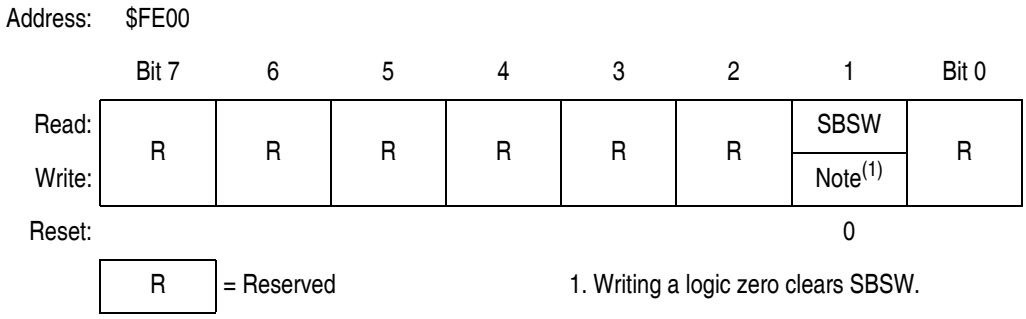

Figure 7-20. Break Status Register (BSR)

9.4.1 Entering Monitor Mode

Table 9-1 shows the pin conditions for entering monitor mode. As specified in the table, monitor mode may be entered after a POR and will allow communication at 9600 baud provided one of the following sets of conditions is met:

1. If $\overline{IRQ1} = V_{DD} + V_{HI}$:
   - External clock on OSC1 is 4.9125 MHz
   - PTB3 = low
2. If $\overline{IRQ1} = V_{DD} + V_{HI}$:
   - External clock on OSC1 is 9.8304 MHz
   - PTB3 = high
3. If $FFFE & $FFFF is blank (contains $FF):
   - The oscillator clock is 9.8304 MHz (X-tal or RC)
   - $\overline{IRQ1} = V_{DD}$

Table 9-1. Monitor Mode Entry Requirements and Options

$\overline{IRQ1}$	$FFFE and $FFFF	PTB3	PTB2	PTB1	PTB0	Clock Source and Frequency	Bus Frequency	Comments
$V_{DD} + V_{HI}$	X	0	0	1	1	OSC1 at 4.9152 MHz	2.4576 MHz	Bypasses X-tal or RC oscillator; external clock driven directly into OSC1. 9600 baud communication on PTB0. COP disabled.
$V_{DD} + V_{HI}$	X	1	0	1	1	OSC1 at 9.8304 MHz	2.4576 MHz	
V_{DD}	BLANK (contain $FF)	X	X	X	1	X-tal or RC oscillator at 9.8304 MHz	2.4576 MHz	Low-voltage entry to monitor mode. 9600 baud communication on PTB0. COP disabled.
V_{DD}	NOT BLANK	X	X	X	X	X-tal or RC oscillator at desired frequency	XTALCLK ÷ 4 or RCCLK ÷ 4	Enters User mode. If $FFFE and $FFFF is blank, MCU will encounter an illegal address reset.

Notes:
1. PTB3 = 0: Bypasses the divide-by-two prescaler to SIM when using $V_{DD} + V_{HI}$ for monitor mode entry. The OSC1 clock must be 50% duty cycle for this condition.
2. XTALCLK is the X-tal oscillator output, for MC68HC908xxx. See Figure 8-1.
4. RCCLK is the RC oscillator output, for MC68HRC908xxx. See Figure 8-2.
5. See Table 18-4 for $V_{DD} + V_{HI}$ voltage level requirements.

10.2 Introduction

This section describes the timer interface module (TIM2, Version B). The TIM is a two-channel timer that provides a timing reference with input capture, output compare, and pulse-width-modulation functions. **Figure 10-1** is a block diagram of the TIM.

10.3 Features

Features of the TIM include the following:

- Two input capture/output compare channels
  - Rising-edge, falling-edge, or any-edge input capture trigger
  - Set, clear, or toggle output compare action
- Buffered and unbuffered pulse width modulation (PWM) signal generation
- Programmable TIM clock input with 7-frequency internal bus clock prescaler selection
- Free-running or modulo up-count operation
- Toggle any channel pin on overflow
- TIM counter stop and reset bits
- Modular architecture expandable to eight channels

10.4 Pin Name Conventions

The TIM share two I/O pins with two port D I/O pins. The full name of the TIM I/O pins are listed in **Table 10-1**. The generic pin name appear in the text that follows.

Table 10-1. Pin Name Conventions

TIM Generic Pin Names:	TCH0	TCH1
Full TIM Pin Names:	PTD4/TCH0	PTD5/TCH1

overflow occurs before the clearing sequence is complete, then writing logic zero to TOF has no effect. Therefore, a TOF interrupt request cannot be lost due to inadvertent clearing of TOF. Reset clears the TOF bit. Writing a logic one to TOF has no effect.

1 = TIM counter has reached modulo value
0 = TIM counter has not reached modulo value

TOIE — TIM Overflow Interrupt Enable Bit

This read/write bit enables TIM overflow interrupts when the TOF bit becomes set. Reset clears the TOIE bit.

1 = TIM overflow interrupts enabled
0 = TIM overflow interrupts disabled

TSTOP — TIM Stop Bit

This read/write bit stops the TIM counter. Counting resumes when TSTOP is cleared. Reset sets the TSTOP bit, stopping the TIM counter until software clears the TSTOP bit.

1 = TIM counter stopped
0 = TIM counter active

NOTE: *Do not set the TSTOP bit before entering wait mode if the TIM is required to exit wait mode.*

TRST — TIM Reset Bit

Setting this write-only bit resets the TIM counter and the TIM prescaler. Setting TRST has no effect on any other registers. Counting resumes from $0000. TRST is cleared automatically after the TIM counter is reset and always reads as logic zero. Reset clears the TRST bit.

1 = Prescaler and TIM counter cleared
0 = No effect

NOTE: *Setting the TSTOP and TRST bits simultaneously stops the TIM counter at a value of $0000.*

PS[2:0] — Prescaler Select Bits

These read/write bits select one of the seven prescaler outputs as the input to the TIM counter as **Table 10-2** shows. Reset clears the PS[2:0] bits.

Section 15. Computer Operating Properly (COP)

15.1 Contents

15.2 Introduction

The computer operating properly (COP) module contains a free-running counter that generates a reset if allowed to overflow. The COP module helps software recover from runaway code. Prevent a COP reset by clearing the COP counter periodically. The COP module can be disabled through the COPD bit in the CONFIG1 register.

17.3 Features

Features of the break module include the following:

- Accessible I/O registers during the break Interrupt
- CPU-generated break interrupts
- Software-generated break interrupts
- COP disabling during break interrupts

17.4 Functional Description

When the internal address bus matches the value written in the break address registers, the break module issues a breakpoint signal ($\overline{\text{BKPT}}$) to the SIM. The SIM then causes the CPU to load the instruction register with a software interrupt instruction (SWI) after completion of the current CPU instruction. The program counter vectors to $FFFC and $FFFD ($FEFC and $FEFD in monitor mode).

The following events can cause a break interrupt to occur:

- A CPU-generated address (the address in the program counter) matches the contents of the break address registers.
- Software writes a logic one to the BRKA bit in the break status and control register.

When a CPU generated address matches the contents of the break address registers, the break interrupt begins after the CPU completes its current instruction. A return from interrupt instruction (RTI) in the break routine ends the break interrupt and returns the MCU to normal operation. **Figure 17-1** shows the structure of the break module.

17.5.1 Break Status and Control Register (BRKSCR)

The break status and control register contains break module enable and status bits.

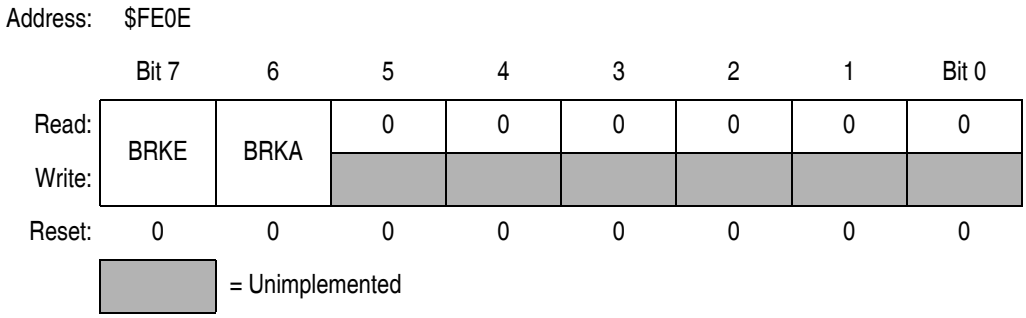

Figure 17-3. Break Status and Control Register (BRKSCR)

BRKE — Break Enable Bit

This read/write bit enables breaks on break address register matches. Clear BRKE by writing a logic zero to bit 7. Reset clears the BRKE bit.

1 = Breaks enabled on 16-bit address match
0 = Breaks disabled

BRKA — Break Active Bit

This read/write status and control bit is set when a break address match occurs. Writing a logic one to BRKA generates a break interrupt. Clear BRKA by writing a logic zero to it before exiting the break routine. Reset clears the BRKA bit.

1 = Break address match
0 = No break address match