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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

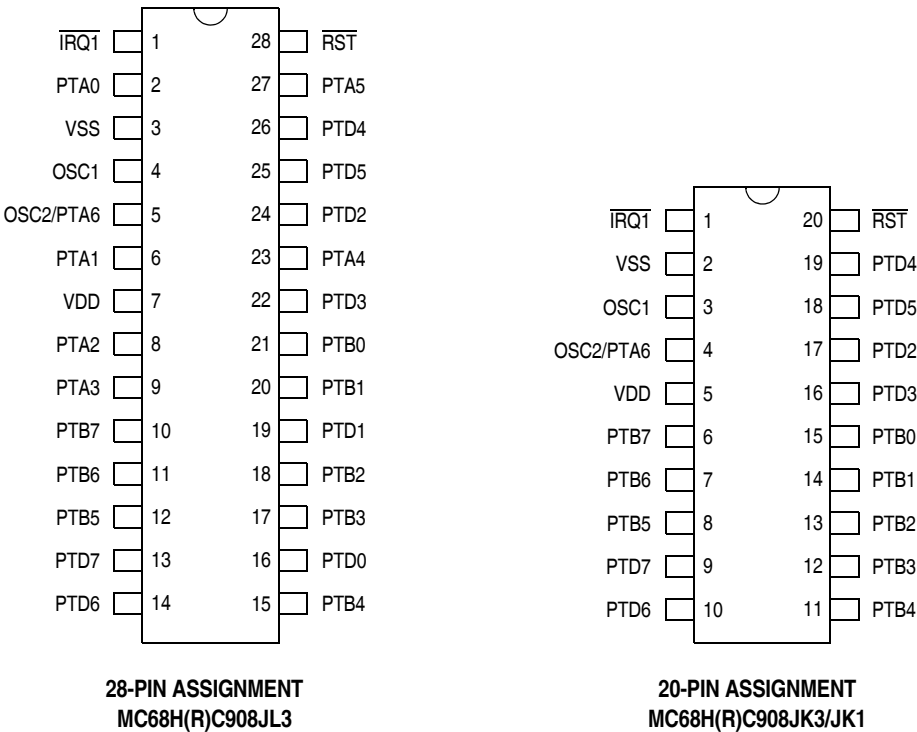
### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	HC08
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	LED, LVD, POR, PWM
Number of I/O	15
Program Memory Size	1.5KB (1.5K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.3V
Data Converters	A/D 12x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOIC
Purchase URL	<a href="https://www.e-xfl.com/product-detail/nxp-semiconductors/mc68hrc908jk1cdw">https://www.e-xfl.com/product-detail/nxp-semiconductors/mc68hrc908jk1cdw</a>

# 1.5 Pin Assignments

The MC68H(R)C908JL3 is available in 28-pin packages and the MC68H(R)C908JK3/JK1 in 20-pin packages. **Figure 1-2** shows the pin assignment for the two packages.



Pins not bonded out on 20-pin package:  
PTA0, PTA1, PTA2, PTA3, PTA4, PTA5,  
PTD0, PTD1.

**Figure 1-2. MCU Pin Assignments**

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
\$002B	Unimplemented	Read:								
\$003B		Write:								
\$003C	ADC Status and Control Register (ADSCR)	Read:	COCO	AIEN	ADCO	CH4	CH3	CH2	CH1	CH0
		Write:								
		Reset:	0	0	0	1	1	1	1	1
\$003D	ADC Data Register (ADR)	Read:	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
		Write:								
		Reset:	Indeterminate after reset							
\$003E	ADC Input Clock Register (ADICLK)	Read:	ADIV2	ADIV1	ADIV0	0	0	0	0	0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
\$003F	Unimplemented	Read:								
		Write:								
\$FE00	Break Status Register (BSR)	Read:	R	R	R	R	R	R	SBSW	R
		Write:							See note	
		Reset:	0							
Note: Writing a logic 0 clears SBSW.										
\$FE01	Reset Status Register (RSR)	Read:	POR	PIN	COP	ILOP	ILAD	MODRST	LVI	0
		Write:								
		POR:	1	0	0	0	0	0	0	0
\$FE02	Reserved	Read:	R	R	R	R	R	R	R	R
		Write:								
\$FE03	Break Flag Control Register (BFCR)	Read:	BCFE	R	R	R	R	R	R	R
		Write:								
		Reset:	0							
\$FE04	Interrupt Status Register 1 (INT1)	Read:	0	IF5	IF4	IF3	0	IF1	0	0
		Write:	R	R	R	R	R	R	R	R
		Reset:	0	0	0	0	0	0	0	0
				= Unimplemented			R	= Reserved		

**Figure 2-2. Control, Status, and Data Registers (Sheet 4 of 5)**

## Section 4. FLASH Memory (FLASH)

### 4.1 Contents

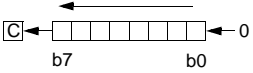
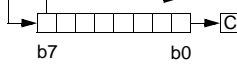
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### 4.2 Introduction

This section describes the operation of the embedded FLASH memory. The FLASH memory can be read, programmed, and erased from a single external supply. The program and erase operations are enabled through the use of an internal charge pump.

- MC68H(R)C908JL3/JK3: 4096 bytes user FLASH from \$EC00 – \$FBFF.
- MC68H(R)C908JK1: 1536 bytes user FLASH from \$F600 – \$FBFF.

## Table 6-1. Instruction Set Summary

Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Cycles
			V	H	I	N	Z	C				
ADC #opr ADC opr ADC opr ADC opr,X ADC opr,X ADC ,X ADC opr,SP ADC opr,SP	Add with Carry	$A \leftarrow (A) + (M) + (C)$	↑	↑	—	↑	↑	↑	IMM DIR EXT IX2 IX1 IX SP1 SP2	A9 B9 C9 D9 E9 F9 9EE9 9ED9	ii dd hh ll ee ff ff ff ff ee ff	2 3 4 4 3 2 4 5
ADD #opr ADD opr ADD opr ADD opr,X ADD opr,X ADD ,X ADD opr,SP ADD opr,SP	Add without Carry	$A \leftarrow (A) + (M)$	↑	↑	—	↑	↑	↑	IMM DIR EXT IX2 IX1 IX SP1 SP2	AB BB CB DB EB FB 9EEB 9EDB	ii dd hh ll ee ff ff ff ff ee ff	2 3 4 4 3 2 4 5
AIS #opr	Add Immediate Value (Signed) to SP	$SP \leftarrow (SP) + (16 \ll M)$	—	—	—	—	—	—	IMM	A7	ii	2
AIX #opr	Add Immediate Value (Signed) to H:X	$H:X \leftarrow (H:X) + (16 \ll M)$	—	—	—	—	—	—	IMM	AF	ii	2
AND #opr AND opr AND opr AND opr,X AND opr,X AND ,X AND opr,SP AND opr,SP	Logical AND	$A \leftarrow (A) \& (M)$	0	—	—	↑	↑	—	IMM DIR EXT IX2 IX1 IX SP1 SP2	A4 B4 C4 D4 E4 F4 9EE4 9ED4	ii dd hh ll ee ff ff ff ff ee ff	2 3 4 4 3 2 4 5
ASL opr ASLA ASLX ASL opr,X ASL ,X ASL opr,SP	Arithmetic Shift Left (Same as LSL)		↑	—	—	↑	↑	↑	DIR INH INH IX1 IX SP1	38 48 58 68 78 9E68	dd ff ff	4 1 1 4 3 5
ASR opr ASRA ASRX ASR opr,X ASR opr,X ASR opr,SP	Arithmetic Shift Right		↑	—	—	↑	↑	↑	DIR INH INH IX1 IX SP1	37 47 57 67 77 9E67	dd ff ff	4 1 1 4 3 5
BCC rel	Branch if Carry Bit Clear	$PC \leftarrow (PC) + 2 + rel \text{ ? } (C) = 0$	—	—	—	—	—	—	REL	24	rr	3
BCLR n, opr	Clear Bit n in M	$M_n \leftarrow 0$	—	—	—	—	—	—	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	11 13 15 17 19 1B 1D 1F	dd dd dd dd dd dd dd dd	4 4 4 4 4 4 4 4

## Table 6-1. Instruction Set Summary

Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Cycles
			V	H	I	N	Z	C				
BRCLR <i>n,opr,rel</i>	Branch if Bit <i>n</i> in M Clear	$PC \leftarrow (PC) + 3 + rel ? (Mn) = 0$							DIR (b0)	01	dd rr	5
									DIR (b1)	03	dd rr	5
									DIR (b2)	05	dd rr	5
									DIR (b3)	07	dd rr	5
									DIR (b4)	09	dd rr	5
									DIR (b5)	0B	dd rr	5
									DIR (b6)	0D	dd rr	5
									DIR (b7)	0F	dd rr	5
BRN <i>rel</i>	Branch Never	$PC \leftarrow (PC) + 2$	-	-	-	-	-	-	REL	21	rr	3
BRSET <i>n,opr,rel</i>	Branch if Bit <i>n</i> in M Set	$PC \leftarrow (PC) + 3 + rel ? (Mn) = 1$							DIR (b0)	00	dd rr	5
									DIR (b1)	02	dd rr	5
									DIR (b2)	04	dd rr	5
									DIR (b3)	06	dd rr	5
									DIR (b4)	08	dd rr	5
									DIR (b5)	0A	dd rr	5
									DIR (b6)	0C	dd rr	5
									DIR (b7)	0E	dd rr	5
BSET <i>n,opr</i>	Set Bit <i>n</i> in M	$Mn \leftarrow 1$							DIR (b0)	10	dd	4
									DIR (b1)	12	dd	4
									DIR (b2)	14	dd	4
									DIR (b3)	16	dd	4
									DIR (b4)	18	dd	4
									DIR (b5)	1A	dd	4
									DIR (b6)	1C	dd	4
									DIR (b7)	1E	dd	4
BSR <i>rel</i>	Branch to Subroutine	$PC \leftarrow (PC) + 2$ ; push (PCL) $SP \leftarrow (SP) - 1$ ; push (PCH) $SP \leftarrow (SP) - 1$ $PC \leftarrow (PC) + rel$	-	-	-	-	-	-	REL	AD	rr	4
CBEQ <i>opr,rel</i> CBEQA # <i>opr,rel</i> CBEQX # <i>opr,rel</i> CBEQ <i>opr,X+,rel</i> CBEQ <i>X+,rel</i> CBEQ <i>opr,SP,rel</i>	Compare and Branch if Equal	$PC \leftarrow (PC) + 3 + rel ? (A) - (M) = \$00$ $PC \leftarrow (PC) + 3 + rel ? (A) - (M) = \$00$ $PC \leftarrow (PC) + 3 + rel ? (X) - (M) = \$00$ $PC \leftarrow (PC) + 3 + rel ? (A) - (M) = \$00$ $PC \leftarrow (PC) + 2 + rel ? (A) - (M) = \$00$ $PC \leftarrow (PC) + 4 + rel ? (A) - (M) = \$00$							DIR IMM IMM IX1+ IX+ SP1	31 41 51 61 71 9E61	dd rr ii rr ii rr ff rr rr ff rr	5 4 4 5 4 6
CLC	Clear Carry Bit	$C \leftarrow 0$	-	-	-	-	-	0	INH	98		1
CLI	Clear Interrupt Mask	$I \leftarrow 0$	-	-	0	-	-	-	INH	9A		2
CLR <i>opr</i> CLRA CLR X CLR H CLR <i>opr,X</i> CLR ,X CLR <i>opr,SP</i>	Clear	$M \leftarrow \$00$ $A \leftarrow \$00$ $X \leftarrow \$00$ $H \leftarrow \$00$ $M \leftarrow \$00$ $M \leftarrow \$00$ $M \leftarrow \$00$	0	-	-	0	1	-	DIR INH INH INH IX1 IX SP1	3F 4F 5F 8C 6F 7F 9E6F	dd   ff ff ff	3 1 1 1 3 2 4



## 7.4.2.5 LVI Reset

The low-voltage inhibit module (LVI) asserts its output to the SIM when the  $V_{DD}$  voltage falls to the LVI trip voltage  $V_{TRIP}$ . The LVI bit in the SIM reset status register (SRSR) is set, and the external reset pin (RSTB) is held low while the SIM counter counts out 4096 2OSCCLK cycles. Sixty-four 2OSCOOUT cycles later, the CPU and memories are released from reset to allow the reset vector sequence to occur. The SIM actively pulls down the (RSTB) pin for all internal reset sources.

## 7.5 SIM Counter

The SIM counter is used by the power-on reset module (POR) and in stop mode recovery to allow the oscillator time to stabilize before enabling the internal bus (IBUS) clocks. The SIM counter also serves as a prescaler for the computer operating properly module (COP). The SIM counter uses 12 stages for counting, followed by a 13th stage that triggers a reset of SIM counters and supplies the clock for the COP module. The SIM counter is clocked by the falling edge of 2OSCOOUT.

### 7.5.1 SIM Counter During Power-On Reset

The power-on reset module (POR) detects power applied to the MCU. At power-on, the POR circuit asserts the signal PORRST. Once the SIM is initialized, it enables the oscillator to drive the bus clock state machine.

### 7.5.2 SIM Counter During Stop Mode Recovery

The SIM counter also is used for stop mode recovery. The STOP instruction clears the SIM counter. After an interrupt, break, or reset, the SIM senses the state of the short stop recovery bit, SSREC, in the mask option register. If the SSREC bit is a logic one, then the stop recovery is reduced from the normal delay of 4096 2OSCOOUT cycles down to 32 2OSCOOUT cycles. This is ideal for applications using canned oscillators that do not require long start-up times from stop mode. External crystal applications should use the full stop recovery time, that is, with SSREC cleared in the configuration register (CONFIG).



### 7.6.2.3 Interrupt Status Register 3

Address: \$FE06

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	0	0	0	IF15
Write:	R	R	R	R	R	R	R	R
Reset:	0	0	0	0	0	0	0	0

R = Reserved

**Figure 7-14. Interrupt Status Register 3 (INT3)**

#### IF15 — Interrupt Flags

These flags indicate the presence of interrupt requests from the sources shown in [Table 7-3](#).

- 1 = Interrupt request present
- 0 = No interrupt request present

Bit 1 to 7 — Always read 0

### 7.6.3 Reset

All reset sources always have equal and highest priority and cannot be arbitrated.

### 7.6.4 Break Interrupts

The break module can stop normal program flow at a software-programmable break point by asserting its break interrupt output. (See [Section 17. Break Module \(BREAK\)](#).) The SIM puts the CPU into the break state by forcing it to the SWI vector location. Refer to the break interrupt subsection of each module to see how each module is affected by the break state.

### 7.6.5 Status Flag Protection in Break Mode

The SIM controls whether status flags contained in other modules can be cleared during break mode. The user can select whether flags are

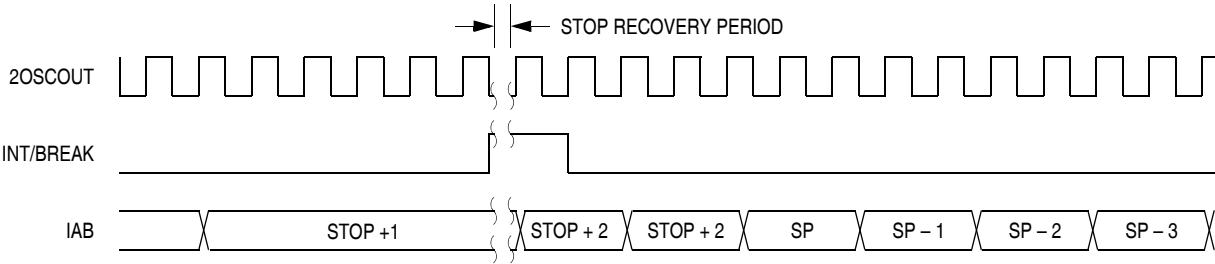


Figure 7-19. Stop Mode Recovery from Interrupt or Break

## 7.8 SIM Registers

The SIM has three memory mapped registers. [Table 7-4](#) shows the mapping of these registers.

Table 7-4. SIM Registers

Address	Register	Access Mode
\$FE00	BSR	User
\$FE01	RSR	User
\$FE03	BFCR	User

### 7.8.1 Break Status Register (BSR)

The break status register contains a flag to indicate that a break caused an exit from stop or wait mode.

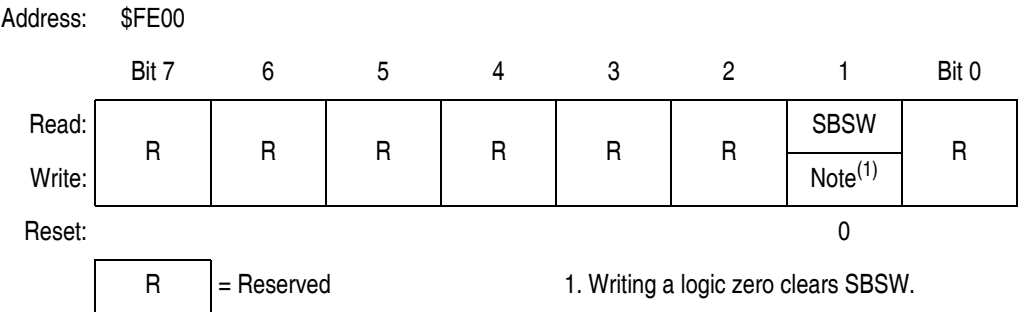


Figure 7-20. Break Status Register (BSR)

9.4.3 Data Format

Communication with the monitor ROM is in standard non-return-to-zero (NRZ) mark/space data format. (See [Figure 9-3](#) and [Figure 9-4](#).)

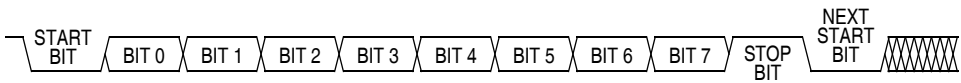


Figure 9-3. Monitor Data Format

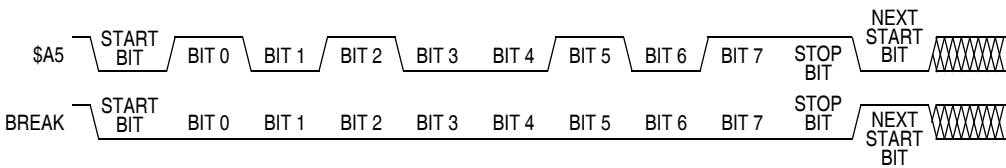


Figure 9-4. Sample Monitor Waveforms

The data transmit and receive rate can be anywhere from 4800 baud to 28.8k-baud. Transmit and receive baud rates must be identical.

9.4.4 Echoing

As shown in [Figure 9-5](#), the monitor ROM immediately echoes each received byte back to the PTB0 pin for error checking.

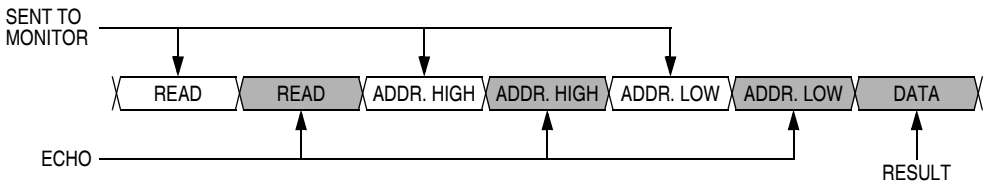


Figure 9-5. Read Transaction

Any result of a command appears after the echo of the last byte of the command.

## Section 10. Timer Interface Module (TIM)

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## 10.2 Introduction

This section describes the timer interface module (TIM2, Version B). The TIM is a two-channel timer that provides a timing reference with input capture, output compare, and pulse-width-modulation functions.

[Figure 10-1](#) is a block diagram of the TIM.

## 10.3 Features

Features of the TIM include the following:

- Two input capture/output compare channels
  - Rising-edge, falling-edge, or any-edge input capture trigger
  - Set, clear, or toggle output compare action
- Buffered and unbuffered pulse width modulation (PWM) signal generation
- Programmable TIM clock input with 7-frequency internal bus clock prescaler selection
- Free-running or modulo up-count operation
- Toggle any channel pin on overflow
- TIM counter stop and reset bits
- Modular architecture expandable to eight channels

## 10.4 Pin Name Conventions

The TIM share two I/O pins with two port D I/O pins. The full name of the TIM I/O pins are listed in [Table 10-1](#). The generic pin name appear in the text that follows.

**Table 10-1. Pin Name Conventions**

TIM Generic Pin Names:	TCH0	TCH1
Full TIM Pin Names:	PTD4/TCH0	PTD5/TCH1

Setting MS0B links channels 0 and 1 and configures them for buffered PWM operation. The TIM channel 0 registers (TCH0H:TCH0L) initially control the buffered PWM output. TIM status control register 0 (TSCR0) controls and monitors the PWM signal from the linked channels. MS0B takes priority over MS0A.

Clearing the toggle-on-overflow bit, TOVx, inhibits output toggles on TIM overflows. Subsequent output compares try to force the output to a state it is already in and have no effect. The result is a 0% duty cycle output.

Setting the channel x maximum duty cycle bit (CHxMAX) and clearing the TOVx bit generates a 100% duty cycle output. (See [10.10.4 TIM Channel Status and Control Registers \(TSC0:TSC1\)](#).)

## 10.6 Interrupts

The following TIM sources can generate interrupt requests:

- TIM overflow flag (TOF) — The TOF bit is set when the TIM counter value rolls over to \$0000 after matching the value in the TIM counter modulo registers. The TIM overflow interrupt enable bit, TOIE, enables TIM overflow CPU interrupt requests. TOF and TOIE are in the TIM status and control register.
- TIM channel flags (CH1F:CH0F) — The CHxF bit is set when an input capture or output compare occurs on channel x. Channel x TIM CPU interrupt requests are controlled by the channel x interrupt enable bit, CHxIE. Channel x TIM CPU interrupt requests are enabled when CHxIE=1. CHxF and CHxIE are in the TIM channel x status and control register.

## 10.7 Wait Mode

The WAIT instruction puts the MCU in low-power-consumption standby mode.

The TIM remains active after the execution of a WAIT instruction. In wait mode the TIM registers are not accessible by the CPU. Any enabled CPU interrupt request from the TIM can bring the MCU out of wait mode.

### 11.4.5 Accuracy and Precision

The conversion process is monotonic and has no missing codes.

## 11.5 Interrupts

When the AIEN bit is set, the ADC module is capable of generating a CPU interrupt after each ADC conversion. A CPU interrupt is generated if the COCO bit is at logic 0. The COCO bit is not used as a conversion complete flag when interrupts are enabled.

## 11.6 Low-Power Modes

The following subsections describe the ADC in low-power modes.

### 11.6.1 Wait Mode

The ADC continues normal operation during wait mode. Any enabled CPU interrupt request from the ADC can bring the MCU out of wait mode. If the ADC is not required to bring the MCU out of wait mode, power down the ADC by setting the CH[4:0] bits in the ADC Status and Control register to logic 1's before executing the WAIT instruction.

### 11.6.2 Stop Mode

The ADC module is inactive after the execution of a STOP instruction. Any pending conversion is aborted. ADC conversions resume when the MCU exits stop mode. Allow one conversion cycle to stabilize the analog circuitry before attempting a new ADC conversion after exiting stop mode.

## 11.7 I/O Signals

The ADC module has 12 channels that are shared with I/O port B and port D.

### 13.5 IRQ Module During Break Interrupts

The system integration module (SIM) controls whether the IRQ1 latch can be cleared during the break state. The BCFE bit in the break flag control register (BFCR) enables software to clear the latches during the break state. (See [Section 7. System Integration Module \(SIM\)](#).)

To allow software to clear the IRQ1 latch during a break interrupt, write a logic one to the BCFE bit. If a latch is cleared during the break state, it remains cleared when the MCU exits the break state.

To protect the latches during the break state, write a logic zero to the BCFE bit. With BCFE at logic zero (its default state), writing to the ACK1 bit in the IRQ status and control register during the break state has no effect on the IRQ latch.


### 13.6 IRQ Status and Control Register (ISCR)

The IRQ Status and Control Register (ISCR) controls and monitors operation of the IRQ module. The ISCR has the following functions:

- Shows the state of the IRQ1 flag
- Clears the IRQ1 latch
- Masks IRQ1 and interrupt request
- Controls triggering sensitivity of the  $\overline{\text{IRQ1}}$  interrupt pin

Address: \$001D

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	IRQF1		IMASK1	MODE1
Write:						ACK1		
Reset:	0	0	0	0	0	0	0	0

 = Unimplemented

**Figure 13-3. IRQ Status and Control Register (INTSCR)**



## IRQF1 — IRQ1 Flag

This read-only status bit is high when the IRQ1 interrupt is pending.  
 1 =  $\overline{\text{IRQ1}}$  interrupt pending  
 0 =  $\overline{\text{IRQ1}}$  interrupt not pending

## ACK1 — IRQ1 Interrupt Request Acknowledge Bit

Writing a logic one to this write-only bit clears the IRQ1 latch. ACK1 always reads as logic zero. Reset clears ACK1.

## IMASK1 — IRQ1 Interrupt Mask Bit

Writing a logic one to this read/write bit disables IRQ1 interrupt requests. Reset clears IMASK1.  
 1 = IRQ1 interrupt requests disabled  
 0 = IRQ1 interrupt requests enabled

## MODE1 — IRQ1 Edge/Level Select Bit

This read/write bit controls the triggering sensitivity of the  $\overline{\text{IRQ1}}$  pin. Reset clears MODE1.  
 1 =  $\overline{\text{IRQ1}}$  interrupt requests on falling edges and low levels  
 0 =  $\overline{\text{IRQ1}}$  interrupt requests on falling edges only

Address: \$001E

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	IRQPUD	R	R	LVIT1	LVIT0	R	R	R
Write:								
Reset:	0	0	0	Not affected	Not affected	0	0	0
POR:	0	0	0	0	0	0	0	0

R = Reserved

**Figure 13-4. Configuration Register 2 (CONFIG2)**

## IRQPUD — $\overline{\text{IRQ1}}$ Pin Pull-up control bit

1 = Internal pull-up is disconnected  
 0 = Internal pull-up is connected between  $\overline{\text{IRQ1}}$  pin and  $V_{DD}$

## 14.5 Wait Mode

The keyboard modules remain active in wait mode. Clearing the IMASKK bit in the keyboard status and control register enables keyboard interrupt requests to bring the MCU out of wait mode.

## 14.6 Stop Mode

The keyboard module remains active in stop mode. Clearing the IMASKK bit in the keyboard status and control register enables keyboard interrupt requests to bring the MCU out of stop mode.

## 14.7 Keyboard Module During Break Interrupts

The system integration module (SIM) controls whether the keyboard interrupt latch can be cleared during the break state. The BCFE bit in the break flag control register (BFCR) enables software to clear status bits during the break state.

To allow software to clear the keyboard interrupt latch during a break interrupt, write a logic 1 to the BCFE bit. If a latch is cleared during the break state, it remains cleared when the MCU exits the break state.

To protect the latch during the break state, write a logic 0 to the BCFE bit. With BCFE at logic 0 (its default state), writing to the keyboard acknowledge bit (ACKK) in the keyboard status and control register during the break state has no effect.

## SBSW — SIM Break Stop/Wait

This status bit is useful in applications requiring a return to wait or stop mode after exiting from a break interrupt. Clear SBSW by writing a logic zero to it. Reset clears SBSW.

1 = Stop mode or wait mode was exited by break interrupt

0 = Stop mode or wait mode was not exited by break interrupt

SBSW can be read within the break state SWI routine. The user can modify the return address on the stack by subtracting one from it. The following code is an example of this. Writing zero to the SBSW bit clears it.

```
; This code works if the H register has been pushed onto the stack in the break
; service routine software. This code should be executed at the end of the
; break service routine software.

HIBYTE EQU 5
LOBYTE EQU 6

; If not SBSW, do RTI

BRCLR SBSW,BSR, RETURN ; See if wait mode or stop mode was exited
; by break.

TST LOBYTE,SP ; If RETURNLO is not zero,
BNE DOLO ; then just decrement low byte.
DEC HIBYTE,SP ; Else deal with high byte, too.
DOLO DEC LOBYTE,SP ; Point to WAIT/STOP opcode.
RETURN PULH ; Restore H register.
RTI
```

## Section 18. Electrical Specifications

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### 18.2 Introduction

This section contains electrical and timing specifications.

## 18.4 Functional Operating Range

**Table 18-2. Operating Range**

Characteristic	Symbol	Value		Unit
Operating temperature range	$T_A$	– 40 to +125	– 40 to +85	°C
Operating voltage range	$V_{DD}$	5 V ± 10%	3 V ± 10%	V

## 18.5 Thermal Characteristics

**Table 18-3. Thermal Characteristics**

Characteristic	Symbol	Value	Unit
Thermal resistance	$\theta_{JA}$		
20-Pin PDIP		70	°C/W
20-Pin SOIC		70	°C/W
28-Pin PDIP		70	°C/W
28-Pin SOIC		70	°C/W
I/O pin power dissipation	$P_{I/O}$	User determined	W
Power dissipation <sup>(1)</sup>	$P_D$	$P_D = (I_{DD} \times V_{DD}) + P_{I/O} =$ $K/(T_J + 273\text{ °C})$	W
Constant <sup>(2)</sup>	K	$P_D \times (T_A + 273\text{ °C})$ $+ P_D^2 \times \theta_{JA}$	W/°C
Average junction temperature	$T_J$	$T_A + (P_D \times \theta_{JA})$	°C
Maximum junction temperature	$T_{JM}$	100	°C

**NOTES:**

1. Power dissipation is a function of temperature.
2. K constant unique to the device. K can be determined for a known  $T_A$  and measured  $P_D$ . With this value of K,  $P_D$  and  $T_J$  can be determined for any value of  $T_A$ .