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Details

Product Status	Obsolete
Core Processor	HC08
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	LED, LVD, POR, PWM
Number of I/O	14
Program Memory Size	1.5KB (1.5K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.3V
Data Converters	A/D 12x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc908jk1cdwe

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Section 1. General Description

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1.2 Introduction

The MC68H(R)C908JL3 is a member of the low-cost, high-performance M68HC08 Family of 8-bit microcontroller units (MCUs). The M68HC08 Family is based on the customer-specified integrated circuit (CSIC) design strategy. All MCUs in the family use the enhanced M68HC08 central processor unit (CPU08) and are available with a variety of modules, memory sizes and types, and package types.

Table 1-1. Summary of Device Variations

Device	FLASH Memory Size	Pin Count
MC68H(R)C908JL3	4096 bytes	28 pins
MC68H(R)C908JK3	4096 bytes	20 pins
MC68H(R)C908JK1	1536 bytes	20 pins

All references to the MC68H(R)C908JL3 in this data book apply equally to the MC68H(R)C908JK3 and MC68H(R)C908JK1, unless otherwise stated.

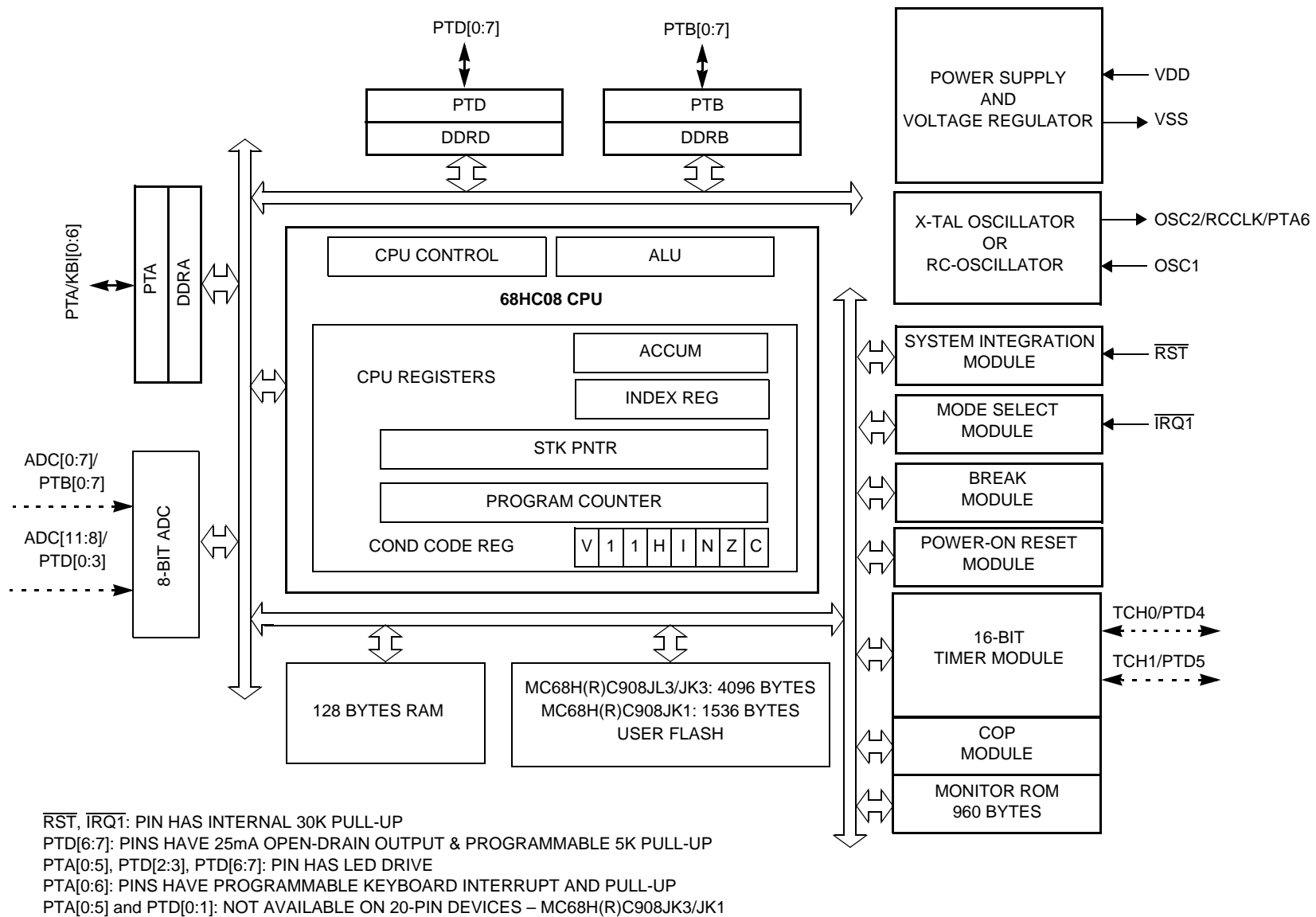



Figure 1-1. MCU Block Diagram

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
\$0021	TIM Counter Register High (TCNTH)	Read:	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
		Write:								
		Reset:	0	0	0	0	0	0	0	0
\$0022	TIM Counter Register Low (TCNTL)	Read:	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
\$0023	TIM Counter Modulo Register High (TMODH)	Read:	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
		Write:								
		Reset:	1	1	1	1	1	1	1	1
\$0024	TIM Counter Modulo Register Low (TMDL)	Read:	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		Write:								
		Reset:	1	1	1	1	1	1	1	1
\$0025	TIM Channel 0 Status and Control Register (TSC0)	Read:	CH0F	CH0IE	MS0B	MS0A	ELS0B	ELS0A	TOV0	CH0MAX
		Write:	0							
		Reset:	0	0	0	0	0	0	0	0
\$0026	TIM Channel 0 Register High (TCH0H)	Read:	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
		Write:								
		Reset:	Indeterminate after reset							
\$0027	TIM Channel 0 Register Low (TCH0L)	Read:	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		Write:								
		Reset:	Indeterminate after reset							
\$0028	TIM Channel 1 Status and Control Register (TSC1)	Read:	CH1F	CH1IE	0	MS1A	ELS1B	ELS1A	TOV1	CH1MAX
		Write:	0							
		Reset:	0	0	0	0	0	0	0	0
\$0029	TIM Channel 1 Register High (TCH1H)	Read:	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
		Write:								
		Reset:	Indeterminate after reset							
\$002A	TIM Channel 1 Register Low (TCH1L)	Read:	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		Write:								
		Reset:	Indeterminate after reset							

= Unimplemented
 = Reserved

Figure 2-2. Control, Status, and Data Registers (Sheet 3 of 5)

Table 2-1. Vector Addresses

Vector Priority	Vector	Address	Vector
<div>Lowest</div> <div></div> <div>Highest</div>	IF15	\$FFDE	ADC Conversion Complete Vector (High)
		\$FFDF	ADC Conversion Complete Vector (Low)
	IF14	\$FFE0	Keyboard Vector (High)
		\$FFE1	Keyboard Vector (Low)
	IF13 to IF6	—	Not Used
	IF5	\$FFF2	TIM Overflow Vector (High)
		\$FFF3	TIM Overflow Vector (Low)
	IF4	\$FFF4	TIM Channel 1 Vector (High)
		\$FFF5	TIM Channel 1 Vector (Low)
	IF3	\$FFF6	TIM Channel 0 Vector (High)
		\$FFF7	TIM Channel 0 Vector (Low)
	IF2	—	Not Used
	IF1	\$FFFA	$\overline{\text{IRQ}}$ Vector (High)
		\$FFFB	$\overline{\text{IRQ}}$ Vector (Low)
	—	\$FFFC	SWI Vector (High)
		\$FFFD	SWI Vector (Low)
—	\$FFFE	Reset Vector (High)	
	\$FFFF	Reset Vector (Low)	

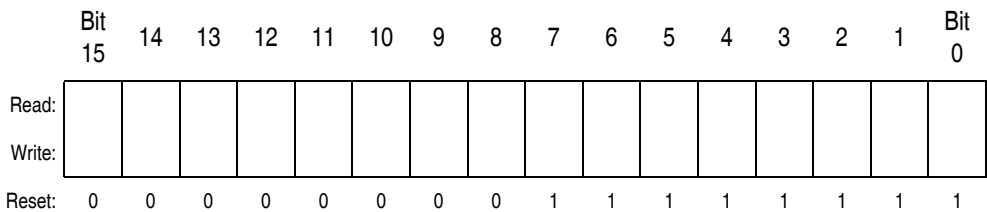


Figure 6-4. Stack Pointer (SP)

NOTE: The location of the stack is arbitrary and may be relocated anywhere in RAM. Moving the SP out of page 0 (\$0000 to \$00FF) frees direct address (page 0) space. For correct operation, the stack pointer must point only to RAM locations.

6.4.4 Program Counter

The program counter is a 16-bit register that contains the address of the next instruction or operand to be fetched.

Normally, the program counter automatically increments to the next sequential memory location every time an instruction or operand is fetched. Jump, branch, and interrupt operations load the program counter with an address other than that of the next sequential location.

During reset, the program counter is loaded with the reset vector address located at \$FFFE and \$FFFF. The vector address is the address of the first instruction to be executed after exiting the reset state.

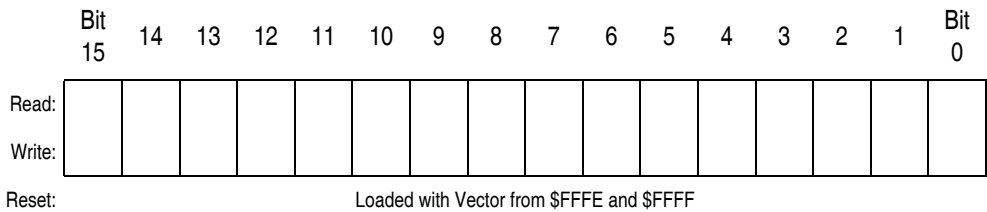


Figure 6-5. Program Counter (PC)

6.4.5 Condition Code Register

The 8-bit condition code register contains the interrupt mask and five flags that indicate the results of the instruction just executed. Bits 6 and

7.4.2.5 LVI Reset

The low-voltage inhibit module (LVI) asserts its output to the SIM when the V_{DD} voltage falls to the LVI trip voltage V_{TRIP} . The LVI bit in the SIM reset status register (SRSR) is set, and the external reset pin (RSTB) is held low while the SIM counter counts out 4096 2OSCCLK cycles. Sixty-four 2OSCOOUT cycles later, the CPU and memories are released from reset to allow the reset vector sequence to occur. The SIM actively pulls down the (RSTB) pin for all internal reset sources.

7.5 SIM Counter

The SIM counter is used by the power-on reset module (POR) and in stop mode recovery to allow the oscillator time to stabilize before enabling the internal bus (IBUS) clocks. The SIM counter also serves as a prescaler for the computer operating properly module (COP). The SIM counter uses 12 stages for counting, followed by a 13th stage that triggers a reset of SIM counters and supplies the clock for the COP module. The SIM counter is clocked by the falling edge of 2OSCOOUT.

7.5.1 SIM Counter During Power-On Reset

The power-on reset module (POR) detects power applied to the MCU. At power-on, the POR circuit asserts the signal PORRST. Once the SIM is initialized, it enables the oscillator to drive the bus clock state machine.

7.5.2 SIM Counter During Stop Mode Recovery

The SIM counter also is used for stop mode recovery. The STOP instruction clears the SIM counter. After an interrupt, break, or reset, the SIM senses the state of the short stop recovery bit, SSREC, in the mask option register. If the SSREC bit is a logic one, then the stop recovery is reduced from the normal delay of 4096 2OSCOOUT cycles down to 32 2OSCOOUT cycles. This is ideal for applications using canned oscillators that do not require long start-up times from stop mode. External crystal applications should use the full stop recovery time, that is, with SSREC cleared in the configuration register (CONFIG).

If $V_{DD} + V_{HI}$ is applied to $\overline{IRQ1}$ and PTB3 is low upon monitor mode entry (**Table 9-1** condition set 1), the bus frequency is a divide-by-two of the external clock input to OSC1. If PTB3 is high with $V_{DD} + V_{HI}$ applied to $\overline{IRQ1}$ upon monitor mode entry (**Table 9-1** condition set 2), the bus frequency is a divide-by-four of the external clock input to OSC1. Holding the PTB3 pin low when entering monitor mode causes a bypass of a divide-by-two stage at the oscillator *only if $V_{DD} + V_{HI}$ is applied to $\overline{IRQ1}$* . In this event, the OSCOUT frequency is equal to the 2OSCOUT frequency, and OSC1 input directly generates internal bus clocks. In this case, the OSC1 signal must have a 50% duty cycle at maximum bus frequency.

Entering monitor mode with $V_{DD} + V_{HI}$ on $\overline{IRQ1}$, the COP is disabled as long as $V_{DD} + V_{HI}$ is applied to either the $\overline{IRQ1}$ or the \overline{RST} . (See **Section 7. System Integration Module (SIM)** for more information on modes of operation.)

If entering monitor mode without high voltage on $\overline{IRQ1}$ and reset vector being blank (\$FFFE and \$FFFF) (**Table 9-1** condition set 3, where applied voltage is V_{DD}), then all port B pin requirements and conditions, including the PTB3 frequency divisor selection, are not in effect. This is to reduce circuit requirements when performing in-circuit programming.

Entering monitor mode with the reset vector being blank, the COP is always disabled regardless of the state of $\overline{IRQ1}$ or the \overline{RST} .

Figure 9-2. shows a simplified diagram of the monitor mode entry when the reset vector is blank and $\overline{IRQ1} = V_{DD}$. An oscillator frequency (XTALCLK or RCCCLK) of 9.8304MHz is required for a baud rate of 9600.

Upon power-on reset, if the received bytes of the security code do not match the data at locations \$FFF6–\$FFFD, the host fails to bypass the security feature. The MCU remains in monitor mode, but reading a FLASH location returns an invalid value and trying to execute code from FLASH causes an illegal address reset. After receiving the eight security bytes from the host, the MCU transmits a break character, signifying that it is ready to receive a command.

NOTE: *The MCU does not transmit a break character until after the host sends the eight security bytes.*

To determine whether the security code entered is correct, check to see if bit 6 of RAM address \$40 is set. If it is, then the correct security code has been entered and FLASH can be accessed.

If the security sequence fails, the device should be reset by a power-on reset and brought up in monitor mode to attempt another entry. After failing the security sequence, the FLASH module can also be mass erased by executing an erase routine that was downloaded into internal RAM. The mass erase operation clears the security code locations so that all eight security bytes become \$FF (blank).

Timer Interface Module (TIM)

Addr.	Register Name	Bit 7	6	5	4	3	2	1	Bit 0
\$0020	TIM Status and Control Register (TSC)	Read: TOF	TOIE	TSTOP	0	0	PS2	PS1	PS0
		Write: 0			TRST				
		Reset: 0	0	1	0	0	0	0	0
\$0021	TIM Counter Register High (TCNTH)	Read: Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
		Write:							
		Reset: 0	0	0	0	0	0	0	0
\$0022	TIM Counter Register Low (TCNTL)	Read: Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		Write:							
		Reset: 0	0	0	0	0	0	0	0
\$0023	TIM Counter Modulo Register High (TMODH)	Read: Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
		Write:							
		Reset: 1	1	1	1	1	1	1	1
\$0024	TIM Counter Modulo Register Low (TMDL)	Read: Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		Write:							
		Reset: 1	1	1	1	1	1	1	1
\$0025	TIM Channel 0 Status and Control Register (TSC0)	Read: CH0F	CH0IE	MS0B	MS0A	ELS0B	ELS0A	TOV0	CH0MAX
		Write: 0							
		Reset: 0	0	0	0	0	0	0	0
\$0026	TIM Channel 0 Register High (TCH0H)	Read: Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
		Write:							
		Reset:	Indeterminate after reset						
\$0027	TIM Channel 0 Register Low (TCH0L)	Read: Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		Write:							
		Reset:	Indeterminate after reset						
\$0028	TIM Channel 1 Status and Control Register (TSC1)	Read: CH1F	CH1IE	0	MS1A	ELS1B	ELS1A	TOV1	CH1MAX
		Write: 0							
		Reset: 0	0	0	0	0	0	0	0

Figure 10-2. TIM I/O Register Summary



IRQF1 — IRQ1 Flag

This read-only status bit is high when the IRQ1 interrupt is pending.
 1 = $\overline{\text{IRQ1}}$ interrupt pending
 0 = $\overline{\text{IRQ1}}$ interrupt not pending

ACK1 — IRQ1 Interrupt Request Acknowledge Bit

Writing a logic one to this write-only bit clears the IRQ1 latch. ACK1 always reads as logic zero. Reset clears ACK1.

IMASK1 — IRQ1 Interrupt Mask Bit

Writing a logic one to this read/write bit disables IRQ1 interrupt requests. Reset clears IMASK1.
 1 = IRQ1 interrupt requests disabled
 0 = IRQ1 interrupt requests enabled

MODE1 — IRQ1 Edge/Level Select Bit

This read/write bit controls the triggering sensitivity of the $\overline{\text{IRQ1}}$ pin. Reset clears MODE1.
 1 = $\overline{\text{IRQ1}}$ interrupt requests on falling edges and low levels
 0 = $\overline{\text{IRQ1}}$ interrupt requests on falling edges only

Address: \$001E

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	IRQPUD	R	R	LVIT1	LVIT0	R	R	R
Write:								
Reset:	0	0	0	Not affected	Not affected	0	0	0
POR:	0	0	0	0	0	0	0	0

R = Reserved

Figure 13-4. Configuration Register 2 (CONFIG2)

IRQPUD — $\overline{\text{IRQ1}}$ Pin Pull-up control bit

1 = Internal pull-up is disconnected
 0 = Internal pull-up is connected between $\overline{\text{IRQ1}}$ pin and V_{DD}

level-triggered interrupt pin must be acknowledged after a delay that depends on the external load.

Another way to avoid a false interrupt:

1. Configure the keyboard pins as outputs by setting the appropriate DDRA bits in the data direction register A.
2. Write logic 1s to the appropriate port A data register bits.
3. Enable the KBI pins by setting the appropriate KBIE_x bits in the keyboard interrupt enable register.

14.4.2 Keyboard Status and Control Register

- Flags keyboard interrupt requests.
- Acknowledges keyboard interrupt requests.
- Masks keyboard interrupt requests.
- Controls keyboard interrupt triggering sensitivity.

Address: \$001A

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	KEYF	0	IMASKK	MODEK
Write:						ACKK		
Reset:	0	0	0	0	0	0	0	0


 = Unimplemented

Figure 14-3. Keyboard Status and Control Register (KBSCR)

Bits 7–4 — Not used

These read-only bits always read as logic 0s.

KEYF — Keyboard Flag Bit

This read-only bit is set when a keyboard interrupt is pending on port-A. Reset clears the KEYF bit.

1 = Keyboard interrupt pending

0 = No keyboard interrupt pending

14.5 Wait Mode

The keyboard modules remain active in wait mode. Clearing the IMASKK bit in the keyboard status and control register enables keyboard interrupt requests to bring the MCU out of wait mode.

14.6 Stop Mode

The keyboard module remains active in stop mode. Clearing the IMASKK bit in the keyboard status and control register enables keyboard interrupt requests to bring the MCU out of stop mode.

14.7 Keyboard Module During Break Interrupts

The system integration module (SIM) controls whether the keyboard interrupt latch can be cleared during the break state. The BCFE bit in the break flag control register (BFCR) enables software to clear status bits during the break state.

To allow software to clear the keyboard interrupt latch during a break interrupt, write a logic 1 to the BCFE bit. If a latch is cleared during the break state, it remains cleared when the MCU exits the break state.

To protect the latch during the break state, write a logic 0 to the BCFE bit. With BCFE at logic 0 (its default state), writing to the keyboard acknowledge bit (ACKK) in the keyboard status and control register during the break state has no effect.

16.4 Functional Description

Figure 16-1 shows the structure of the LVI module. The LVI is enabled after a reset. The LVI module contains a bandgap reference circuit and comparator. Setting LVI disable bit (LVID) disables the LVI to monitor V_{DD} voltage. The LVI trip voltage selection bits (LVIT1, LVIT0) determines at which V_{DD} level the LVI module should take actions.

The LVI module generates one output signal:

LVI Reset — an reset signal will be generated to reset the CPU when V_{DD} drops to below the set trip point.

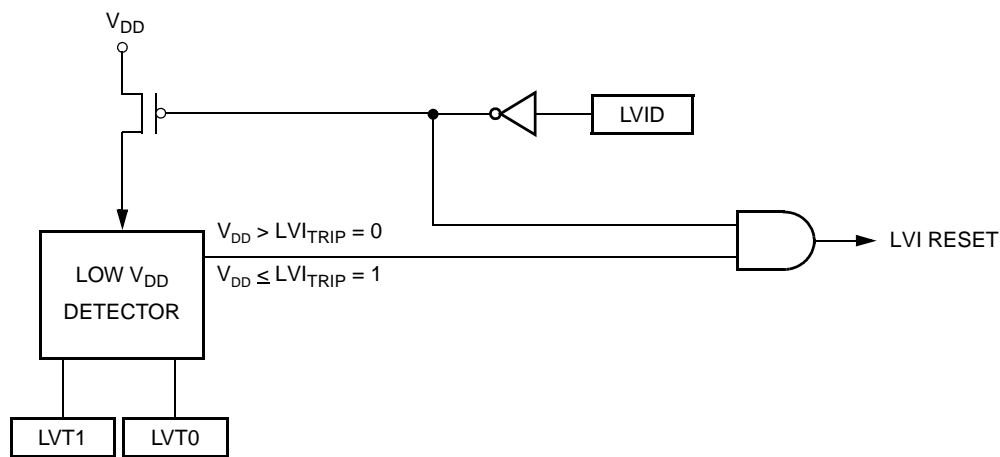


Figure 16-1. LVI Module Block Diagram

16.5 LVI Control Register (CONFIG2/CONFIG1)

Address: \$001E

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	IRQPUD	R	R	LVIT1	LVIT0	R	R	R
Write:								
Reset:	0	0	0	Not affected	Not affected	0	0	0
POR:	0	0	0	0	0	0	0	0

R = Reserved

Figure 16-2. Configuration Register 2 (CONFIG2)

SBSW — SIM Break Stop/Wait

This status bit is useful in applications requiring a return to wait or stop mode after exiting from a break interrupt. Clear SBSW by writing a logic zero to it. Reset clears SBSW.

- 1 = Stop mode or wait mode was exited by break interrupt
- 0 = Stop mode or wait mode was not exited by break interrupt

SBSW can be read within the break state SWI routine. The user can modify the return address on the stack by subtracting one from it. The following code is an example of this. Writing zero to the SBSW bit clears it.

```
; This code works if the H register has been pushed onto the stack in the break
; service routine software. This code should be executed at the end of the
; break service routine software.

HIBYTE EQU 5
LOBYTE EQU 6

; If not SBSW, do RTI

BRCLR SBSW,BSR, RETURN ; See if wait mode or stop mode was exited
; by break.

TST LOBYTE,SP ; If RETURNLO is not zero,
BNE DOLO ; then just decrement low byte.
DEC HIBYTE,SP ; Else deal with high byte, too.
DOLO DEC LOBYTE,SP ; Point to WAIT/STOP opcode.
RETURN PULH ; Restore H register.
RTI
```

17.5.4 Break Flag Control Register (BFCR)

The break control register contains a bit that enables software to clear status bits while the MCU is in a break state.

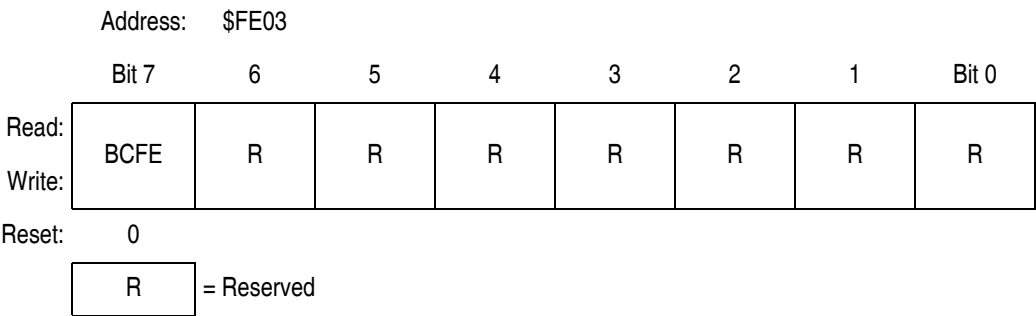


Figure 17-7. Break Flag Control Register (BFCR)

BCFE — Break Clear Flag Enable Bit

This read/write bit enables software to clear status bits by accessing status registers while the MCU is in a break state. To clear status bits during the break state, the BCFE bit must be set.

- 1 = Status bits clearable during break
- 0 = Status bits not clearable during break

17.6 Low-Power Modes

The WAIT and STOP instructions put the MCU in low-power-consumption standby modes.

17.6.1 Wait Mode

If enabled, the break module is active in wait mode. In the break routine, the user can subtract one from the return address on the stack if SBSW is set (see [7.7 Low-Power Modes](#)). Clear the SBSW bit by writing logic zero to it.

17.6.2 Stop Mode

A break interrupt causes exit from stop mode and sets the SBSW bit in the break status register. See [7.8 SIM Registers](#).

18.9 3V DC Electrical Characteristics

Table 18-7. DC Electrical Characteristics (3V)

Characteristic ⁽¹⁾	Symbol	Min	Typ ⁽²⁾	Max	Unit
Output high voltage ($I_{LOAD} = -1.0\text{mA}$) PTA0–PTA6, PTB0–PTB7, PTD0–PTD7	V_{OH}	$V_{DD} - 0.4$	—	—	V
Output low voltage ($I_{LOAD} = 0.8\text{mA}$) PTA6, PTB0–PTB7, PTD0, PTD1, PTD4, PTD5	V_{OL}	—	—	0.4	V
Output low voltage ($I_{LOAD} = 20\text{mA}$) PTD6, PTD7	V_{OL}	—	—	0.5	V
LED drives ($V_{OL} = 1.8\text{V}$) PTA0–PTA5, PTD2, PTD3, PTD6, PTD7	I_{OL}	4	9	12	mA
Input high voltage PTA0–PTA6, PTB0–PTB7, PTD0–PTD7, \overline{RST} , $\overline{IRQ1}$, OSC1	V_{IH}	$0.7 \times V_{DD}$	—	V_{DD}	V
Input low voltage PTA0–PTA6, PTB0–PTB7, PTD0–PTD7, \overline{RST} , $\overline{IRQ1}$, OSC1	V_{IL}	V_{SS}	—	$0.3 \times V_{DD}$	V
V_{DD} supply current Run, $f_{OP} = 2\text{MHz}$ ⁽³⁾ Wait (MC68HRC908xxx) ⁽⁴⁾ Wait (MC68HC908xxx) ⁽⁴⁾ Stop ⁽⁵⁾ -40°C to 85°C	I_{DD}	— — — —	5 1 4 1	8 1.3 4.5 5	mA mA mA μA
Digital I/O ports Hi-Z leakage current	I_{IL}	—	—	± 10	μA
Input current	I_{IN}	—	—	± 1	μA
Capacitance Ports (as input or output)	C_{OUT} C_{IN}	— —	— —	12 8	pF
POR rearm voltage ⁽⁶⁾	V_{POR}	0	—	100	mV
POR rise time ramp rate ⁽⁷⁾	R_{POR}	0.035	—	—	V/ms
Monitor mode entry voltage	$V_{DD} + V_{HI}$	$1.5 \times V_{DD}$	—	8.5	V
Pullup resistors ⁽⁸⁾ PTD6, PTD7 \overline{RST} , $\overline{IRQ1}$, PTA0–PTA6	R_{PU1} R_{PU2}	1.8 16	3.3 26	4.8 36	k Ω k Ω
LVI reset voltage	V_{LVR3}	2.0	2.4	2.69	V

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