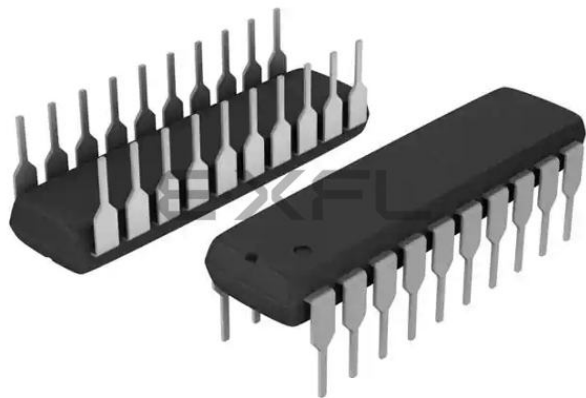




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Details

Product Status	Obsolete
Core Processor	HC08
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	LED, LVD, POR, PWM
Number of I/O	14
Program Memory Size	1.5KB (1.5K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.3V
Data Converters	A/D 12x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	20-DIP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mchc908jk1cpe

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Section 2. Memory

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2.2 Introduction

The CPU08 can address 64 Kbytes of memory space. The memory map, shown in **Figure 2-1**, includes:

- 4096 bytes of user FLASH for MC68H(R)C908JL3/JK3
1536 bytes of user FLASH for MC68H(R)C908JK1
- 128 bytes of RAM
- 48 bytes of user-defined vectors
- 960 bytes of Monitor ROM

4.3 Functional Description

The FLASH memory consists of an array of 4096 or 1536 bytes with an additional 48 bytes for user vectors. The minimum size of FLASH memory that can be erased is 64 bytes; and the maximum size of FLASH memory that can be programmed in a program cycle is 32 bytes (a row). Program and erase operations are facilitated through control bits in the Flash Control Register (FLCR). Details for these operations appear later in this section. The address ranges for the user memory and vectors are:

- \$EC00 – \$FBFF; user memory, 4096 bytes:
MC68H(R)C908JL3/JK3
- \$F600 – \$FBFF; user memory, 1536 bytes: MC68H(R)C908JK1
- \$FFD0 – \$FFFF; user interrupt vectors, 48 bytes.

NOTE: *An erased bit reads as logic 1 and a programmed bit reads as logic 0. A security feature prevents viewing of the FLASH contents.¹*

4.4 FLASH Control Register

The FLASH Control Register controls FLASH program and erase operations.

Address: \$FE08

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	HVEN	MASS	ERASE	PGM
Write:								
Reset:	0	0	0	0	0	0	0	0

Figure 4-1. FLASH Control Register (FLCR)

HVEN — High Voltage Enable Bit

This read/write bit enables high voltage from the charge pump to the memory for either program or erase operation. It can only be set if either PGM=1 or ERASE=1 and the proper sequence for program or erase is followed.

1. No security feature is absolutely secure. However, Freescale's strategy is to make reading or copying the FLASH difficult for unauthorized users.

Table 6-1. Instruction Set Summary

Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Cycles
			V	H	I	N	Z	C				
SUB #opr SUB opr SUB opr SUB opr,X SUB opr,X SUB ,X SUB opr,SP SUB opr,SP	Subtract	$A \leftarrow (A) - (M)$	↑	—	—	↑	↑	↑	IMM DIR EXT IX2 IX1 IX SP1 SP2	A0 B0 C0 D0 E0 F0 9EE0 9ED0	ii dd hh ll ee ff ff ff ee ff	2 3 4 4 3 2 4 5
SWI	Software Interrupt	PC ← (PC) + 1; Push (PCL) SP ← (SP) – 1; Push (PCH) SP ← (SP) – 1; Push (X) SP ← (SP) – 1; Push (A) SP ← (SP) – 1; Push (CCR) SP ← (SP) – 1; I ← 1 PCH ← Interrupt Vector High Byte PCL ← Interrupt Vector Low Byte	—	—	1	—	—	—	INH	83		9
TAP	Transfer A to CCR	$CCR \leftarrow (A)$	↑	↑	↑	↑	↑	↑	INH	84		2
TAX	Transfer A to X	$X \leftarrow (A)$	—	—	—	—	—	—	INH	97		1
TPA	Transfer CCR to A	$A \leftarrow (CCR)$	—	—	—	—	—	—	INH	85		1
TST opr TSTA TSTX TST opr,X TST ,X TST opr,SP	Test for Negative or Zero	$(A) - \$00$ or $(X) - \$00$ or $(M) - \$00$	0	—	—	↑	↑	—	DIR INH INH IX1 IX SP1	3D 4D 5D 6D 7D 9E6D	dd ff ff	3 1 1 3 2 4
TSX	Transfer SP to H:X	$H:X \leftarrow (SP) + 1$	—	—	—	—	—	—	INH	95		2
TXA	Transfer X to A	$A \leftarrow (X)$	—	—	—	—	—	—	INH	9F		1
TXS	Transfer H:X to SP	$(SP) \leftarrow (H:X) - 1$	—	—	—	—	—	—	INH	94		2

System Integration Module (SIM)

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
\$FE00	Break Status Register (BSR)	Read:							SBSW	R
		Write:	R	R	R	R	R		NOTE	
		Reset:	0	0	0	0	0	0	0	0
Note: Writing a logic 0 clears SBSW.										
\$FE01	Reset Status Register (RSR)	Read:	POR	PIN	COP	ILOP	ILAD	MODRST	LVI	0
		Write:								
		POR:	1	0	0	0	0	0	0	0
\$FE02	Reserved	Read:	R	R	R	R	R	R	R	R
		Write:								
		Reset:								
\$FE03	Break Flag Control Register (BFCR)	Read:	BCFE	R	R	R	R	R	R	R
		Write:								
		Reset:	0							
\$FE04	Interrupt Status Register 1 (INT1)	Read:	0	IF5	IF4	IF3	0	IF1	0	0
		Write:	R	R	R	R	R	R	R	R
		Reset:	0	0	0	0	0	0	0	0
\$FE05	Interrupt Status Register 2 (INT2)	Read:	IF14	0	0	0	0	0	0	0
		Write:	R	R	R	R	R	R	R	R
		Reset:	0	0	0	0	0	0	0	0
\$FE06	Interrupt Status Register 3 (INT3)	Read:	0	0	0	0	0	0	0	IF15
		Write:	R	R	R	R	R	R	R	R
		Reset:	0	0	0	0	0	0	0	0
				= Unimplemented				R	= Reserved	

Figure 7-2. SIM I/O Register Summary

Section 8. Oscillator (OSC)

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8.2 Introduction

The oscillator module provides the reference clock for the MCU system and bus. Two types of oscillator modules are available:

- MC68HC908xxx— built-in oscillator module (X-tal oscillator) that requires an external crystal or ceramic-resonator. This option also allows an external clock that can be driven directly into OSC1.
- MC68HRC908xxx — built-in oscillator module (RC oscillator) that requires an external RC connection only.

The series resistor (R_S) is included in the diagram to follow strict Pierce oscillator guidelines and may not be required for all ranges of operation, especially with high frequency crystals. Refer to the crystal manufacturer's data for more information.

8.4 RC Oscillator (MC68HRC908xxx)

The RC oscillator circuit is designed for use with external R and C to provide a clock source with tolerance less than 10%.

In its typical configuration, the RC oscillator requires two external components, one R and one C. Component values should have a tolerance of 1% or less, to obtain a clock source with less than 10% tolerance. The oscillator configuration uses two components:

- C_{EXT}
- R_{EXT}

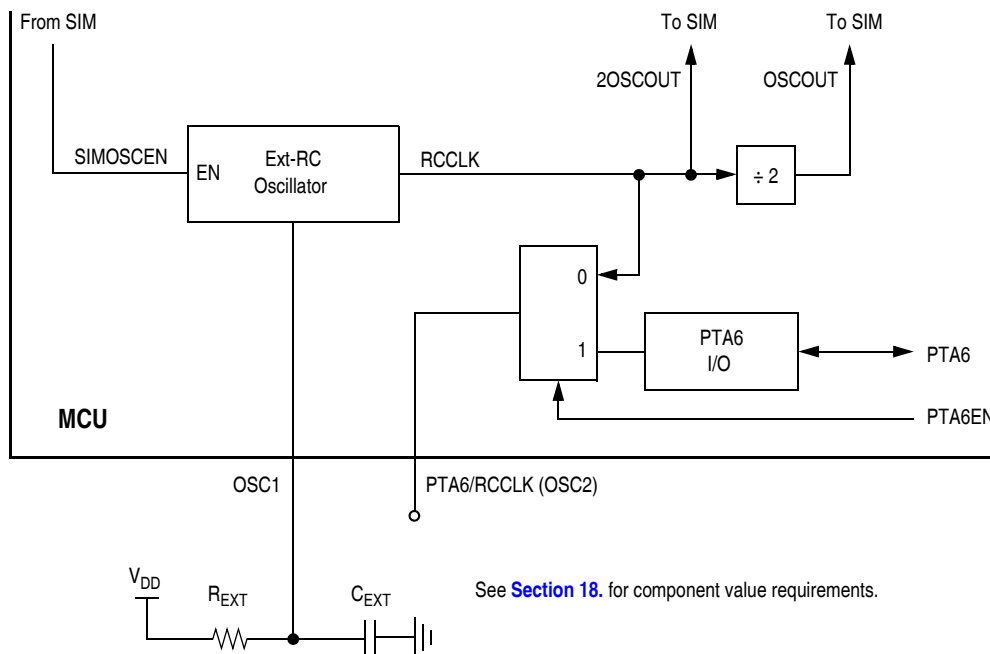


Figure 8-2. RC Oscillator External Connections

8.7 Oscillator During Break Mode

The oscillator continues to drive OSCOUT and 2OSCOUT when the device enters the break state.

9.3 Features

Features of the monitor ROM include the following:

- Normal user-mode pin functionality
- One pin dedicated to serial communication between monitor ROM and host computer
- Standard mark/space non-return-to-zero (NRZ) communication with host computer
- Execution of code in RAM or FLASH
- FLASH memory security feature¹
- FLASH memory programming interface
- 960 bytes monitor ROM code size
- Monitor mode entry without high voltage, $V_{DD} + V_{HI}$, if reset vector is blank (\$FFFE and \$FFFF contain \$FF)
- Standard monitor mode entry if high voltage, $V_{DD} + V_{HI}$, is applied to $\overline{IRQ1}$

9.4 Functional Description

The monitor ROM receives and executes commands from a host computer. **Figure 9-1** shows a example circuit used to enter monitor mode and communicate with a host computer via a standard RS-232 interface.

Simple monitor commands can access any memory address. In monitor mode, the MCU can execute host-computer code in RAM while most MCU pins retain normal operating mode functions. All communication between the host computer and the MCU is through the PTB0 pin. A level-shifting and multiplexing interface is required between PTB0 and the host computer. PTB0 is used in a wired-OR configuration and requires a pull-up resistor.

1. No security feature is absolutely secure. However, Freescale's strategy is to make reading or copying the FLASH difficult for unauthorized users.

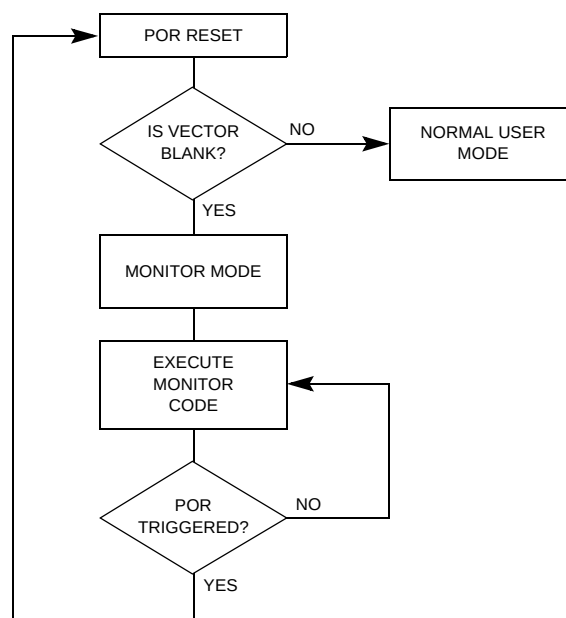


Figure 9-2. Low-Voltage Monitor Mode Entry Flowchart

Enter monitor mode with the pin configuration shown above by pulling $\overline{\text{RST}}$ low and then high. The rising edge of $\overline{\text{RST}}$ latches monitor mode. Once monitor mode is latched, the values on the specified pins can change.

Once out of reset, the MCU waits for the host to send eight security bytes. (See [9.5 Security](#).) After the security bytes, the MCU sends a break signal (10 consecutive logic zeros) to the host, indicating that it is ready to receive a command. The break signal also provides a timing reference to allow the host to determine the necessary baud rate.

In monitor mode, the MCU uses different vectors for reset, SWI, and break interrupt. The alternate vectors are in the \$FE page instead of the \$FF page and allow code execution from the internal monitor firmware instead of user code.

Table 9-4. READ (Read Memory) Command

Description	Read byte from memory
Operand	Specifies 2-byte address in high byte:low byte order
Data Returned	Returns contents of specified address
Opcode	\$4A
Command Sequence SENT TO MONITOR READ READ ADDR. HIGH ADDR. HIGH ADDR. LOW ADDR. LOW DATA ECHO RESULT	

Table 9-5. WRITE (Write Memory) Command

Description	Write byte to memory
Operand	Specifies 2-byte address in high byte:low byte order; low byte followed by data byte
Data Returned	None
Opcode	\$49
Command Sequence SENT TO MONITOR WRITE WRITE ADDR. HIGH ADDR. HIGH ADDR. LOW ADDR. LOW DATA DATA ECHO	

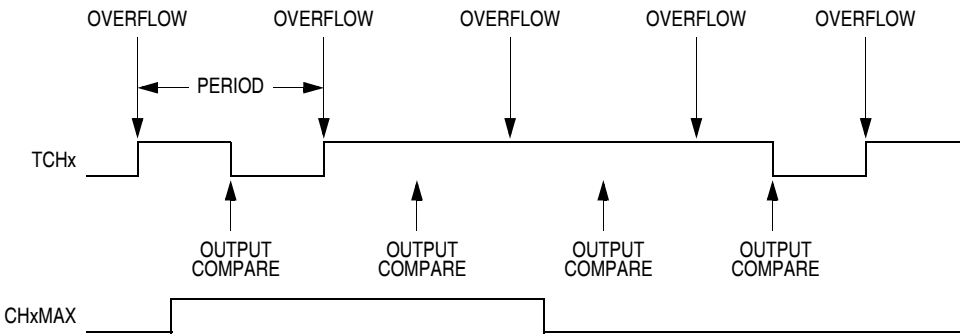


Figure 10-8. CHxMAX Latency

10.10.5 TIM Channel Registers (TCH0H/L:TCH1H/L)

These read/write registers contain the captured TIM counter value of the input capture function or the output compare value of the output compare function. The state of the TIM channel registers after reset is unknown.

In input capture mode ($MSxB:MSxA = 0:0$), reading the high byte of the TIM channel x registers (TCHxH) inhibits input captures until the low byte (TCHxL) is read.

In output compare mode ($MSxB:MSxA \neq 0:0$), writing to the high byte of the TIM channel x registers (TCHxH) inhibits output compares until the low byte (TCHxL) is written.

12.6.2 Data Direction Register D (DDRD)

Data direction register D determines whether each port D pin is an input or an output. Writing a logic one to a DDRD bit enables the output buffer for the corresponding port D pin; a logic zero disables the output buffer.

Address: \$0007

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	DDRD7	DDRD6	DDRD5	DDRD4	DDRD3	DDRD2	DDRD1	DDRD0
Write:	DDRD7	DDRD6	DDRD5	DDRD4	DDRD3	DDRD2	DDRD1	DDRD0
Reset:	0	0	0	0	0	0	0	0

Figure 12-10. Data Direction Register D (DDRD)

DDRD[7:0] — Data Direction Register D Bits

These read/write bits control port D data direction. Reset clears DDRD[7:0], configuring all port D pins as inputs.

- 1 = Corresponding port D pin configured as output
- 0 = Corresponding port D pin configured as input

NOTE: Avoid glitches on port D pins by writing to the port D data register before changing data direction register D bits from 0 to 1. [Figure 12-11](#) shows the port D I/O logic.

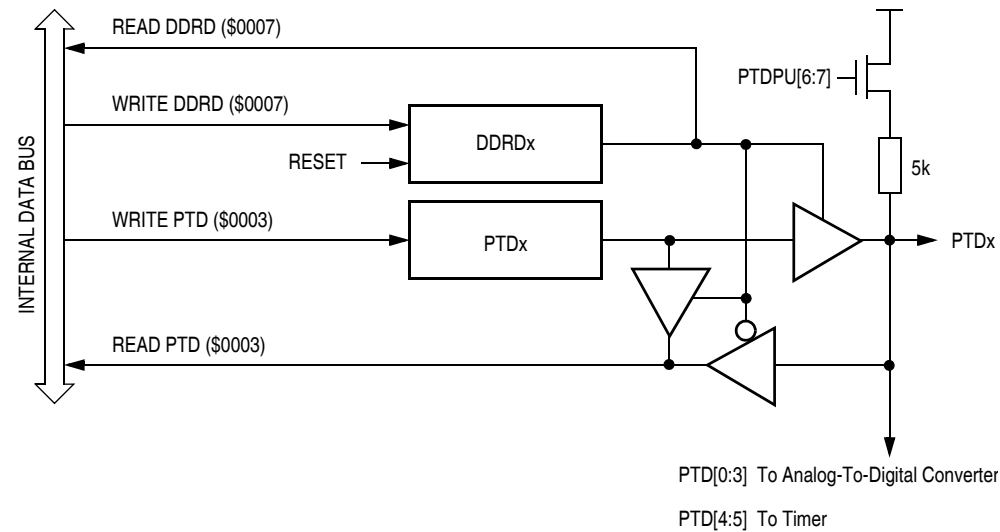


Figure 12-11. Port D I/O Circuit

Section 16. Low Voltage Inhibit (LVI)

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16.2 Introduction

This section describes the low-voltage inhibit module (LVI), which monitors the voltage on the V_{DD} pin and generates a reset when the V_{DD} voltage falls to the LVI trip (LVI_{TRIP}) voltage.

16.3 Features

Features of the LVI module include the following:

- Selectable LVI trip voltage
- Selectable LVI circuit disable

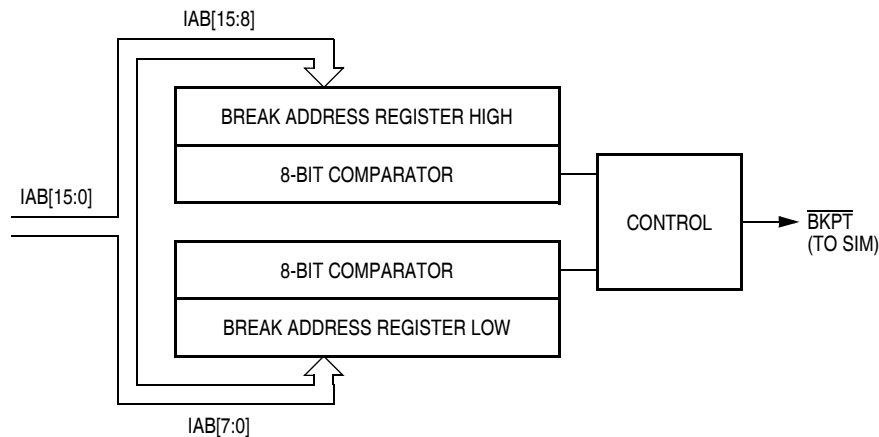


Figure 17-1. Break Module Block Diagram

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
\$FE00	Break Status Register (BSR)	Read:							SBSW	
		Write:	R	R	R	R	R	R	See note	R
		Reset:	0							
\$FE03	Break Flag Control Register (BFCR)	Read:								
		Write:	BCFE	R	R	R	R	R	R	R
		Reset:	0							
\$FE0C	Break Address High Register (BRKH)	Read:								
		Write:	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
		Reset:	0	0	0	0	0	0	0	0
\$FE0D	Break Address low Register (BRKL)	Read:								
		Write:	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		Reset:	0	0	0	0	0	0	0	0
\$FE0E	Break Status and Control Register (BRKSCR)	Read:								
		Write:	BRKE	BRKA						
		Reset:	0	0	0	0	0	0	0	0

Note: Writing a logic 0 clears SBSW. = Unimplemented R = Reserved

Figure 17-2. Break I/O Register Summary

17.5.4 Break Flag Control Register (BFCR)

The break control register contains a bit that enables software to clear status bits while the MCU is in a break state.

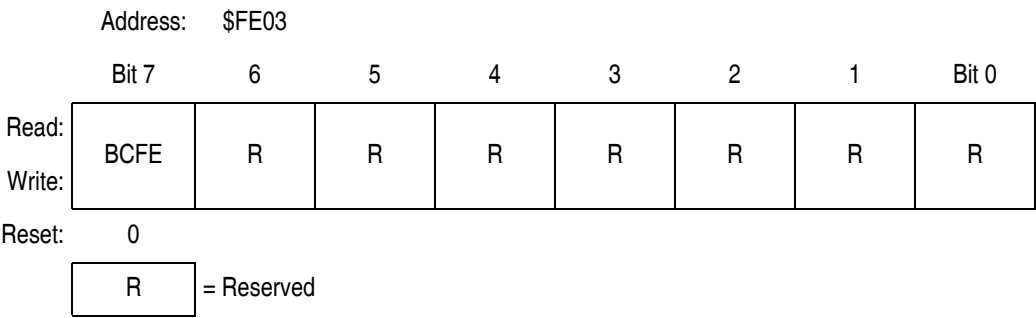


Figure 17-7. Break Flag Control Register (BFCR)

BCFE — Break Clear Flag Enable Bit

This read/write bit enables software to clear status bits by accessing status registers while the MCU is in a break state. To clear status bits during the break state, the BCFE bit must be set.

- 1 = Status bits clearable during break
- 0 = Status bits not clearable during break

17.6 Low-Power Modes

The WAIT and STOP instructions put the MCU in low-power-consumption standby modes.

17.6.1 Wait Mode

If enabled, the break module is active in wait mode. In the break routine, the user can subtract one from the return address on the stack if SBSW is set (see [7.7 Low-Power Modes](#)). Clear the SBSW bit by writing logic zero to it.

17.6.2 Stop Mode

A break interrupt causes exit from stop mode and sets the SBSW bit in the break status register. See [7.8 SIM Registers](#).

18.4 Functional Operating Range

Table 18-2. Operating Range

Characteristic	Symbol	Value		Unit
Operating temperature range	T_A	– 40 to +125	– 40 to +85	°C
Operating voltage range	V_{DD}	5V ± 10%	3V ± 10%	V

18.5 Thermal Characteristics

Table 18-3. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal resistance	θ_{JA}		
20-Pin PDIP		70	°C/W
20-Pin SOIC		70	°C/W
28-Pin PDIP		70	°C/W
28-Pin SOIC		70	°C/W
I/O pin power dissipation	$P_{I/O}$	User determined	W
Power dissipation ⁽¹⁾	P_D	$P_D = (I_{DD} \times V_{DD}) + P_{I/O} =$ $K/(T_J + 273\text{ °C})$	W
Constant ⁽²⁾	K	$P_D \times (T_A + 273\text{ °C})$ $+ P_D^2 \times \theta_{JA}$	W/°C
Average junction temperature	T_J	$T_A + (P_D \times \theta_{JA})$	°C
Maximum junction temperature	T_{JM}	100	°C

NOTES:

1. Power dissipation is a function of temperature.
2. K constant unique to the device. K can be determined for a known T_A and measured P_D . With this value of K, P_D and T_J can be determined for any value of T_A .

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MC68HC908JL3/H

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