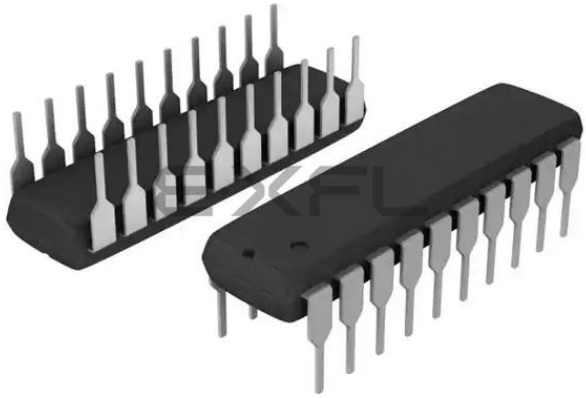


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC08
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	LED, LVD, POR, PWM
Number of I/O	14
Program Memory Size	1.5KB (1.5K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 12x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	20-DIP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mchc908jk1mpe

7.8.1 Break Status Register (BSR) 91
7.8.2 Reset Status Register (RSR) 92
7.8.3 Break Flag Control Register (BFCR) 94

Section 8. Oscillator (OSC)

8.1 Contents 95
8.2 Introduction 95
8.3 X-tal Oscillator (MC68HC908xxx) 96
8.4 RC Oscillator (MC68HRC908xxx) 97
8.5 I/O Signals 98
8.5.1 Crystal Amplifier Input Pin (OSC1) 98
8.5.2 Crystal Amplifier Output Pin (OSC2/PTA6/RCCLK) 98
8.5.3 Oscillator Enable Signal (SIMOSCEN) 98
8.5.4 X-tal Oscillator Clock (XTALCLK) 98
8.5.5 RC Oscillator Clock (RCCLK) 99
8.5.6 Oscillator Out 2 (2OSCOUT) 99
8.5.7 Oscillator Out (OSCOUT) 99
8.6 Low Power Modes 99
8.6.1 Wait Mode 99
8.6.2 Stop Mode 99
8.7 Oscillator During Break Mode 100

Section 9. Monitor ROM (MON)

9.1 Contents 101
9.2 Introduction 101
9.3 Features 102
9.4 Functional Description 102
9.4.1 Entering Monitor Mode 104
9.4.2 Baud Rate 107
9.4.3 Data Format 108
9.4.4 Echoing 108
9.4.5 Break Signal 109

List of Tables

Table	Title	Page
1-1	Summary of Device Variations	21
1-2	Pin Functions	26
2-1	Vector Addresses	35
6-1	Instruction Set Summary	60
6-2	Opcode Map	69
7-1	Signal Name Conventions	73
7-2	PIN Bit Set Timing	76
7-3	Interrupt Sources	85
7-4	SIM Registers	91
9-1	Monitor Mode Entry Requirements and Options	104
9-2	Monitor Mode Vector Differences	107
9-3	Monitor Baud Rate Selection	107
9-4	READ (Read Memory) Command	110
9-5	WRITE (Write Memory) Command	110
9-6	IREAD (Indexed Read) Command	111
9-7	IWRITE (Indexed Write) Command	111
9-8	READSP (Read Stack Pointer) Command	112
9-9	RUN (Run User Program) Command	112
10-1	Pin Name Conventions	116
10-2	Prescaler Selection	129
10-3	Mode, Edge, and Level Selection	134
11-1	MUX Channel Select	144
11-2	ADC Clock Divide Ratio	146

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0021	TIM Counter Register High (TCNTH)	Read:	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0022	TIM Counter Register Low (TCNTL)	Read:	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0023	TIM Counter Modulo Register High (TMODH)	Read:	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
		Write:								
		Reset:	1	1	1	1	1	1	1	1
$0024	TIM Counter Modulo Register Low (TMODL)	Read:	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		Write:								
		Reset:	1	1	1	1	1	1	1	1
$0025	TIM Channel 0 Status and Control Register (TSC0)	Read:	CH0F	CH0IE	MS0B	MS0A	ELS0B	ELS0A	TOV0	CH0MAX
		Write:	0							
		Reset:	0	0	0	0	0	0	0	0
$0026	TIM Channel 0 Register High (TCH0H)	Read:	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
		Write:								
		Reset:	Indeterminate after reset							
$0027	TIM Channel 0 Register Low (TCH0L)	Read:	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		Write:								
		Reset:	Indeterminate after reset							
$0028	TIM Channel 1 Status and Control Register (TSC1)	Read:	CH1F	CH1IE	0	MS1A	ELS1B	ELS1A	TOV1	CH1MAX
		Write:	0							
		Reset:	0	0	0	0	0	0	0	0
$0029	TIM Channel 1 Register High (TCH1H)	Read:	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
		Write:								
		Reset:	Indeterminate after reset							
$002A	TIM Channel 1 Register Low (TCH1L)	Read:	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		Write:								
		Reset:	Indeterminate after reset							

= Unimplemented R = Reserved

Figure 2-2. Control, Status, and Data Registers (Sheet 3 of 5)

Section 6. Central Processor Unit (CPU)

6.1 Contents

6.2 Introduction 51
6.3 Features 52
6.4 CPU Registers 52
6.4.1 Accumulator 53
6.4.2 Index Register 54
6.4.3 Stack Pointer 54
6.4.4 Program Counter 55
6.4.5 Condition Code Register 55
6.5 Arithmetic/Logic Unit (ALU) 58
6.6 Low-Power Modes 58
6.6.1 Wait Mode 58
6.6.2 Stop Mode 59
6.7 CPU During Break Interrupts 59
6.8 Instruction Set Summary 59
6.9 Opcode Map 59

6.2 Introduction

The M68HC08 CPU (central processor unit) is an enhanced and fully object-code-compatible version of the M68HC05 CPU. The *CPU08 Reference Manual* (Freescale document order number CPU08RM/AD) contains a description of the CPU instruction set, addressing modes, and architecture.

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$FE00	Break Status Register (BSR)	Read:	R	R	R	R	R	R	SBSW	R
		Write:							NOTE	
		Reset:	0	0	0	0	0	0	0	0

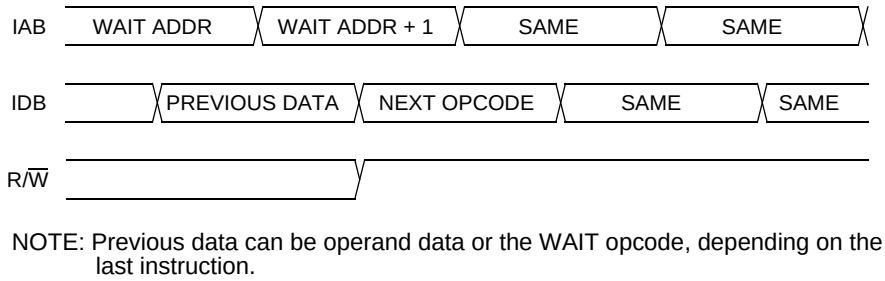
Note: Writing a logic 0 clears SBSW.

$FE01	Reset Status Register (RSR)	Read:	POR	PIN	COP	ILOP	ILAD	MODRST	LVI	0
		Write:								
		POR:	1	0	0	0	0	0	0	0
$FE02	Reserved	Read:	R	R	R	R	R	R	R	R
		Write:								
		Reset:								
$FE03	Break Flag Control Register (BFCR)	Read:	BCFE	R	R	R	R	R	R	R
		Write:								
		Reset:	0							
$FE04	Interrupt Status Register 1 (INT1)	Read:	0	IF5	IF4	IF3	0	IF1	0	0
		Write:	R	R	R	R	R	R	R	R
		Reset:	0	0	0	0	0	0	0	0
$FE05	Interrupt Status Register 2 (INT2)	Read:	IF14	0	0	0	0	0	0	0
		Write:	R	R	R	R	R	R	R	R
		Reset:	0	0	0	0	0	0	0	0
$FE06	Interrupt Status Register 3 (INT3)	Read:	0	0	0	0	0	0	0	IF15
		Write:	R	R	R	R	R	R	R	R
		Reset:	0	0	0	0	0	0	0	0

= Unimplemented R = Reserved

Figure 7-2. SIM I/O Register Summary

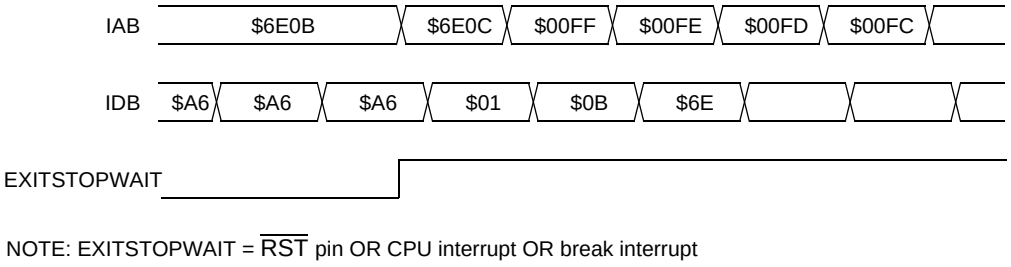
status register (BSR). If the COP disable bit, COPD, in the mask option register is logic zero, then the computer operating properly module (COP) is enabled and remains active in wait mode.



NOTE: Previous data can be operand data or the WAIT opcode, depending on the last instruction.

Figure 7-15. Wait Mode Entry Timing

Figure 7-16 and **Figure 7-17** show the timing for WAIT recovery.



NOTE: EXITSTOPWAIT = $\overline{\text{RST}}$ pin OR CPU interrupt OR break interrupt

Figure 7-16. Wait Recovery from Interrupt or Break

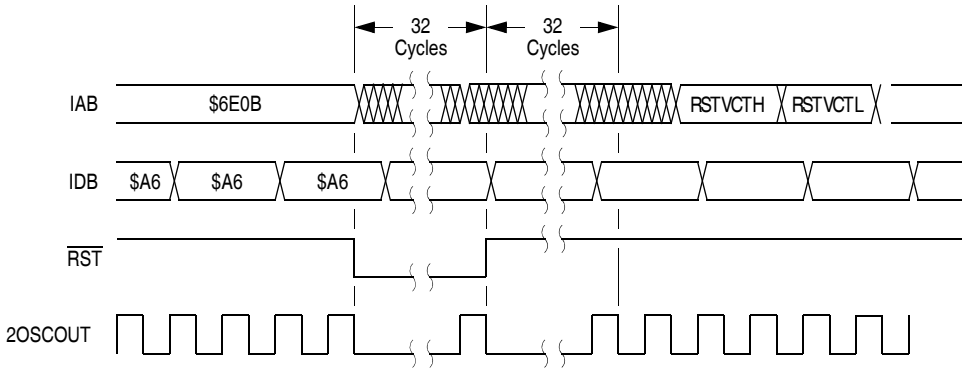


Figure 7-17. Wait Recovery from Internal Reset

8.3 X-tal Oscillator (MC68HC908xxx)

The X-tal oscillator circuit is designed for use with an external crystal or ceramic resonator to provide accurate clock source.

In its typical configuration, the X-tal oscillator is connected in a Pierce oscillator configuration, as shown in **Figure 8-1**. This figure shows only the logical representation of the internal components and may not represent actual circuitry. The oscillator configuration uses five components:

- Crystal, X_1
- Fixed capacitor, C_1
- Tuning capacitor, C_2 (can also be a fixed capacitor)
- Feedback resistor, R_B
- Series resistor, R_S (optional)

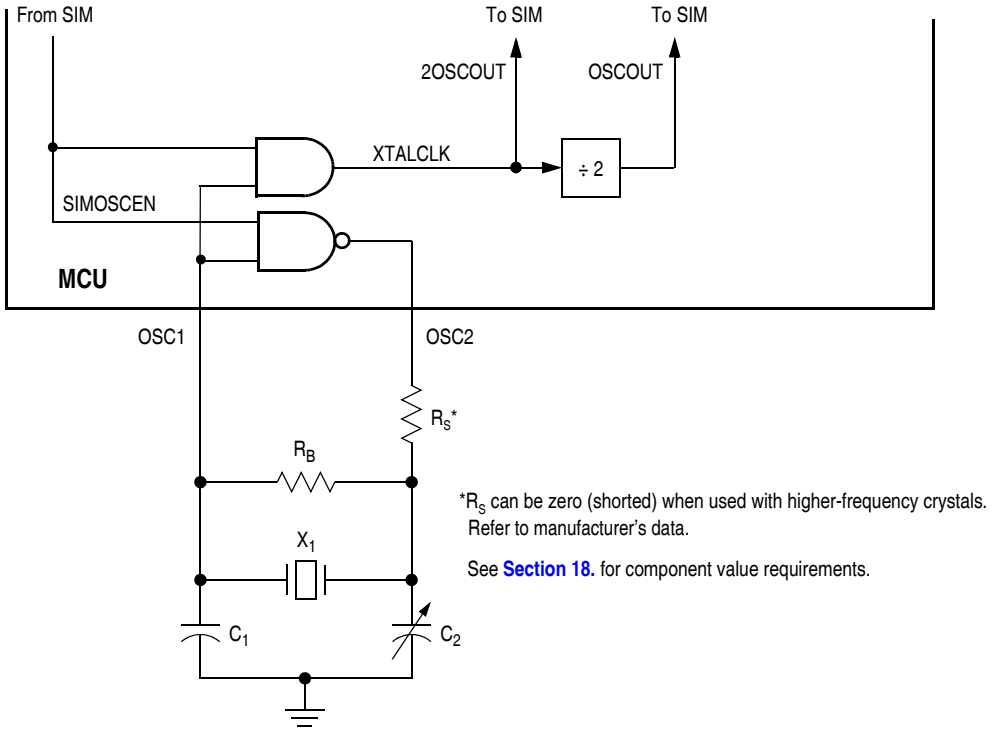


Figure 8-1. X-tal Oscillator External Connections

8.5.5 RC Oscillator Clock (RCCLK)

RCCLK is the RC oscillator output signal. Its frequency is directly proportional to the time constant of the external R and C. **Figure 8-2** shows only the logical relation of RCCLK to OSC1 and may not represent the actual circuitry.

8.5.6 Oscillator Out 2 (2OSCOUT)

2OSCOUT is same as the input clock (XTALCLK or RCCLK). This signal is driven to the SIM module and is used to determine the COP cycles.

8.5.7 Oscillator Out (OSCOUT)

The frequency of this signal is equal to half of the 2OSCOUT, this signal is driven to the SIM for generation of the bus clocks used by the CPU and other modules on the MCU. OSCOUT will be divided again in the SIM and results in the internal bus frequency being one fourth of the XTALCLK or RCCLK frequency.

8.6 Low Power Modes

The WAIT and STOP instructions put the MCU in low-power consumption standby modes.

8.6.1 Wait Mode

The WAIT instruction has no effect on the oscillator logic. OSCOUT and 2OSCOUT continues to drive to the SIM module.

8.6.2 Stop Mode

The STOP instruction disables the XTALCLK or the RCCLK output, hence OSCOUT and 2OSCOUT.

9.4.1 Entering Monitor Mode

Table 9-1 shows the pin conditions for entering monitor mode. As specified in the table, monitor mode may be entered after a POR and will allow communication at 9600 baud provided one of the following sets of conditions is met:

1. If $\overline{IRQ1} = V_{DD} + V_{HI}$:
   - External clock on OSC1 is 4.9125 MHz
   - PTB3 = low
2. If $\overline{IRQ1} = V_{DD} + V_{HI}$:
   - External clock on OSC1 is 9.8304 MHz
   - PTB3 = high
3. If $FFFE & $FFFF is blank (contains $FF):
   - The oscillator clock is 9.8304 MHz (X-tal or RC)
   - $\overline{IRQ1} = V_{DD}$

Table 9-1. Monitor Mode Entry Requirements and Options

$\overline{IRQ1}$	$FFFE and $FFFF	PTB3	PTB2	PTB1	PTB0	Clock Source and Frequency	Bus Frequency	Comments
$V_{DD} + V_{HI}$	X	0	0	1	1	OSC1 at 4.9152 MHz	2.4576 MHz	Bypasses X-tal or RC oscillator; external clock driven directly into OSC1. 9600 baud communication on PTB0. COP disabled.
$V_{DD} + V_{HI}$	X	1	0	1	1	OSC1 at 9.8304 MHz	2.4576 MHz	
V_{DD}	BLANK (contain $FF)	X	X	X	1	X-tal or RC oscillator at 9.8304 MHz	2.4576 MHz	Low-voltage entry to monitor mode. 9600 baud communication on PTB0. COP disabled.
V_{DD}	NOT BLANK	X	X	X	X	X-tal or RC oscillator at desired frequency	XTALCLK ÷ 4 or RCCLK ÷ 4	Enters User mode. If $FFFE and $FFFF is blank, MCU will encounter an illegal address reset.

Notes:
1. PTB3 = 0: Bypasses the divide-by-two prescaler to SIM when using $V_{DD} + V_{HI}$ for monitor mode entry. The OSC1 clock must be 50% duty cycle for this condition.
2. XTALCLK is the X-tal oscillator output, for MC68HC908xxx. See Figure 8-1.
4. RCCLK is the RC oscillator output, for MC68HRC908xxx. See Figure 8-2.
5. See Table 18-4 for $V_{DD} + V_{HI}$ voltage level requirements.

Table 9-4. READ (Read Memory) Command

Description	Read byte from memory
Operand	Specifies 2-byte address in high byte:low byte order
Data Returned	Returns contents of specified address
Opcode	$4A
Command Sequence	

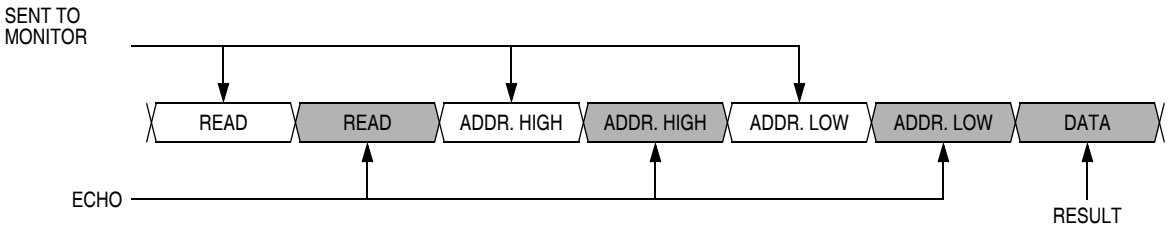


Table 9-5. WRITE (Write Memory) Command

Description	Write byte to memory
Operand	Specifies 2-byte address in high byte:low byte order; low byte followed by data byte
Data Returned	None
Opcode	$49
Command Sequence	

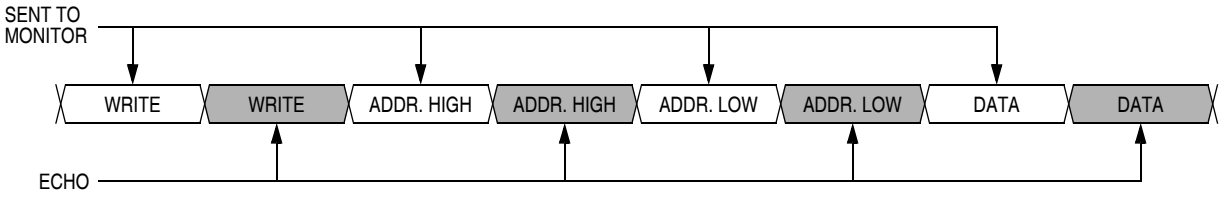


Table 9-8. READSP (Read Stack Pointer) Command

Description	Reads stack pointer
Operand	None
Data Returned	Returns stack pointer in high byte:low byte order
Opcode	$0C
Command Sequence	

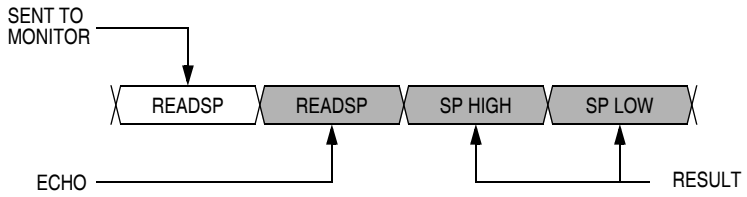
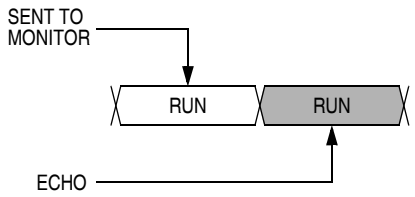


Table 9-9. RUN (Run User Program) Command

Description	Executes RTI instruction
Operand	None
Data Returned	None
Opcode	$28
Command Sequence	

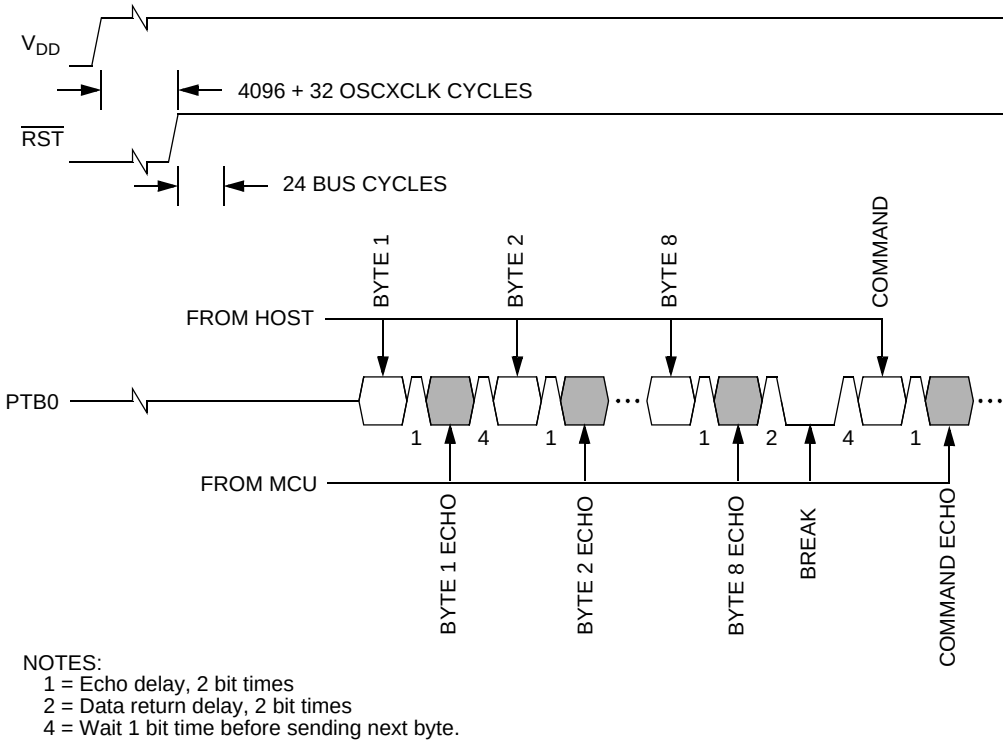


9.5 Security

A security feature discourages unauthorized reading of FLASH locations while in monitor mode. The host can bypass the security feature at monitor mode entry by sending eight security bytes that match the bytes at locations $FFF6–$FFFD. Locations $FFF6–$FFFD contain user-defined data.

NOTE: *Do not leave locations $FFF6–$FFFD blank. For security reasons, program locations $FFF6–$FFFD even if they are not used for vectors.*

During monitor mode entry, the MCU waits after the power-on reset for the host to send the eight security bytes on pin PTB0. If the received bytes match those at locations $FFF6–$FFFD, the host bypasses the security feature and can read all FLASH locations and execute code from FLASH. Security remains bypassed until a power-on reset occurs. If the reset was not a power-on reset, security remains bypassed and security code entry is not required. (See **Figure 9-7**.)



NOTES:
1 = Echo delay, 2 bit times
2 = Data return delay, 2 bit times
4 = Wait 1 bit time before sending next byte.

Figure 9-7. Monitor Mode Entry Timing

$0029	TIM Channel 1 Register High (TCH1H)	Read:	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
		Write:								
		Reset:	Indeterminate after reset							
$002A	TIM Channel 1 Register Low (TCH1L)	Read:	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		Write:								
		Reset:	Indeterminate after reset							

= Unimplemented

Figure 10-2. TIM I/O Register Summary

10.5.1 TIM Counter Prescaler

The TIM clock source is one of the seven prescaler outputs. The prescaler generates seven clock rates from the internal bus clock. The prescaler select bits, PS[2:0], in the TIM status and control register (TSC) select the TIM clock source.

10.5.2 Input Capture

With the input capture function, the TIM can capture the time at which an external event occurs. When an active edge occurs on the pin of an input capture channel, the TIM latches the contents of the TIM counter into the TIM channel registers, TCHxH:TCHxL. The polarity of the active edge is programmable. Input captures can generate TIM CPU interrupt requests.

10.5.3 Output Compare

With the output compare function, the TIM can generate a periodic pulse with a programmable polarity, duration, and frequency. When the counter reaches the value in the registers of an output compare channel, the TIM can set, clear, or toggle the channel pin. Output compares can generate TIM CPU interrupt requests.

11.4.5 Accuracy and Precision

The conversion process is monotonic and has no missing codes.

11.5 Interrupts

When the AIEN bit is set, the ADC module is capable of generating a CPU interrupt after each ADC conversion. A CPU interrupt is generated if the COCO bit is at logic 0. The COCO bit is not used as a conversion complete flag when interrupts are enabled.

11.6 Low-Power Modes

The following subsections describe the ADC in low-power modes.

11.6.1 Wait Mode

The ADC continues normal operation during wait mode. Any enabled CPU interrupt request from the ADC can bring the MCU out of wait mode. If the ADC is not required to bring the MCU out of wait mode, power down the ADC by setting the CH[4:0] bits in the ADC Status and Control register to logic 1’s before executing the WAIT instruction.

11.6.2 Stop Mode

The ADC module is inactive after the execution of a STOP instruction. Any pending conversion is aborted. ADC conversions resume when the MCU exits stop mode. Allow one conversion cycle to stabilize the analog circuitry before attempting a new ADC conversion after exiting stop mode.

11.7 I/O Signals

The ADC module has 12 channels that are shared with I/O port B and port D.

Section 12. I/O Ports

12.1 Contents

12.2 Introduction 147
12.3 Port A 148
12.4 Port A Data Register (PTA) 149
12.4.1 Data Direction Register A (DDRA) 150
12.4.2 Port A Input Pull-up Enable Register (PTAPUE) 151
12.5 Port B 153
12.5.1 Port B Data Register (PTB) 153
12.5.2 Data Direction Register B (DDRB) 153
12.6 Port D 155
12.6.1 Port D Data Register (PTD) 155
12.6.2 Data Direction Register D (DDRD) 156
12.6.3 Port D Control Register (PDCR) 157

12.2 Introduction

Twenty three bidirectional input-output (I/O) pins form three parallel ports. All I/O pins are programmable as inputs or outputs.

NOTE: *Connect any unused I/O pins to an appropriate logic level, either V_{DD} or V_{SS}. Although the I/O ports do not require termination for proper operation, termination reduces excess current consumption and the possibility of electrostatic damage.*

12.5 Port B

Port B is an 8-bit special function port that shares all eight of its port pins with the Analog-to-Digital converter (ADC) module, **See Section 11.**

12.5.1 Port B Data Register (PTB)

The port B data register contains a data latch for each of the eight port B pins.

Address: $0001

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PTB7	PTB6	PTB5	PTB4	PTB3	PTB2	PTB1	PTB0
Reset:	Unaffected by reset							
Alternative Function:	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC2	ADC0

Figure 12-6. Port B Data Register (PTB)

PTB[7:0] — Port B Data Bits

These read/write bits are software programmable. Data direction of each port B pin is under the control of the corresponding bit in data direction register B. Reset has no effect on port B data.

12.5.2 Data Direction Register B (DDRB)

Data direction register B determines whether each port B pin is an input or an output. Writing a logic one to a DDRB bit enables the output buffer for the corresponding port B pin; a logic zero disables the output buffer.

Address: $0005

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDRB7	DDRB6	DDRB5	DDRB4	DDRB3	DDRB2	DDRB1	DDRB0
Reset:	0	0	0	0	0	0	0	0

Figure 12-7. Data Direction Register B (DDRB)

13.5 IRQ Module During Break Interrupts

The system integration module (SIM) controls whether the IRQ1 latch can be cleared during the break state. The BCFE bit in the break flag control register (BFCR) enables software to clear the latches during the break state. (See **Section 7. System Integration Module (SIM)**.)

To allow software to clear the IRQ1 latch during a break interrupt, write a logic one to the BCFE bit. If a latch is cleared during the break state, it remains cleared when the MCU exits the break state.

To protect the latches during the break state, write a logic zero to the BCFE bit. With BCFE at logic zero (its default state), writing to the ACK1 bit in the IRQ status and control register during the break state has no effect on the IRQ latch.

13.6 IRQ Status and Control Register (ISCR)

The IRQ Status and Control Register (ISCR) controls and monitors operation of the IRQ module. The ISCR has the following functions:

- Shows the state of the IRQ1 flag
- Clears the IRQ1 latch
- Masks IRQ1 and interrupt request
- Controls triggering sensitivity of the $\overline{\text{IRQ1}}$ interrupt pin

Address: $001D

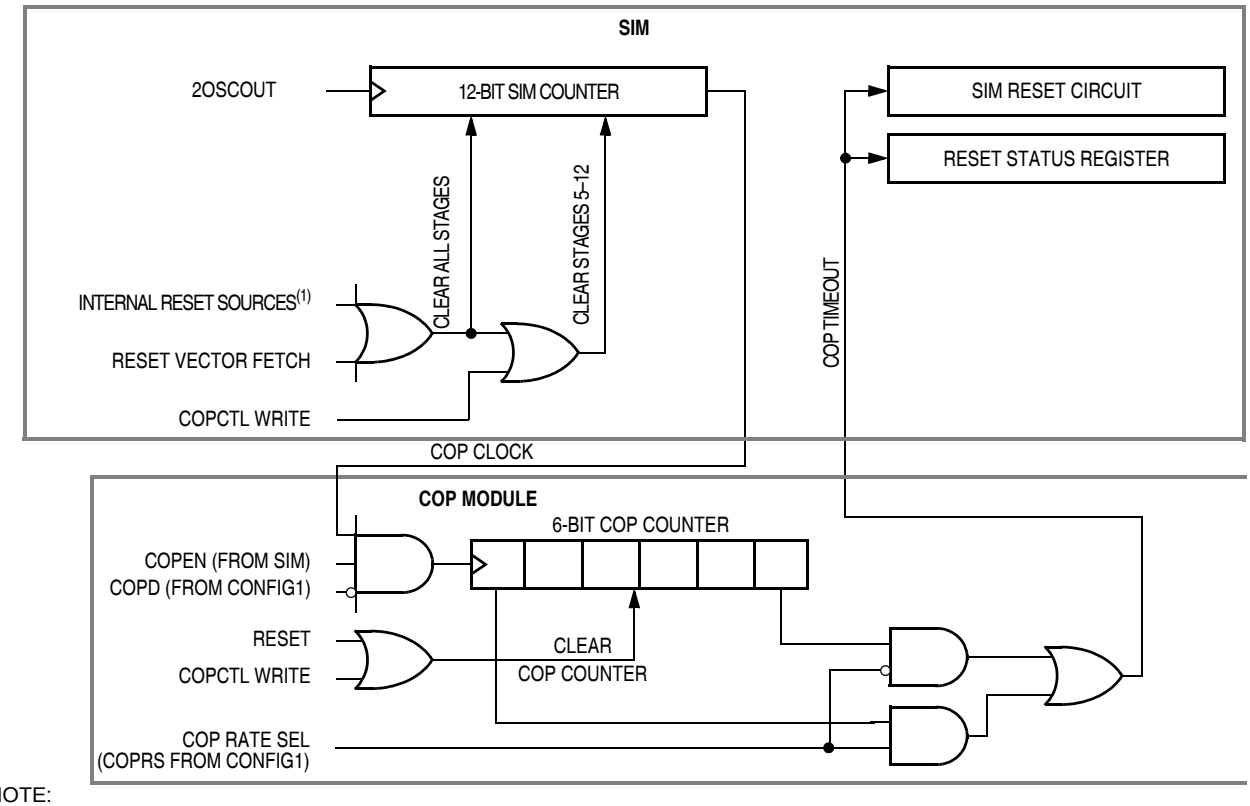
	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	IRQF1		IMASK1	MODE1
Write:						ACK1		
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 13-3. IRQ Status and Control Register (INTSCR)

15.3 Functional Description

Figure 15-1 shows the structure of the COP module.



NOTE:

1. See SIM section for more details.

Figure 15-1. COP Block Diagram

The COP counter is a free-running 6-bit counter preceded by the 12-bit system integration module (SIM) counter. If not cleared by software, the COP counter overflows and generates an asynchronous reset after $2^{18} - 2^4$ or $2^{13} - 2^4$ 2OSCOUT cycles; depending on the state of the COP rate select bit, COPRS, in configuration register 1. With a $2^{18} - 2^4$ 2OSCOUT cycle overflow option, a 8MHz crystal gives a COP timeout period of 32.766 ms. Writing any value to location $FFFF before an overflow occurs prevents a COP reset by clearing the COP counter and stages 12 through 5 of the SIM counter.

17.3 Features

Features of the break module include the following:

- Accessible I/O registers during the break Interrupt
- CPU-generated break interrupts
- Software-generated break interrupts
- COP disabling during break interrupts

17.4 Functional Description

When the internal address bus matches the value written in the break address registers, the break module issues a breakpoint signal ($\overline{\text{BKPT}}$) to the SIM. The SIM then causes the CPU to load the instruction register with a software interrupt instruction (SWI) after completion of the current CPU instruction. The program counter vectors to $FFFC and $FFFD ($FEFC and $FEFD in monitor mode).

The following events can cause a break interrupt to occur:

- A CPU-generated address (the address in the program counter) matches the contents of the break address registers.
- Software writes a logic one to the BRKA bit in the break status and control register.

When a CPU generated address matches the contents of the break address registers, the break interrupt begins after the CPU completes its current instruction. A return from interrupt instruction (RTI) in the break routine ends the break interrupt and returns the MCU to normal operation. **Figure 17-1** shows the structure of the break module.

18.6 5V DC Electrical Characteristics

Table 18-4. DC Electrical Characteristics (5V)

Characteristic[1]	Symbol	Min	Typ[2]	Max	Unit
Output high voltage (I_{LOAD} = –2.0mA) PTA0–PTA6, PTB0–PTB7, PTD0–PTD7	V_{OH}	V_{DD}–0.8	—	—	V
Output low voltage (I_{LOAD} = 1.6mA) PTA6, PTB0–PTB7, PTD0, PTD1, PTD4, PTD5	V_{OL}	—	—	0.4	V
Output low voltage (I_{LOAD} = 25mA) PTD6, PTD7	V_{OL}	—	—	0.5	V
LED drives (V_{OL} = 3V) PTA0–PTA5, PTD2, PTD3, PTD6, PTD7	I_{OL}	10	19	25	mA
Input high voltage PTA0–PTA6, PTB0–PTB7, PTD0–PTD7, $\overline{RST}$, $\overline{IRQ1}$, OSC1	V_{IH}	0.7 × V_{DD}	—	V_{DD}	V
Input low voltage PTA0–PTA6, PTB0–PTB7, PTD0–PTD7, $\overline{RST}$, $\overline{IRQ1}$, OSC1	V_{IL}	V_{SS}	—	0.3 × V_{DD}	V
V_{DD} supply current Run, f_{OP} = 4MHz[3] Wait (MC68HRC908xxx)[4] Wait (MC68HC908xxx)[4] Stop[5] –40°C to 85°C	I_{DD}	— — — —	7 1 5 1	10 1.5 5.5 5	mA mA mA µA
Digital I/O ports Hi-Z leakage current	I_{IL}	—	—	± 10	µA
Input current	I_{IN}	—	—	± 1	µA
Capacitance Ports (as input or output)	C_{OUT} C_{IN}	— —	— —	12 8	pF
POR rearm voltage[6]	V_{POR}	0	—	100	mV
POR rise time ramp rate[7]	R_{POR}	0.035	—	—	V/ms
Monitor mode entry voltage	V_{DD}+V_{HI}	1.5 × V_{DD}	—	8.5	V
Pullup resistors[8] PTD6, PTD7 $\overline{RST}$, $\overline{IRQ1}$, PTA0–PTA6	 R_{PU1} R_{PU2}	 1.8 16	 3.3 26	 4.8 36	 kΩ kΩ
LVI reset voltage	V_{LVR5}	3.6	4.0	4.4	V