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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	HC08
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	LED, LVD, POR, PWM
Number of I/O	14
Program Memory Size	1.5KB (1.5K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.3V
Data Converters	A/D 12x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	20-DIP
Purchase URL	<a href="https://www.e-xfl.com/product-detail/nxp-semiconductors/mchrc908jk1cpe">https://www.e-xfl.com/product-detail/nxp-semiconductors/mchrc908jk1cpe</a>



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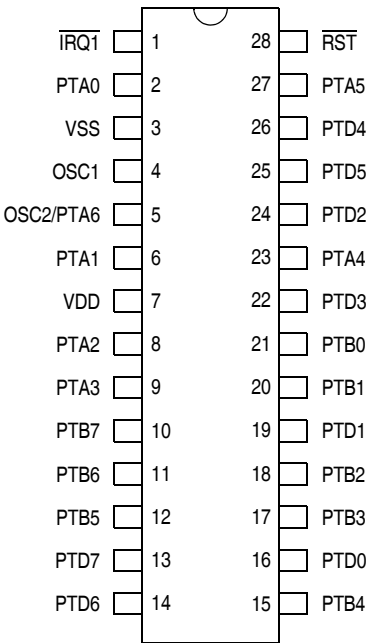
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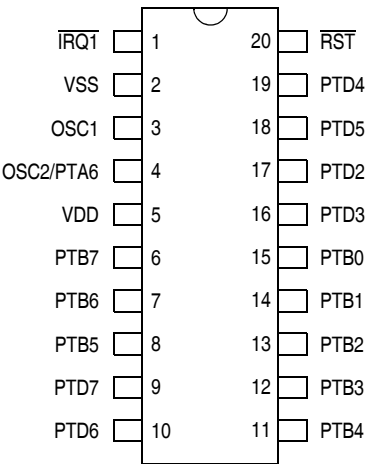
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# 1.5 Pin Assignments

The MC68H(R)C908JL3 is available in 28-pin packages and the MC68H(R)C908JK3/JK1 in 20-pin packages. **Figure 1-2** shows the pin assignment for the two packages.



28-PIN ASSIGNMENT  
MC68H(R)C908JL3



20-PIN ASSIGNMENT  
MC68H(R)C908JK3/JK1

Pins not bonded out on 20-pin package:  
PTA0, PTA1, PTA2, PTA3, PTA4, PTA5,  
PTD0, PTD1.

Figure 1-2. MCU Pin Assignments

- 1 = High voltage enabled to array and charge pump on
- 0 = High voltage disabled to array and charge pump off

#### MASS — Mass Erase Control Bit

This read/write bit configures the memory for mass erase operation or block erase operation when the ERASE bit is set.

- 1 = Mass Erase operation selected
- 0 = Block Erase operation selected

#### ERASE — Erase Control Bit

This read/write bit configures the memory for erase operation. This bit and the PGM bit should not be set to 1 at the same time.

- 1 = Erase operation selected
- 0 = Erase operation not selected

#### PGM — Program Control Bit

This read/write bit configures the memory for program operation. This bit and the ERASE bit should not be set to 1 at the same time.

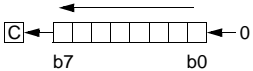
- 1 = Program operation selected
- 0 = Program operation not selected

## 4.5 FLASH Block Erase Operation

Use the following procedure to erase a block of FLASH memory. A block consists of 64 consecutive bytes starting from addresses \$XX00, \$XX40, \$XX80 or \$XXC0. The 48-byte User Interrupt Vectors area also forms a block. Any block within the 4K bytes User Memory area (\$EC00–\$FBFF) can be erased alone. The 48-byte User Interrupt Vector blocks can not be erased alone due to security concern. Mass erase is required to erase this block.

1. Set the ERASE bit and clear the MASS bit in the FLASH Control Register.
2. Write any data to any FLASH location within the address range of the block to be erased.
3. Wait for a time,  $t_{nvs}$  (10 $\mu$ s).
4. Set the HVEN bit.

**Table 6-1. Instruction Set Summary**

Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Cycles
			V	H	I	N	Z	C				
EOR #opr EOR opr EOR opr EOR opr,X EOR opr,X EOR ,X EOR opr,SP EOR opr,SP	Exclusive OR M with A	$A \leftarrow (A \oplus M)$	0	—	—	↑	↑	—	IMM DIR EXT IX2 IX1 IX SP1 SP2	A8 B8 C8 D8 E8 F8 9EE8 9ED8	ii dd hh ll ee ff ff ff ff ff ff	2 3 4 4 3 2 4 5
INC opr INCA INCX INC opr,X INC ,X INC opr,SP INC opr,SP	Increment	$M \leftarrow (M) + 1$ $A \leftarrow (A) + 1$ $X \leftarrow (X) + 1$ $M \leftarrow (M) + 1$ $M \leftarrow (M) + 1$ $M \leftarrow (M) + 1$	↑	—	—	↑	↑	—	DIR INH INH IX1 IX SP1	3C 4C 5C 6C 7C 9E6C	dd ff ff ff ff ff	4 1 1 4 3 5
JMP opr JMP opr JMP opr,X JMP opr,X JMP ,X	Jump	$PC \leftarrow \text{Jump Address}$	—	—	—	—	—	—	DIR EXT IX2 IX1 IX	BC CC DC EC FC	dd hh ll ee ff ff ff	2 3 4 3 2
JSR opr JSR opr JSR opr,X JSR opr,X JSR ,X	Jump to Subroutine	$PC \leftarrow (PC) + n$ ( $n = 1, 2, \text{ or } 3$ ) Push (PCL); $SP \leftarrow (SP) - 1$ Push (PCH); $SP \leftarrow (SP) - 1$ $PC \leftarrow \text{Unconditional Address}$	—	—	—	—	—	—	DIR EXT IX2 IX1 IX	BD CD DD ED FD	dd hh ll ee ff ff ff	4 5 6 5 4
LDA #opr LDA opr LDA opr LDA opr,X LDA opr,X LDA ,X LDA opr,SP LDA opr,SP	Load A from M	$A \leftarrow (M)$	0	—	—	↑	↑	—	IMM DIR EXT IX2 IX1 IX SP1 SP2	A6 B6 C6 D6 E6 F6 9EE6 9ED6	ii dd hh ll ee ff ff ff ff ff	2 3 4 4 3 2 4 5
LDHX #opr LDHX opr	Load H:X from M	$H:X \leftarrow (M:M + 1)$	0	—	—	↑	↑	—	IMM DIR	45 55	ii jj dd	3 4
LDX #opr LDX opr LDX opr LDX opr,X LDX opr,X LDX ,X LDX opr,SP LDX opr,SP	Load X from M	$X \leftarrow (M)$	0	—	—	↑	↑	—	IMM DIR EXT IX2 IX1 IX SP1 SP2	AE BE CE DE EE FE 9EEE 9EDE	ii dd hh ll ee ff ff ff ff ff	2 3 4 4 3 2 4 5
LSL opr LSLA LSLX LSL opr,X LSL ,X LSL opr,SP LSL opr,SP	Logical Shift Left (Same as ASL)		↑	—	—	↑	↑	↑	DIR INH INH IX1 IX SP1	38 48 58 68 78 9E68	dd ff ff ff ff ff	4 1 1 4 3 5



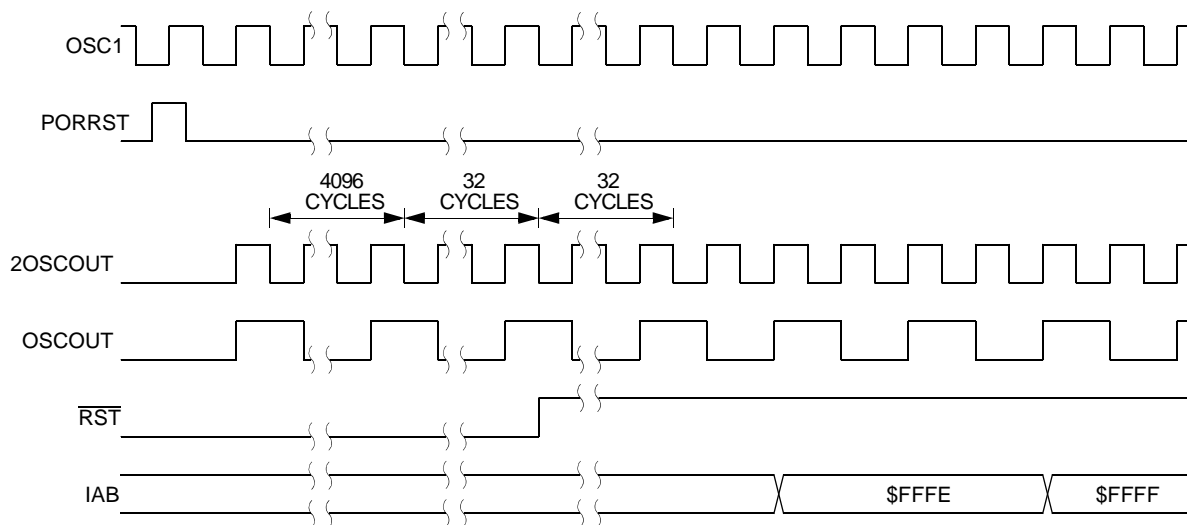
The active reset feature allows the part to issue a reset to peripherals and other chips within a system built around the MCU.

## 7.4.2.1 Power-On Reset

When power is first applied to the MCU, the power-on reset module (POR) generates a pulse to indicate that power-on has occurred. The external reset pin ( $\overline{\text{RST}}$ ) is held low while the SIM counter counts out 4096 2OSCOUT cycles. Sixty-four 2OSCOUT cycles later, the CPU and memories are released from reset to allow the reset vector sequence to occur.

At power-on, the following events occur:

- A POR pulse is generated.
- The internal reset signal is asserted.
- The SIM enables the oscillator to drive 2OSCOUT.
- Internal clocks to the CPU and modules are held inactive for 4096 2OSCOUT cycles to allow stabilization of the oscillator.
- The  $\overline{\text{RST}}$  pin is driven low during the oscillator stabilization time.
- The POR bit of the reset status register (RSR) is set and all other bits in the register are cleared.



**Figure 7-7. POR Recovery**

## 7.4.2.5 LVI Reset

The low-voltage inhibit module (LVI) asserts its output to the SIM when the  $V_{DD}$  voltage falls to the LVI trip voltage  $V_{TRIP}$ . The LVI bit in the SIM reset status register (SRSR) is set, and the external reset pin (RSTB) is held low while the SIM counter counts out 4096 2OSCCLK cycles. Sixty-four 2OSCOOUT cycles later, the CPU and memories are released from reset to allow the reset vector sequence to occur. The SIM actively pulls down the (RSTB) pin for all internal reset sources.

## 7.5 SIM Counter

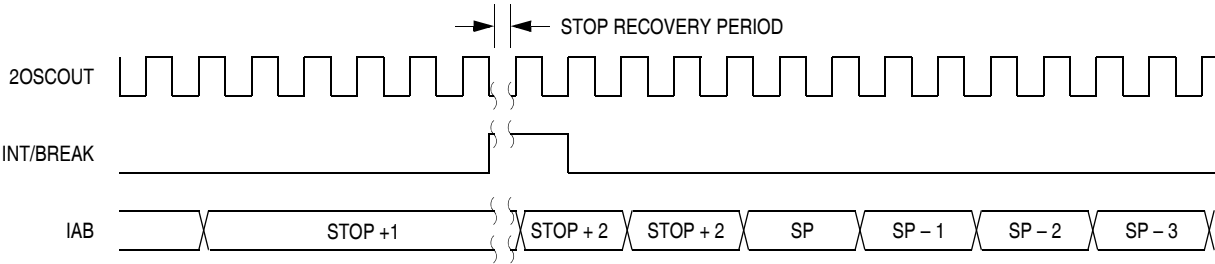
The SIM counter is used by the power-on reset module (POR) and in stop mode recovery to allow the oscillator time to stabilize before enabling the internal bus (IBUS) clocks. The SIM counter also serves as a prescaler for the computer operating properly module (COP). The SIM counter uses 12 stages for counting, followed by a 13th stage that triggers a reset of SIM counters and supplies the clock for the COP module. The SIM counter is clocked by the falling edge of 2OSCOOUT.

### 7.5.1 SIM Counter During Power-On Reset

The power-on reset module (POR) detects power applied to the MCU. At power-on, the POR circuit asserts the signal PORRST. Once the SIM is initialized, it enables the oscillator to drive the bus clock state machine.

### 7.5.2 SIM Counter During Stop Mode Recovery

The SIM counter also is used for stop mode recovery. The STOP instruction clears the SIM counter. After an interrupt, break, or reset, the SIM senses the state of the short stop recovery bit, SSREC, in the mask option register. If the SSREC bit is a logic one, then the stop recovery is reduced from the normal delay of 4096 2OSCOOUT cycles down to 32 2OSCOOUT cycles. This is ideal for applications using canned oscillators that do not require long start-up times from stop mode. External crystal applications should use the full stop recovery time, that is, with SSREC cleared in the configuration register (CONFIG).



**Figure 7-19. Stop Mode Recovery from Interrupt or Break**

## 7.8 SIM Registers

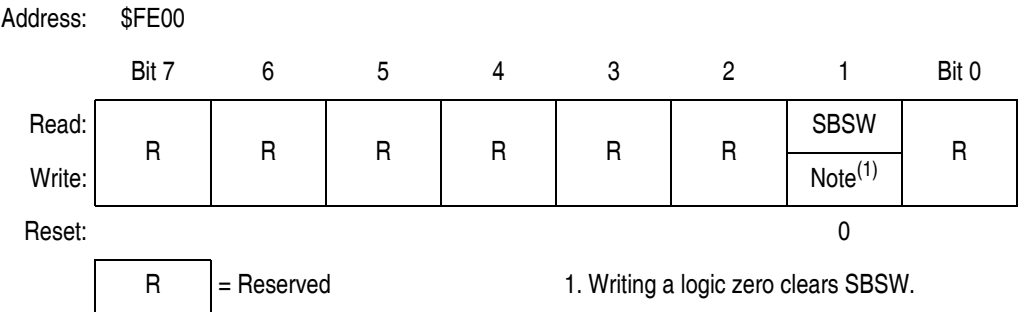
The SIM has three memory mapped registers. **Table 7-4** shows the mapping of these registers.

**Table 7-4. SIM Registers**

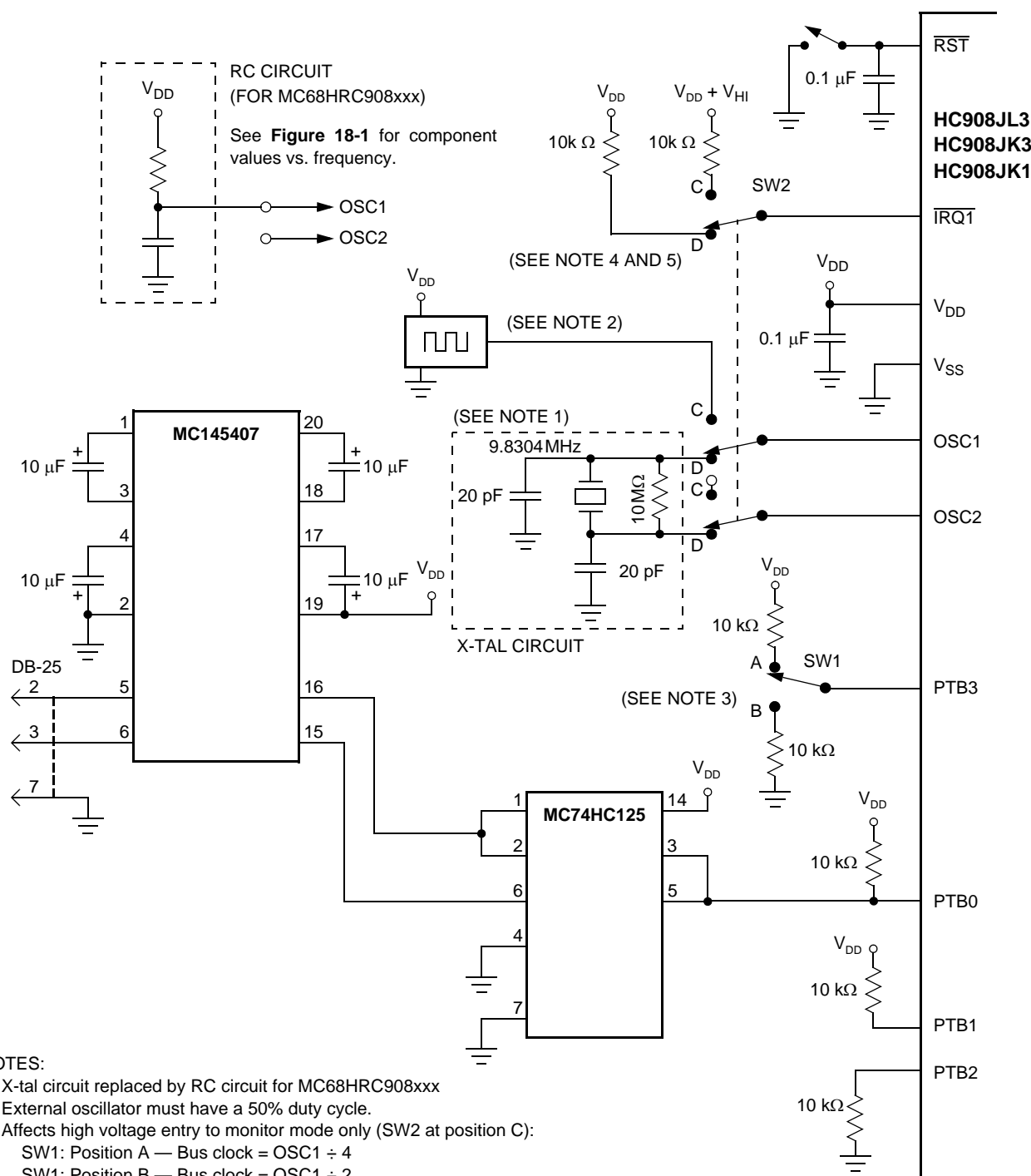
Address	Register	Access Mode
\$FE00	BSR	User
\$FE01	RSR	User
\$FE03	BFCR	User

### 7.8.1 Break Status Register (BSR)

The break status register contains a flag to indicate that a break caused an exit from stop or wait mode.



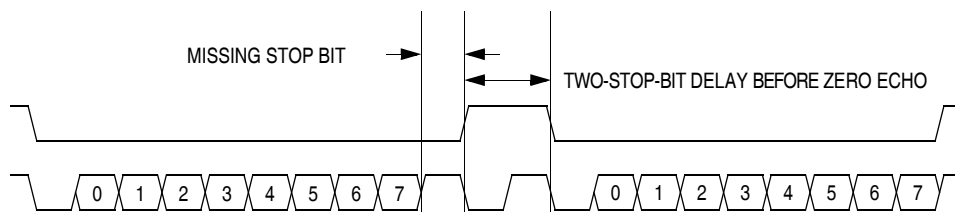
**Figure 7-20. Break Status Register (BSR)**



**Figure 9-1. Monitor Mode Circuit**

### 9.4.5 Break Signal

A start bit followed by nine low bits is a break signal. (See **Figure 9-6.**) When the monitor receives a break signal, it drives the PTB0 pin high for the duration of two bits before echoing the break signal.



**Figure 9-6. Break Transaction**

### 9.4.6 Commands

The monitor ROM uses the following commands:

- READ (read memory)
- WRITE (write memory)
- IREAD (indexed read)
- IWRITE (indexed write)
- READSP (read stack pointer)
- RUN (run user program)

**Table 10-2. Prescaler Selection**

PS2	PS1	PS0	TIM Clock Source
0	0	0	Internal Bus Clock ÷ 1
0	0	1	Internal Bus Clock ÷ 2
0	1	0	Internal Bus Clock ÷ 4
0	1	1	Internal Bus Clock ÷ 8
1	0	0	Internal Bus Clock ÷ 16
1	0	1	Internal Bus Clock ÷ 32
1	1	0	Internal Bus Clock ÷ 64
1	1	1	Not available

### 10.10.2 TIM Counter Registers (TCNTH:TCNTL)

The two read-only TIM counter registers contain the high and low bytes of the value in the TIM counter. Reading the high byte (TCNTH) latches the contents of the low byte (TCNTL) into a buffer. Subsequent reads of TCNTH do not affect the latched TCNTL value until TCNTL is read. Reset clears the TIM counter registers. Setting the TIM reset bit (TRST) also clears the TIM counter registers.

**NOTE:** *If you read TCNTH during a break interrupt, be sure to unlatch TCNTL by reading TCNTL before exiting the break interrupt. Otherwise, TCNTL retains the value latched during the break.*

Writes to the port register or DDR will not have any affect on the port pin that is selected by the ADC. Read of a port pin which is in use by the ADC will return a logic 0 if the corresponding DDR bit is at logic 0. If the DDR bit is at logic 1, the value in the port data latch is read.

## 11.4.2 Voltage Conversion

When the input voltage to the ADC equals  $V_{DD}$ , the ADC converts the signal to \$FF (full scale). If the input voltage equals  $V_{SS}$ , the ADC converts it to \$00. Input voltages between  $V_{DD}$  and  $V_{SS}$  are a straight-line linear conversion. All other input voltages will result in \$FF if greater than  $V_{DD}$  and \$00 if less than  $V_{SS}$ .

**NOTE:** *Input voltage should not exceed the analog supply voltages.*

## 11.4.3 Conversion Time

Sixteen ADC internal clocks are required to perform one conversion. The ADC starts a conversion on the first rising edge of the ADC internal clock immediately following a write to the ADSCR. If the ADC internal clock is selected to run at 1 MHz, then one conversion will take 16 $\mu$ s to complete. With a 1 MHz ADC internal clock the maximum sample rate is 62.5kHz.

$$\text{Conversion Time} = \frac{16 \text{ ADC Clock Cycles}}{\text{ADC Clock Frequency}}$$

$$\text{Number of Bus Cycles} = \text{Conversion Time} \times \text{Bus Frequency}$$

## 11.4.4 Continuous Conversion

In the continuous conversion mode, the ADC continuously converts the selected channel filling the ADC data register with new data after each conversion. Data from the previous conversion will be overwritten whether that data has been read or not. Conversions will continue until the ADCO bit is cleared. The COCO bit (ADC Status & Control register, \$003C) is set after each conversion and can be cleared by writing the ADC status and control register or reading of the ADC data register.

### 11.4.5 Accuracy and Precision

The conversion process is monotonic and has no missing codes.

## 11.5 Interrupts

When the AIEN bit is set, the ADC module is capable of generating a CPU interrupt after each ADC conversion. A CPU interrupt is generated if the COCO bit is at logic 0. The COCO bit is not used as a conversion complete flag when interrupts are enabled.

## 11.6 Low-Power Modes

The following subsections describe the ADC in low-power modes.

### 11.6.1 Wait Mode

The ADC continues normal operation during wait mode. Any enabled CPU interrupt request from the ADC can bring the MCU out of wait mode. If the ADC is not required to bring the MCU out of wait mode, power down the ADC by setting the CH[4:0] bits in the ADC Status and Control register to logic 1's before executing the WAIT instruction.

### 11.6.2 Stop Mode

The ADC module is inactive after the execution of a STOP instruction. Any pending conversion is aborted. ADC conversions resume when the MCU exits stop mode. Allow one conversion cycle to stabilize the analog circuitry before attempting a new ADC conversion after exiting stop mode.

## 11.7 I/O Signals

The ADC module has 12 channels that are shared with I/O port B and port D.



## Section 12. I/O Ports

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### 12.2 Introduction

Twenty three bidirectional input-output (I/O) pins form three parallel ports. All I/O pins are programmable as inputs or outputs.

**NOTE:** *Connect any unused I/O pins to an appropriate logic level, either  $V_{DD}$  or  $V_{SS}$ . Although the I/O ports do not require termination for proper operation, termination reduces excess current consumption and the possibility of electrostatic damage.*



## 14.5 Wait Mode

The keyboard modules remain active in wait mode. Clearing the IMASKK bit in the keyboard status and control register enables keyboard interrupt requests to bring the MCU out of wait mode.

## 14.6 Stop Mode

The keyboard module remains active in stop mode. Clearing the IMASKK bit in the keyboard status and control register enables keyboard interrupt requests to bring the MCU out of stop mode.

## 14.7 Keyboard Module During Break Interrupts

The system integration module (SIM) controls whether the keyboard interrupt latch can be cleared during the break state. The BCFE bit in the break flag control register (BFCR) enables software to clear status bits during the break state.

To allow software to clear the keyboard interrupt latch during a break interrupt, write a logic 1 to the BCFE bit. If a latch is cleared during the break state, it remains cleared when the MCU exits the break state.

To protect the latch during the break state, write a logic 0 to the BCFE bit. With BCFE at logic 0 (its default state), writing to the keyboard acknowledge bit (ACKK) in the keyboard status and control register during the break state has no effect.

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### 18.2 Introduction

This section contains electrical and timing specifications.

## 18.14 Memory Characteristics

**Table 18-11. Memory Characteristics**

Characteristic	Symbol	Min	Max	Unit
RAM data retention voltage	$V_{RDR}$	1.3	—	V
FLASH program bus clock frequency	—	1	—	MHz
FLASH read bus clock frequency	$f_{Read}^{(1)}$	32k	8M	Hz
FLASH page erase time	$t_{Erase}^{(2)}$	1	—	ms
FLASH mass erase time	$t_{MErase}^{(3)}$	4	—	ms
FLASH PGM/ERASE to HVEN set up time	$t_{nvs}$	10	—	$\mu s$
FLASH high-voltage hold time	$t_{nvh}$	5	—	$\mu s$
FLASH high-voltage hold time (mass erase)	$t_{nvhl}$	100	—	$\mu s$
FLASH program hold time	$t_{pgs}$	5	—	$\mu s$
FLASH program time	$t_{PROG}$	30	40	$\mu s$
FLASH return to read time	$t_{rcv}^{(4)}$	1	—	$\mu s$
FLASH cumulative program hv period	$t_{HV}^{(5)}$	—	4	ms
FLASH row erase endurance <sup>(6)</sup>	—	10k	—	cycles
FLASH row program endurance <sup>(7)</sup>	—	10k	—	cycles
FLASH data retention time <sup>(8)</sup>	—	10	—	years

**NOTES:**

- $f_{Read}$  is defined as the frequency range for which the FLASH memory can be read.
- If the page erase time is longer than  $t_{Erase}$  (Min), there is no erase-disturb, but it reduces the endurance of the FLASH memory.
- If the mass erase time is longer than  $t_{MErase}$  (Min), there is no erase-disturb, but it reduces the endurance of the FLASH memory.
- $t_{rcv}$  is defined as the time it needs before the FLASH can be read after turning off the high voltage charge pump, by clearing HVEN to logic 0.
- $t_{HV}$  is defined as the cumulative high voltage programming time to the same row before next erase.  
 $t_{HV}$  must satisfy this condition:  $t_{nvs} + t_{nvh} + t_{pgs} + (t_{PROG} \times 32) \leq t_{HV} \text{ max.}$
- The minimum row endurance value specifies each row of the FLASH memory is guaranteed to work for at least this many erase / program cycles.
- The minimum row endurance value specifies each row of the FLASH memory is guaranteed to work for at least this many erase / program cycles.
- The FLASH is guaranteed to retain data over the entire operating temperature range for at least the minimum time specified.