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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	HC08
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	LED, LVD, POR, PWM
Number of I/O	15
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.3V
Data Converters	A/D 12x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOIC
Purchase URL	<a href="https://www.e-xfl.com/product-detail/nxp-semiconductors/mcr98jk3ecdwe">https://www.e-xfl.com/product-detail/nxp-semiconductors/mcr98jk3ecdwe</a>



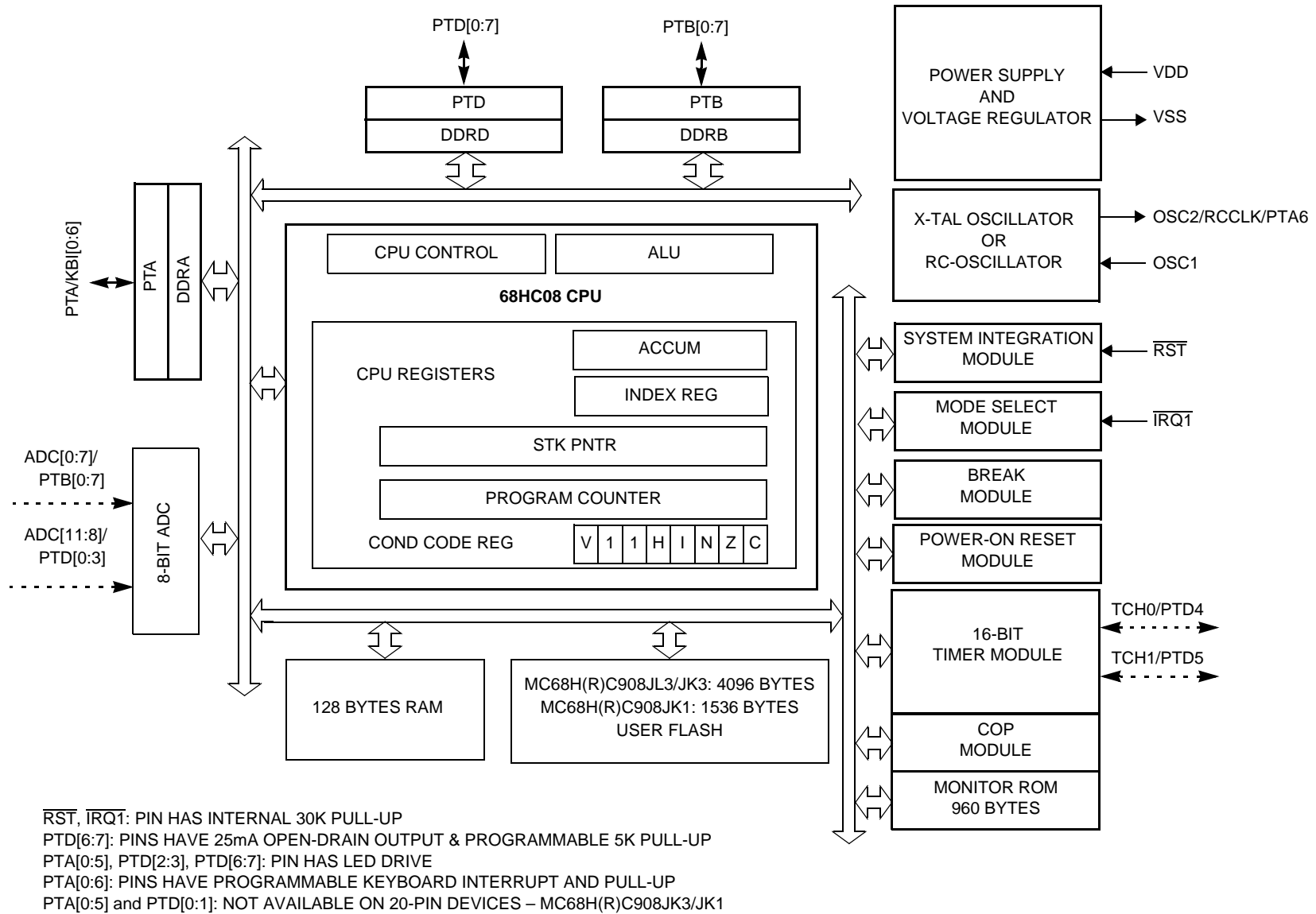


Figure 1-1. MCU Block Diagram

## 1.6 Pin Functions

Description of the pin functions are provided in **Table 1-2**.

**Table 1-2. Pin Functions**

PIN NAME	PIN DESCRIPTION	IN/OUT	VOLTAGE LEVEL
VDD	Power supply.	In	5V or 3V
VSS	Power supply ground	Out	0V
$\overline{\text{RST}}$	RESET input, active low. With Internal pull-up and schmitt trigger input.	Input	VDD
$\overline{\text{IRQ1}}$	External IRQ pin. With software programmable internal pull-up and schmitt trigger input. This pin is also used for mode entry selection.	Input	VDD to VDD+V <sub>HI</sub>
OSC1	X-tal or RC oscillator input.	In	Analog
OSC2	For X-tal oscillator option: X-tal oscillator output, this is the inverting OSC1 signal.	Out	Analog
	For RC oscillator option: Default is RCCLK output. Shared with PTA6/KBI6, with programmable pull-up.	In/Out	VDD
PTA[0:6]	7-bit general purpose I/O port.	In/Out	VDD
	Shared with 7 keyboard interrupts KBI[0:6].	In	VDD
	Each pin has programmable internal pull-up device.	In	VDD
PTB[0:7]	8-bit general purpose I/O port.	In/Out	VDD
	Shared with 8 ADC inputs, ADC[0:7].	In	Analog
PTD[0:7]	8-bit general purpose I/O port.	In/Out	VDD
	PTD[3:0] shared with 4 ADC inputs, ADC[8:11].	Input	Analog
	PTD[4:5] shared with TIM channels, TCH0 and TCH1.	In/Out	VDD
	PTD[6:7] can be configured as 25mA open-drain output with pull-up.	In/Out	VDD

**NOTE:** On the 20-pin package, the following pins are not available:  
PTA0, PTA1, PTA2, PTA3, PTA4, PTA5, PTD0, and PTD1.

- 1 = High voltage enabled to array and charge pump on
- 0 = High voltage disabled to array and charge pump off

#### MASS — Mass Erase Control Bit

This read/write bit configures the memory for mass erase operation or block erase operation when the ERASE bit is set.

- 1 = Mass Erase operation selected
- 0 = Block Erase operation selected

#### ERASE — Erase Control Bit

This read/write bit configures the memory for erase operation. This bit and the PGM bit should not be set to 1 at the same time.

- 1 = Erase operation selected
- 0 = Erase operation not selected

#### PGM — Program Control Bit

This read/write bit configures the memory for program operation. This bit and the ERASE bit should not be set to 1 at the same time.

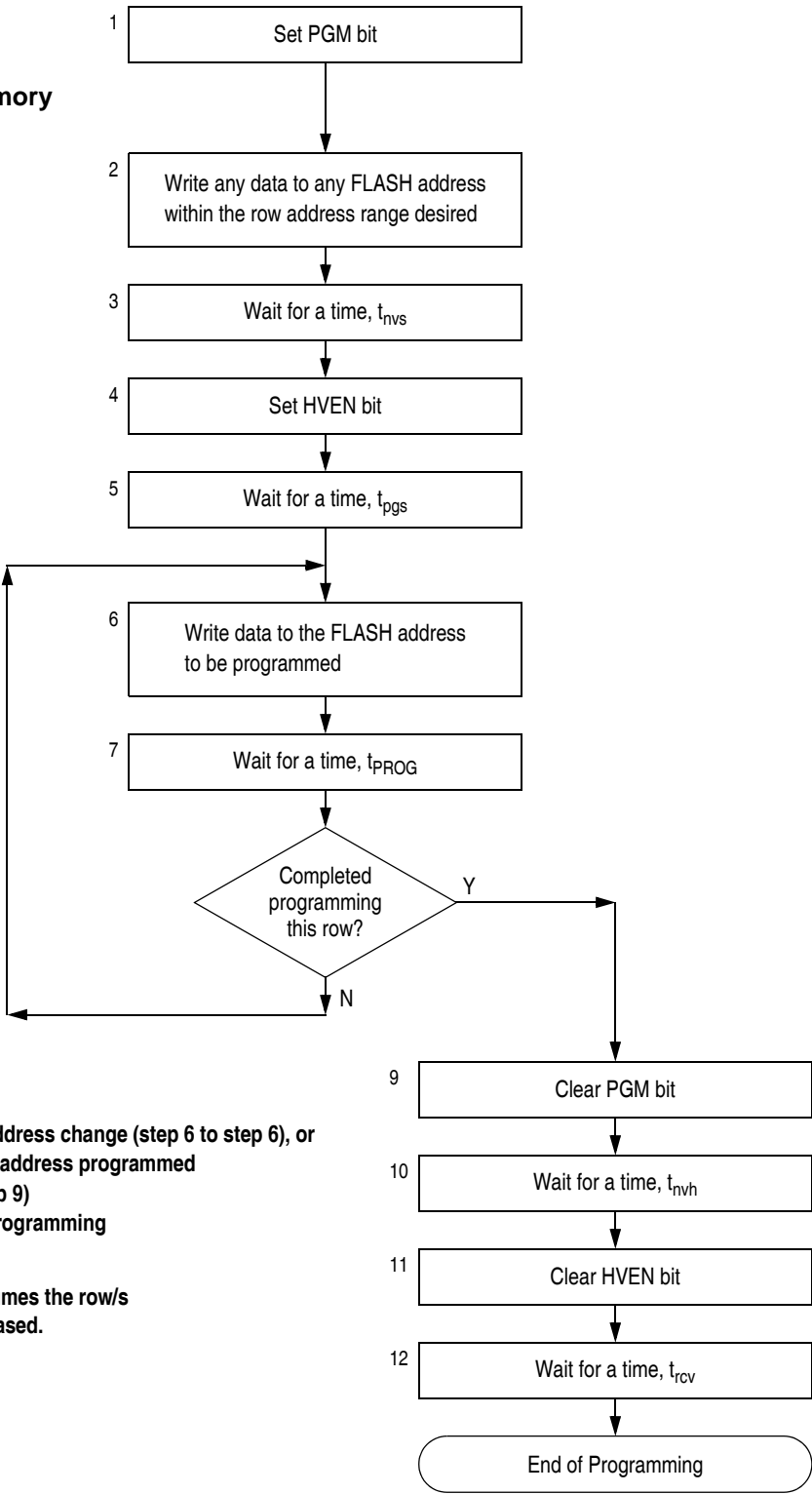
- 1 = Program operation selected
- 0 = Program operation not selected

## 4.5 FLASH Block Erase Operation

Use the following procedure to erase a block of FLASH memory. A block consists of 64 consecutive bytes starting from addresses \$XX00, \$XX40, \$XX80 or \$XXC0. The 48-byte User Interrupt Vectors area also forms a block. Any block within the 4K bytes User Memory area (\$EC00–\$FBFF) can be erased alone. The 48-byte User Interrupt Vector blocks can not be erased alone due to security concern. Mass erase is required to erase this block.

1. Set the ERASE bit and clear the MASS bit in the FLASH Control Register.
2. Write any data to any FLASH location within the address range of the block to be erased.
3. Wait for a time,  $t_{nvs}$  (10 $\mu$ s).
4. Set the HVEN bit.

Algorithm for programming  
a row (32 bytes) of FLASH memory



**NOTE:**  
 The time between each FLASH address change (step 6 to step 6), or the time between the last FLASH address programmed to clearing PGM bit (step 6 to step 9) must not exceed the maximum programming time,  $t_{PROG\ max}$ .  
 This row program algorithm assumes the row/s to be programmed are initially erased.

Figure 4-2. FLASH Programming Flowchart

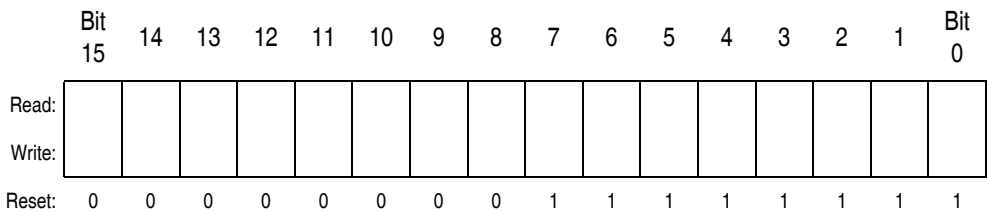


Figure 6-4. Stack Pointer (SP)

**NOTE:** The location of the stack is arbitrary and may be relocated anywhere in RAM. Moving the SP out of page 0 (\$0000 to \$00FF) frees direct address (page 0) space. For correct operation, the stack pointer must point only to RAM locations.

6.4.4 Program Counter

The program counter is a 16-bit register that contains the address of the next instruction or operand to be fetched.

Normally, the program counter automatically increments to the next sequential memory location every time an instruction or operand is fetched. Jump, branch, and interrupt operations load the program counter with an address other than that of the next sequential location.

During reset, the program counter is loaded with the reset vector address located at \$FFFE and \$FFFF. The vector address is the address of the first instruction to be executed after exiting the reset state.

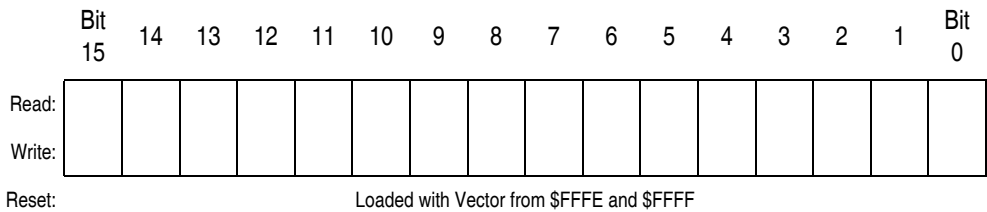


Figure 6-5. Program Counter (PC)

6.4.5 Condition Code Register

The 8-bit condition code register contains the interrupt mask and five flags that indicate the results of the instruction just executed. Bits 6 and

In wait mode, the CPU clocks are inactive. The SIM also produces two sets of clocks for other modules. Refer to the wait mode subsection of each module to see if the module is active or inactive in wait mode. Some modules can be programmed to be active in wait mode.

## 7.4 Reset and System Initialization

The MCU has these reset sources:

- Power-on reset module (POR)
- External reset pin ( $\overline{RST}$ )
- Computer operating properly module (COP)
- Low-voltage inhibit module (LVI)
- Illegal opcode
- Illegal address

All of these resets produce the vector \$FFFE–FFFF (\$FEFE–FEFF in Monitor mode) and assert the internal reset signal (IRST). IRST causes all registers to be returned to their default values and all modules to be returned to their reset states.

An internal reset clears the SIM counter (see **7.5 SIM Counter**), but an external reset does not. Each of the resets sets a corresponding bit in the reset status register (RSR). (See **7.8 SIM Registers**.)

### 7.4.1 External Pin Reset

The  $\overline{RST}$  pin circuits include an internal pull-up device. Pulling the asynchronous  $\overline{RST}$  pin low halts all processing. The PIN bit of the reset status register (RSR) is set as long as  $\overline{RST}$  is held low for a minimum of 67 2OSCCLK cycles, assuming that the POR was not the source of the reset. See **Table 7-2** for details. **Figure 7-4** shows the relative timing.

**Table 7-2. PIN Bit Set Timing**

Reset Type	Number of Cycles Required to Set PIN
POR	4163 (4096 + 64 + 3)
All others	67 (64 + 3)



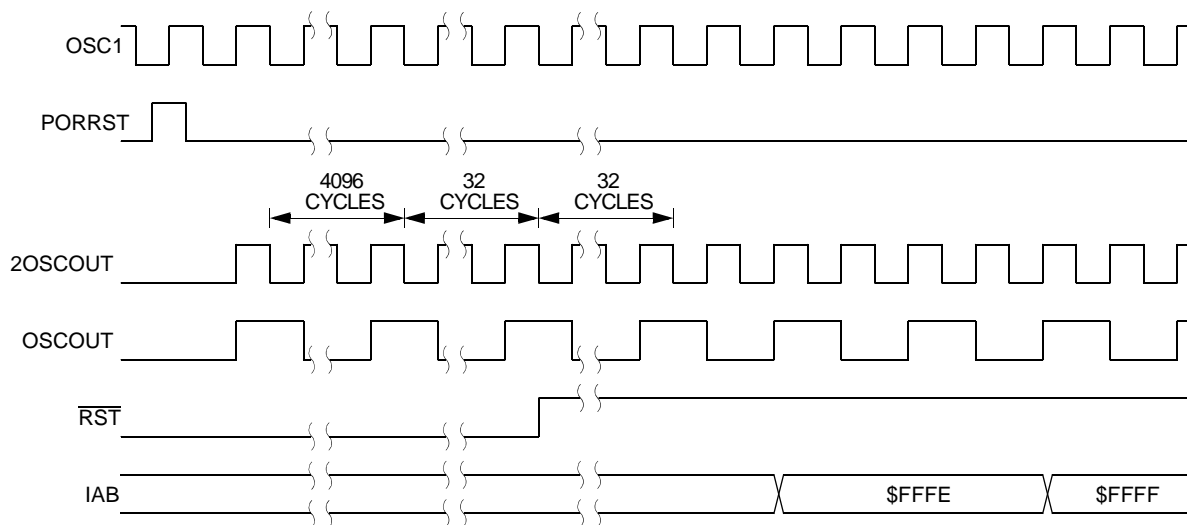
The active reset feature allows the part to issue a reset to peripherals and other chips within a system built around the MCU.

## 7.4.2.1 Power-On Reset

When power is first applied to the MCU, the power-on reset module (POR) generates a pulse to indicate that power-on has occurred. The external reset pin ( $\overline{\text{RST}}$ ) is held low while the SIM counter counts out 4096 2OSCOUT cycles. Sixty-four 2OSCOUT cycles later, the CPU and memories are released from reset to allow the reset vector sequence to occur.

At power-on, the following events occur:

- A POR pulse is generated.
- The internal reset signal is asserted.
- The SIM enables the oscillator to drive 2OSCOUT.
- Internal clocks to the CPU and modules are held inactive for 4096 2OSCOUT cycles to allow stabilization of the oscillator.
- The  $\overline{\text{RST}}$  pin is driven low during the oscillator stabilization time.
- The POR bit of the reset status register (RSR) is set and all other bits in the register are cleared.



**Figure 7-7. POR Recovery**

## 7.4.2.5 LVI Reset

The low-voltage inhibit module (LVI) asserts its output to the SIM when the  $V_{DD}$  voltage falls to the LVI trip voltage  $V_{TRIP}$ . The LVI bit in the SIM reset status register (SRSR) is set, and the external reset pin (RSTB) is held low while the SIM counter counts out 4096 2OSCCLK cycles. Sixty-four 2OSCOOUT cycles later, the CPU and memories are released from reset to allow the reset vector sequence to occur. The SIM actively pulls down the (RSTB) pin for all internal reset sources.

## 7.5 SIM Counter

The SIM counter is used by the power-on reset module (POR) and in stop mode recovery to allow the oscillator time to stabilize before enabling the internal bus (IBUS) clocks. The SIM counter also serves as a prescaler for the computer operating properly module (COP). The SIM counter uses 12 stages for counting, followed by a 13th stage that triggers a reset of SIM counters and supplies the clock for the COP module. The SIM counter is clocked by the falling edge of 2OSCOOUT.

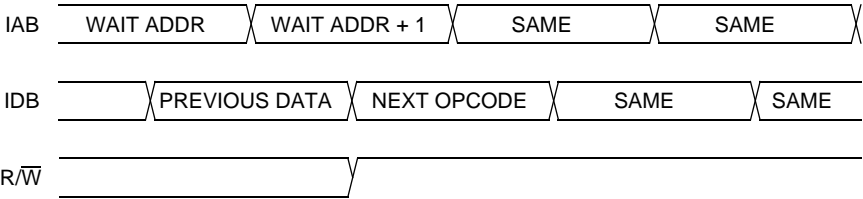
### 7.5.1 SIM Counter During Power-On Reset

The power-on reset module (POR) detects power applied to the MCU. At power-on, the POR circuit asserts the signal PORRST. Once the SIM is initialized, it enables the oscillator to drive the bus clock state machine.

### 7.5.2 SIM Counter During Stop Mode Recovery

The SIM counter also is used for stop mode recovery. The STOP instruction clears the SIM counter. After an interrupt, break, or reset, the SIM senses the state of the short stop recovery bit, SSREC, in the mask option register. If the SSREC bit is a logic one, then the stop recovery is reduced from the normal delay of 4096 2OSCOOUT cycles down to 32 2OSCOOUT cycles. This is ideal for applications using canned oscillators that do not require long start-up times from stop mode. External crystal applications should use the full stop recovery time, that is, with SSREC cleared in the configuration register (CONFIG).

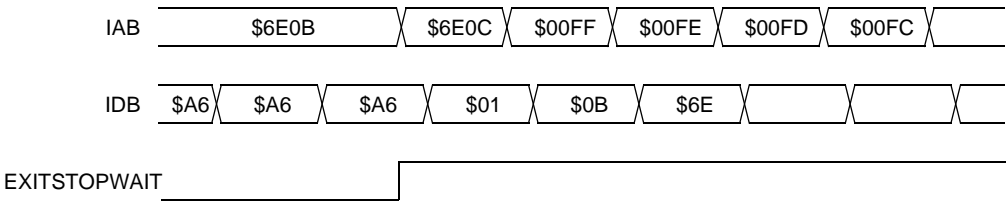
status register (BSR). If the COP disable bit, COPD, in the mask option register is logic zero, then the computer operating properly module (COP) is enabled and remains active in wait mode.



NOTE: Previous data can be operand data or the WAIT opcode, depending on the last instruction.

Figure 7-15. Wait Mode Entry Timing

Figure 7-16 and Figure 7-17 show the timing for WAIT recovery.



NOTE: EXITSTOPWAIT =  $\overline{\text{RST}}$  pin OR CPU interrupt OR break interrupt

Figure 7-16. Wait Recovery from Interrupt or Break

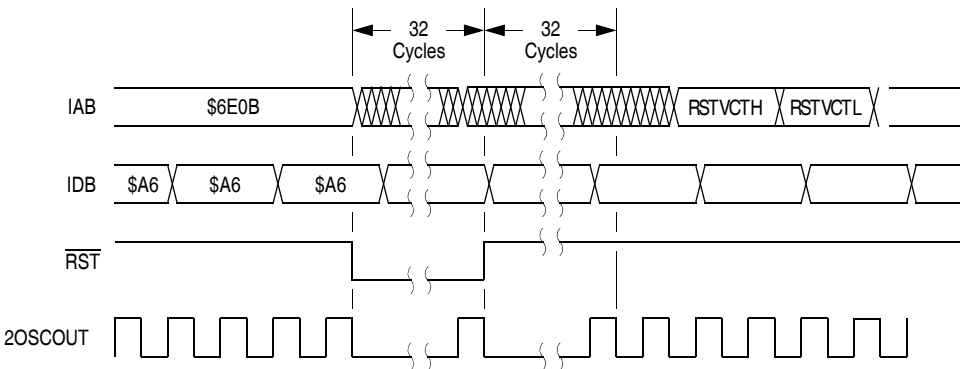


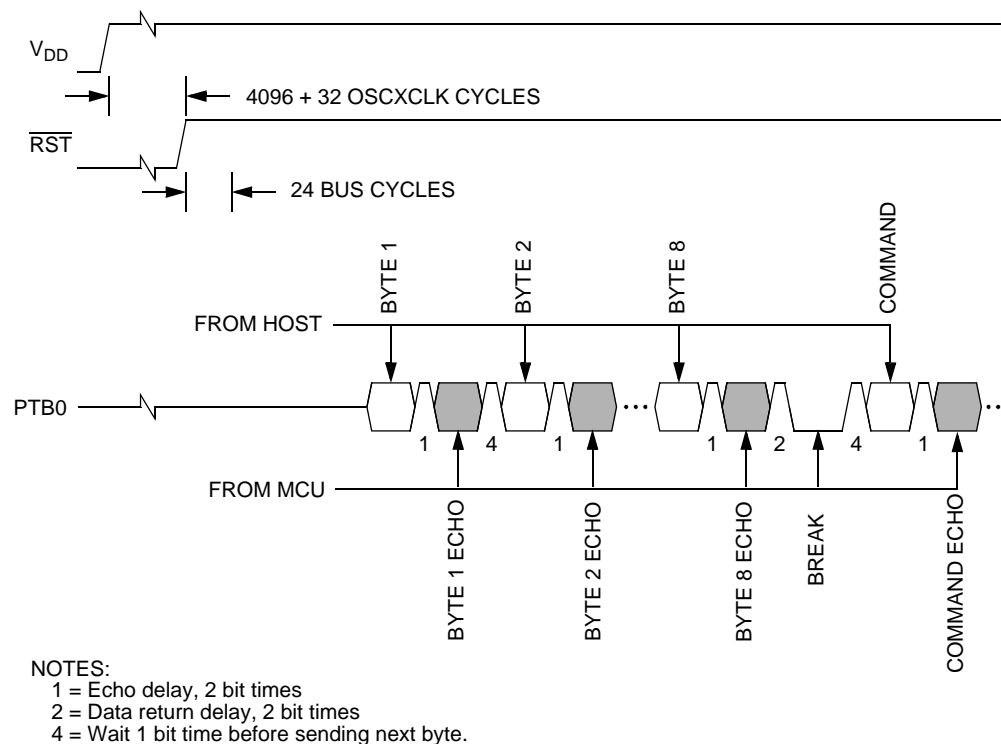
Figure 7-17. Wait Recovery from Internal Reset

## 9.5 Security

A security feature discourages unauthorized reading of FLASH locations while in monitor mode. The host can bypass the security feature at monitor mode entry by sending eight security bytes that match the bytes at locations \$FFF6–\$FFFD. Locations \$FFF6–\$FFFD contain user-defined data.

**NOTE:** Do not leave locations \$FFF6–\$FFFD blank. For security reasons, program locations \$FFF6–\$FFFD even if they are not used for vectors.

During monitor mode entry, the MCU waits after the power-on reset for the host to send the eight security bytes on pin PTB0. If the received bytes match those at locations \$FFF6–\$FFFD, the host bypasses the security feature and can read all FLASH locations and execute code from FLASH. Security remains bypassed until a power-on reset occurs. If the reset was not a power-on reset, security remains bypassed and security code entry is not required. (See **Figure 9-7.**)



**Figure 9-7. Monitor Mode Entry Timing**

\$0029	TIM Channel 1 Register High (TCH1H)	Read:	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	
		Write:									
		Reset:	Indeterminate after reset								
\$002A	TIM Channel 1 Register Low (TCH1L)	Read:	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
		Write:									
		Reset:	Indeterminate after reset								
			= Unimplemented								

**Figure 10-2. TIM I/O Register Summary**

### 10.5.1 TIM Counter Prescaler

The TIM clock source is one of the seven prescaler outputs. The prescaler generates seven clock rates from the internal bus clock. The prescaler select bits, PS[2:0], in the TIM status and control register (TSC) select the TIM clock source.

### 10.5.2 Input Capture

With the input capture function, the TIM can capture the time at which an external event occurs. When an active edge occurs on the pin of an input capture channel, the TIM latches the contents of the TIM counter into the TIM channel registers, TCHxH:TCHxL. The polarity of the active edge is programmable. Input captures can generate TIM CPU interrupt requests.

### 10.5.3 Output Compare

With the output compare function, the TIM can generate a periodic pulse with a programmable polarity, duration, and frequency. When the counter reaches the value in the registers of an output compare channel, the TIM can set, clear, or toggle the channel pin. Output compares can generate TIM CPU interrupt requests.

**Table 10-2. Prescaler Selection**

PS2	PS1	PS0	TIM Clock Source
0	0	0	Internal Bus Clock ÷ 1
0	0	1	Internal Bus Clock ÷ 2
0	1	0	Internal Bus Clock ÷ 4
0	1	1	Internal Bus Clock ÷ 8
1	0	0	Internal Bus Clock ÷ 16
1	0	1	Internal Bus Clock ÷ 32
1	1	0	Internal Bus Clock ÷ 64
1	1	1	Not available

### 10.10.2 TIM Counter Registers (TCNTH:TCNTL)

The two read-only TIM counter registers contain the high and low bytes of the value in the TIM counter. Reading the high byte (TCNTH) latches the contents of the low byte (TCNTL) into a buffer. Subsequent reads of TCNTH do not affect the latched TCNTL value until TCNTL is read. Reset clears the TIM counter registers. Setting the TIM reset bit (TRST) also clears the TIM counter registers.

**NOTE:** *If you read TCNTH during a break interrupt, be sure to unlatch TCNTL by reading TCNTL before exiting the break interrupt. Otherwise, TCNTL retains the value latched during the break.*

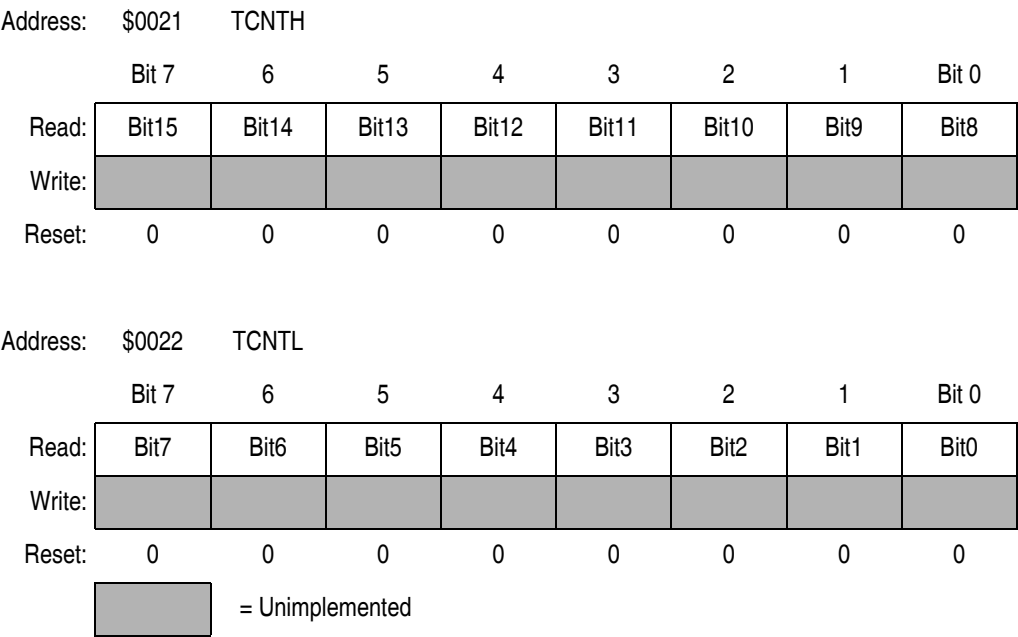


Figure 10-5. TIM Counter Registers (TCNTH:TCNTL)

10.10.3 TIM Counter Modulo Registers (TMODH:TMODL)

The read/write TIM modulo registers contain the modulo value for the TIM counter. When the TIM counter reaches the modulo value, the overflow flag (TOF) becomes set, and the TIM counter resumes counting from \$0000 at the next clock. Writing to the high byte (TMODH) inhibits the TOF bit and overflow interrupts until the low byte (TMODL) is written. Reset sets the TIM counter modulo registers.

### MSxB — Mode Select Bit B

This read/write bit selects buffered output compare/PWM operation. MSxB exists only in the TIM channel 0 status and control register.

Setting MS0B disables the channel 1 status and control register and reverts TCH1 to general-purpose I/O.

Reset clears the MSxB bit.

- 1 = Buffered output compare/PWM operation enabled
- 0 = Buffered output compare/PWM operation disabled

### MSxA — Mode Select Bit A

When ELSxB:A  $\neq$  00, this read/write bit selects either input capture operation or unbuffered output compare/PWM operation.

See **Table 10-3**.

- 1 = Unbuffered output compare/PWM operation
- 0 = Input capture operation

When ELSxB:A = 00, this read/write bit selects the initial output level of the TCHx pin. (See **Table 10-3**.) Reset clears the MSxA bit.

- 1 = Initial output level low
- 0 = Initial output level high

**NOTE:** Before changing a channel function by writing to the MSxB or MSxA bit, set the TSTOP and TRST bits in the TIM status and control register (TSC).

### ELSxB and ELSxA — Edge/Level Select Bits

When channel x is an input capture channel, these read/write bits control the active edge-sensing logic on channel x.

When channel x is an output compare channel, ELSxB and ELSxA control the channel x output behavior when an output compare occurs.

When ELSxB and ELSxA are both clear, channel x is not connected to an I/O port, and pin TCHx is available as a general-purpose I/O pin.

**Table 10-3** shows how ELSxB and ELSxA work. Reset clears the ELSxB and ELSxA bits.



Writes to the port register or DDR will not have any affect on the port pin that is selected by the ADC. Read of a port pin which is in use by the ADC will return a logic 0 if the corresponding DDR bit is at logic 0. If the DDR bit is at logic 1, the value in the port data latch is read.

## 11.4.2 Voltage Conversion

When the input voltage to the ADC equals  $V_{DD}$ , the ADC converts the signal to \$FF (full scale). If the input voltage equals  $V_{SS}$ , the ADC converts it to \$00. Input voltages between  $V_{DD}$  and  $V_{SS}$  are a straight-line linear conversion. All other input voltages will result in \$FF if greater than  $V_{DD}$  and \$00 if less than  $V_{SS}$ .

**NOTE:** *Input voltage should not exceed the analog supply voltages.*

## 11.4.3 Conversion Time

Sixteen ADC internal clocks are required to perform one conversion. The ADC starts a conversion on the first rising edge of the ADC internal clock immediately following a write to the ADSCR. If the ADC internal clock is selected to run at 1 MHz, then one conversion will take 16 $\mu$ s to complete. With a 1 MHz ADC internal clock the maximum sample rate is 62.5kHz.

$$\text{Conversion Time} = \frac{16 \text{ ADC Clock Cycles}}{\text{ADC Clock Frequency}}$$

$$\text{Number of Bus Cycles} = \text{Conversion Time} \times \text{Bus Frequency}$$

## 11.4.4 Continuous Conversion

In the continuous conversion mode, the ADC continuously converts the selected channel filling the ADC data register with new data after each conversion. Data from the previous conversion will be overwritten whether that data has been read or not. Conversions will continue until the ADCO bit is cleared. The COCO bit (ADC Status & Control register, \$003C) is set after each conversion and can be cleared by writing the ADC status and control register or reading of the ADC data register.



### 12.4.2 Port A Input Pull-up Enable Register (PTAPUE)

The Port A Input Pull-up Enable Register (PTAPUE) contains a software configurable pull-up device for each of the seven port A pins. Each bit is individually configurable and requires the corresponding data direction register, DDRAx be configured as input. Each pull-up device is automatically and dynamically disabled when its corresponding DDRAx bit is configured as output.

**NOTE:** *Service the COP immediately after reset and before entering or after exiting stop mode to guarantee the maximum time before the first COP counter overflow.*

A COP reset pulls the  $\overline{\text{RST}}$  pin low for  $32 \times 2\text{OSCOUT}$  cycles and sets the COP bit in the reset status register (RSR). (See **7.8.2 Reset Status Register (RSR)**).

**NOTE:** *Place COP clearing instructions in the main program and not in an interrupt subroutine. Such an interrupt subroutine could keep the COP from generating a reset even while the main program is not working properly.*

## 15.4 I/O Signals

The following paragraphs describe the signals shown in **Figure 15-1**.

### 15.4.1 2OSCOUT

2OSCOUT is the oscillator output signal. 2OSCOUT frequency is equal to the crystal frequency or the RC-oscillator frequency.

### 15.4.2 COPCTL Write

Writing any value to the COP control register (COPCTL) (see **15.5 COP Control Register**) clears the COP counter and clears bits 12 through 5 of the SIM counter. Reading the COP control register returns the low byte of the reset vector.

### 15.4.3 Power-On Reset

The power-on reset (POR) circuit in the SIM clears the SIM counter  $4096 \times 2\text{OSCOUT}$  cycles after power-up.

### 15.4.4 Internal Reset

An internal reset clears the SIM counter and the COP counter.

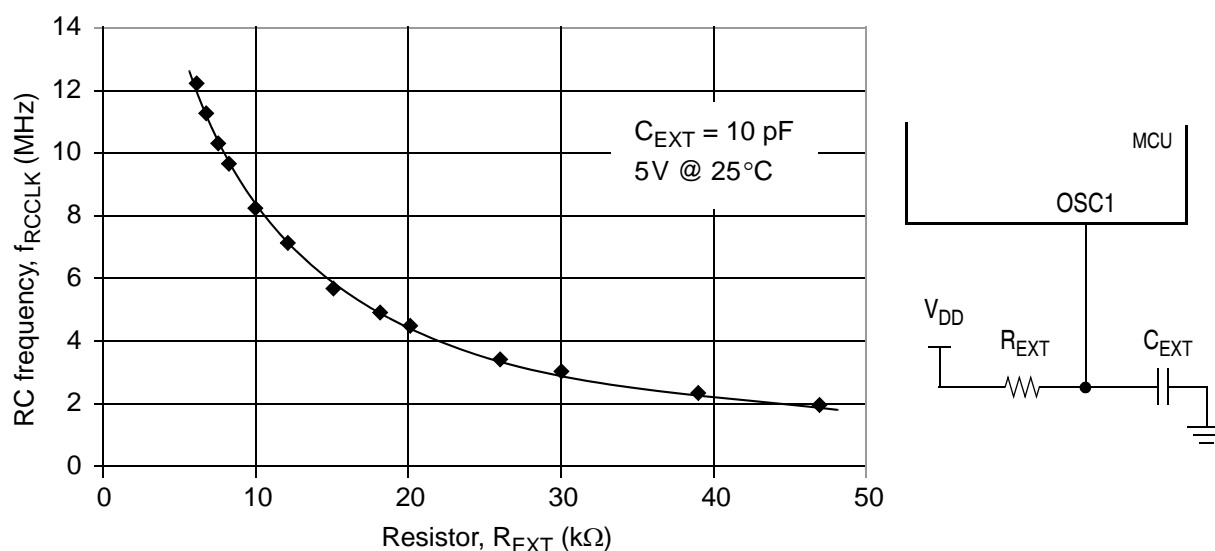
## 18.8 5V Oscillator Characteristics

**Table 18-6. Oscillator Component Specifications (5V)**

Characteristic	Symbol	Min	Typ	Max	Unit
Crystal frequency, XTALCLK	$f_{\text{OSCCLK}}$	—	10	32	MHz
RC oscillator frequency, RCCLK	$f_{\text{RCCLK}}$	2	10	12	MHz
External clock reference frequency <sup>(1)</sup>	$f_{\text{OSCCLK}}$	dc	—	32	MHz
Crystal load capacitance <sup>(2)</sup>	$C_L$	—	—	—	
Crystal fixed capacitance <sup>(2)</sup>	$C_1$	—	$2 \times C_L$	—	
Crystal tuning capacitance <sup>(2)</sup>	$C_2$	—	$2 \times C_L$	—	
Feedback bias resistor	$R_B$	—	10 M $\Omega$	—	
Series resistor <sup>(2), (3)</sup>	$R_S$	—	—	—	
RC oscillator external R	$R_{\text{EXT}}$	See <b>Figure 18-1</b>			
RC oscillator external C	$C_{\text{EXT}}$	—	10	—	pF

**NOTES:**

1. No more than 10% duty cycle deviation from 50%
2. Consult crystal vendor data sheet
3. Not Required for high frequency crystals



**Figure 18-1. RC vs. Frequency (5V @ 25°C)**

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